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Cost-Effective Co-Optimization of RF Process Technology Targeting Performances/Power/Area Enhancements for RF and mmWave Applications

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Abstract: In this paper, we propose a cost-effective way to tune RF process technology to achieve well-optimized RF and mmWave performances/power/area by tweaking back-end-of-line (BEOL) configurations. This paper suggests that the most favorable altitude is that of an ultra-thick-metal (UTM) layer from the silicon substrate, and the effort also focuses on the calibration of the via height/pitch underneath the UTM to satisfy the least ohmic loss in the interface between the active and passive device components. We implemented a process optimization in a 28 nm fully depleted silicon-on-insulator (FD-SOI) process technology, and the results show performance enhancements on the inductor, achieving a 14.8% quality factor improvement and a 13.1% self-resonance frequency improvement. This paper also showcases how the process optimization boosts 29 GHz LNA performances, with a 31.8% gain in boosting and a 9.1% reduction in noise-figure.

Keywords: low-noise amplifier (LNA); performances/power/area (PPA); ultra-thick-metal (UTM)

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1. Introduction

In the development of modern advanced silicon process technology, one of the primary focuses is on increasing front-end-of-line (FEOL) device density by reducing device dimensions, including a channel length reduction for device speed advantages. However, the FEOL shrinkage enforces the back-end-of-line (BEOL) to be scaled down to match with the FEOL scaling for interconnects. BEOL scaling implies not only a reduction in the metal width, but also the metal thickness to prevent aggravating the RC constant time imposed by the metal interconnects.

Though the thinner metal layers allow for an increased number of metal layers to be packed in an adequate die thickness for handling, packaging, and so on, every metal layers becomes closer to the silicon substrate. Hence, due to the more complicated high frequency interactions among the metal layers and with the silicon substrate present, the magnetic and electric interactions in RF chips yield lower performances for passive RF components, such as inductors, transmission lines, and metal capacitors.

The additional metal stack can increase the distance of the UTM to the substrate [1–4]. Due to this, the mask process increased. And if the UTM-to-substrate distance is increased, the characteristics of the RF passive device are improved, but other active circuits may be deteriorated due to the increase in the routing resistance.

2. Problem Statement

As the position of ultra-thick-metal (UTM) layer becomes closer to the silicon substrate, negative effects on passive RF components occur. Figure 1a shows the quasi-TEM modes occurring in the substrate due to microwave and millimeter wave frequencies, as well as the

deep penetration of the E-field and H-field into the substrate. Figure 1b shows the E-field within the substrate according to frequency, using an HFSS EM simulator. We obtained the material and thickness information for EM simulations from foundry technology files, which were then calibrated through the silicon validation of a general inductor pattern. Based on these considerations, the next part presents a solution to circumvent these losses. Firstly, the proximity of the UTM layer to the substrate increases an electrical coupling to the substrate, as shown in Figure 1c. The increased electrical coupling lowers the self-resonance frequency (SRF), with an increased coupling capacitance to the substrate. Note that the dropped SRF handicaps the maximum operation frequency. The increased electrical coupling also gives rise to an aggravated displacement current loss because of the lossy substrate grounding, as illustrated in Figure 1d. Secondly, the penetration of electrical fields into the silicon substrates becomes deeper, as the operating frequency is increased. The increasing depth of the penetration worsens the dielectric loss due to the lossy silicon substrate material. Lastly, more magnetic flux interacts with the silicon substrate as the UTM layer becomes closer to the silicon substrate, and hence one can notice the increasing Eddy current loss through the increasing magnetic coupling, as depicted in Figure 1e. As shown in Figure 1f, a total effective magnetic flux surrounding the UTM layer generated by AC current flows is diminished as the space between the UTM layer and the silicon substrate narrows. The consequence of this is a reduced inductance density for an equivalent inductor dimension.

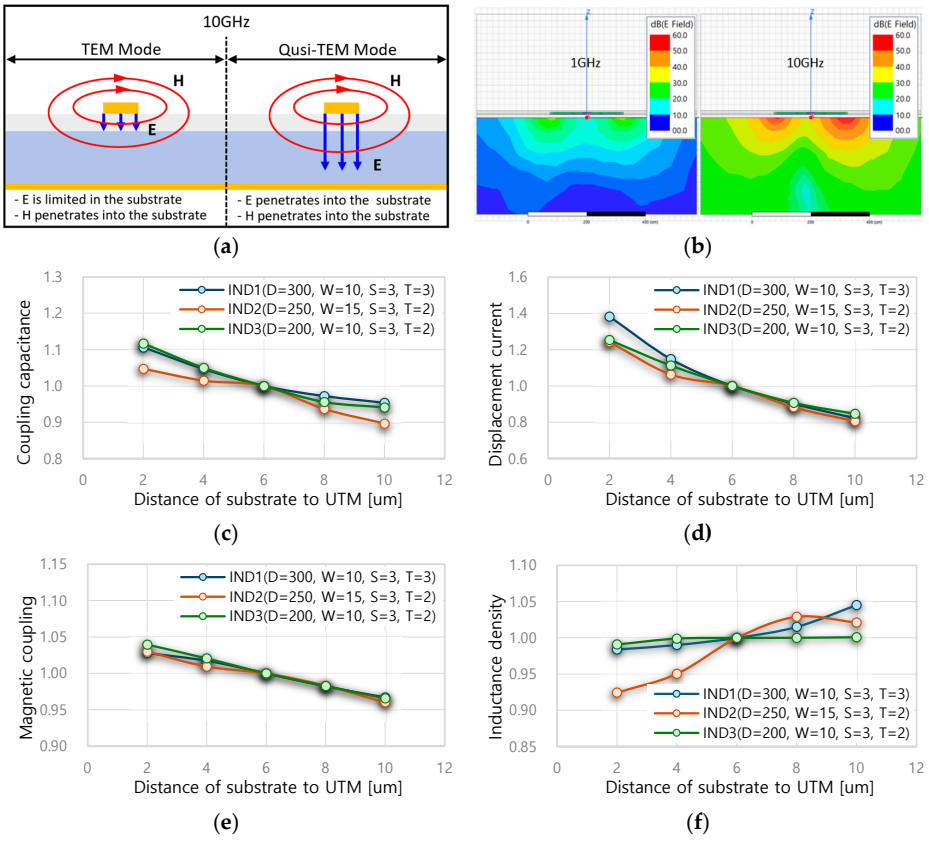


Figure 1. Potential performance affects in relation to the distance of the UTM layer to the substrate: (**a**) different modes of propagation; (**b**) E-field variation according to frequency; (**c**) normalized coupling capacitance; (**d**) normalized displacement current; (**e**) normalized magnetic coupling; and (**f**) normalized inductance density.

Therefore, the research objective is to find a fair position for the UTM layer without compromising full circuit integration for three purposes. One purpose is to minimize the magnetic loss and the electrical loss on RF passive components, and the second is not to impose excessive ohmic losses on metal interconnects through multi-via chain from

FEOL devices to the top of the metal layers, which is the UTM layer. The third purpose, therefore, is to accomplish an RF circuit performance enhancement that can exchange with area optimizations and power minimizations. In this paper, the proposed optimization method proves the advancement by evaluating the quality of several passive components, such as the inductor and transmission lines, in the RF (<10 GHz) and mmWave (>10 GHz) frequency ranges.

3. Experiments

Loss mechanisms associating with the UTM altitude described earlier are used to simply drive the desires of the most favorable UTM position for the process-aided RF circuit performance enhancement. The observation of the electric field and magnetic field profiles in an integrated silicon material is the first step to understand the various loss mechanisms at various frequency ranges. There are three scenarios in the observation of the depths of the E-field in a UTM layer inductor, as follows: (1) substrate surface with n-type epitaxial layer (N_{epi}), as suggested in [5]; (2) without N_{epi}; and (3) with patterned-ground-shield (PGS) [6–8].

As presented in Figure 2a, the penetration depth of the E-field determines the total amount of dielectric loss of the lossy substrate material, and Figure 2b summarizes the dielectric loss amount for each inductor configuration. Four key performance metrics of inductors, such as (1) the peak quality factor (Q_{max}), (2) the self-resonance-frequency (SRF), (3) the coupling capacitance to the substrate (C_{ox}), and (4) the effective line inductance (L_{eff}), are evaluated for various distances of the UTM layer from the silicon substrate, as shown in Figure 2c–f. The results suggest the improvement of peak Q, and the SRF is saturated beyond a distance of 7 um, while L_{eff} is slightly increased as the UTM becomes further away from the substrate.

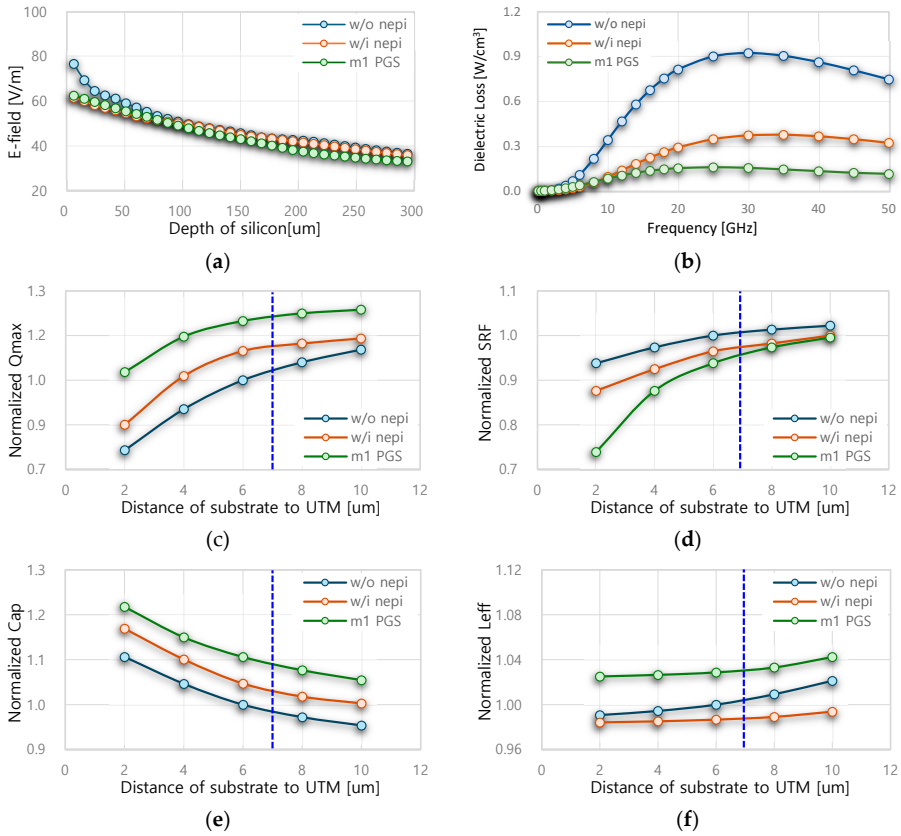


Figure 2. Optimization of UTM height for an inductor, using the HFSS EM simulator: (**a**) electric-field; (**b**) dielectric loss; (**c**) normalized Q_{max}; (**d**) normalized self-resonance frequency; (**e**) normalized capacitance; and (**f**) normalized inductance.

4. Process Optimization

The increased height of the via underneath the UTM layer escalates the UTM position. A similar previous work showed the effectiveness of the escalated UTM position by simply adding more metal layers at the cost of extra masks and processing steps [2]. Instead of adding complexity in the BEOL process, fabricating the taller via underneath the UTM does the trick, as far as concerns the process of choice balances via resistance for the benefit of the escalated UTM position at various frequency ranges.

Three process aspects determining via contact resistance (R_c) density are (1) via aspect ratio, (2) pitch of the via process implying via diameter (D_{via}) and the spacing between vias (S_{via}), and (3) a composition of materials for via fabrication. The optimization of the via height incorporates all three of these aspects.

Figure 3 describes the via structures under consideration, and Tables 1 and 2 tabulate the compositions of the materials for via fabrication. As the via height increases, a portion of the main via material, Cu, dominates the overall R_c, while the thickness of the barrier materials is unchanged. The aspect ratio of the via needs to be maintained in order to not affect a profile of vertical via shape, which causes potential voids during via fabrication. Meanwhile, reliability requirements, such as time-dependent dielectric breakdown (TDDB), determine a minimum via spacing, which depends slightly on via height. One can maintain the minimum via spacing, as long as the reliability requirement is satisfied.

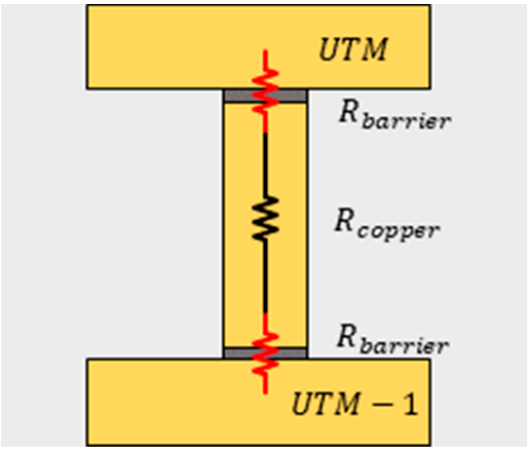


Figure 3. Via structure.

Table 1. Material compositions and dimension of vias.

	Material	Resistivity [uΩ-m]	Normalized Height	Normalized Area
Conventional	Cu	0.017	1.0	1.0
	Barrier	3~5	0.06	1.0
Elevated Via	Cu	0.017	4.10	4.0
	Barrier	3~5	0.06	4.0

Table 2. Reduction in via R_c through process optimization.

	Normalized via Height	Normalized via Pitch	Aspect Ratio	Normalized via R_c	Normalized R_c Density
Conventional	1.0	1.0	6.48	1.0	1.0
Elevated Via	4.0	1.45	6.48	0.42	0.71

As per the results, Figure 4a summarizes the trend of via contact resistance (R_c) according to via heights. Figure 4b also summarizes via contact resistance density according to via height complying to reliability requirements with a minimum allowable via spacing.

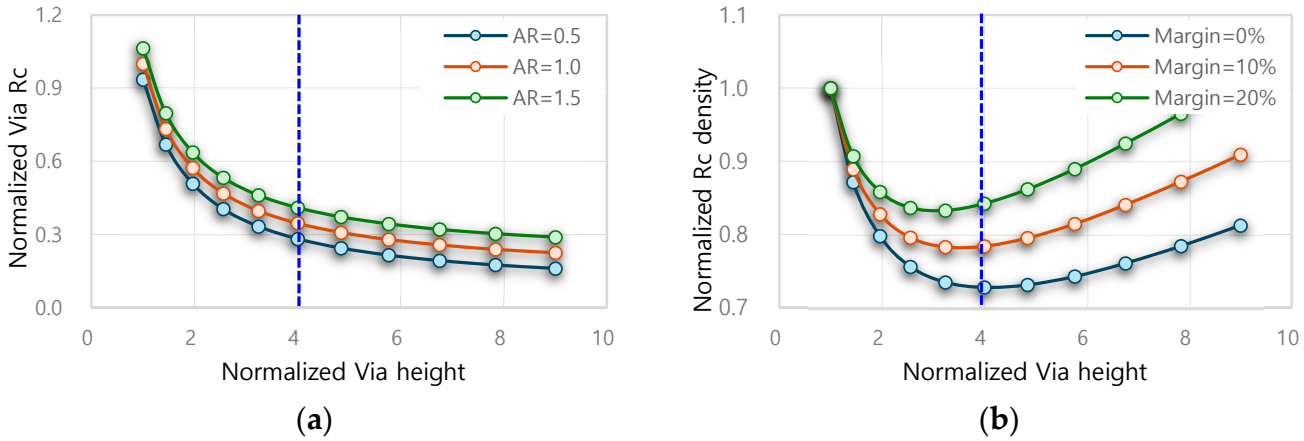


Figure 4. Optimization of via height for active circuit integration: (**a**) normalized via contact resistance (R_c) by aspect ratio (AR); (**b**) normalized via contact resistance (R_c) density.

4.1. DC Result of Process Optimization

The investigation of the altitude of the UTM layer takes into account the UTM position on E-field/M-field couplings, as well as the change in via resistance as a result of process modifications. The conclusion suggests escalating the via height to position the UTM layer at an optimal cost-effective position away from the silicon substrate, as illustrated in Figure 5. One can find the photos of the vertical via profile before and after process modification in Figure 6a. Figure 6b illustrates the total resistance from the full via stacks from the lowest via metal to the highest metal layer (also known as the UTM layer), which drops by as much as one-third.

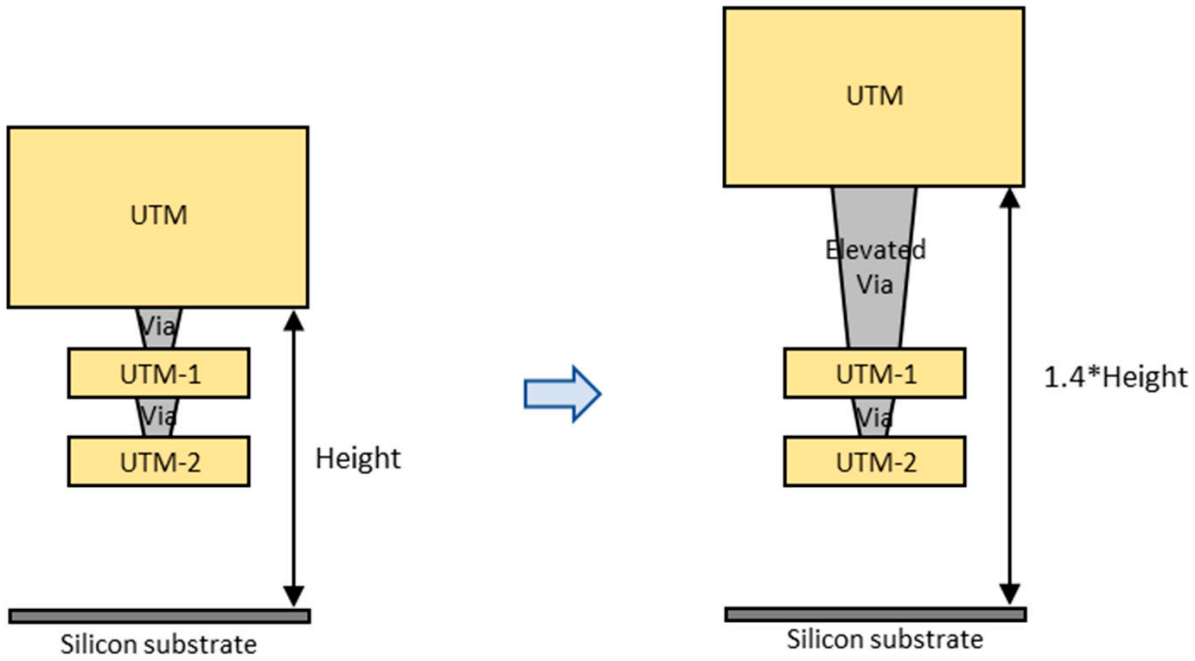


Figure 5. Proposed process optimization for RF/mmWave applications without additional processes.

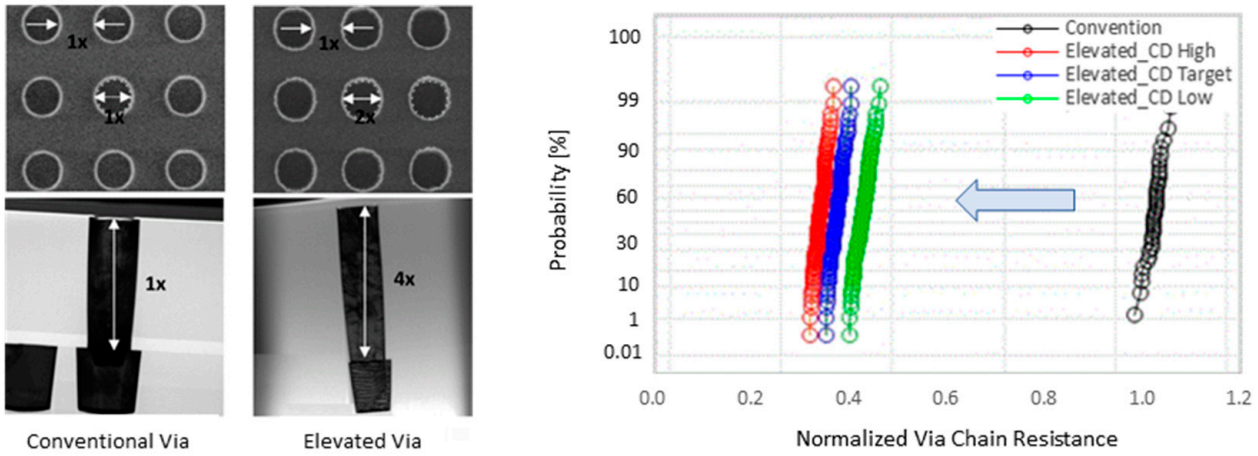


Figure 6. Setup results of proposed elevated UTM processes: (**a**) CD/TEM images; (**b**) via chain contact resistance (R_c).

4.2. Measurement Results of Micro-Strip

Circuit designs for RF/mmWave applications require a 50 ohm transmission line. However, one layer of a technologically advanced metal has a small width/thickness, so insertion loss is serious when implementing microstrip line and coplanar waveguide (CPW); so, UTM-1 and UTM-2 metals are used as ground metals. Since UTM-2 has a short distance, the UTM width is reduced to 50 ohms, so that the insertion loss is inevitably large. In this paper, it is possible to fabricate a 50 ohm transmission line using UTM-1 and UTM-2 by increasing the height of the via below the UTM layer.

We provide the total effect of the escalated UTM position, and the re-engineered via process on a microstrip line design in Figure 7. Figure 7a displays the normalized characteristic impedances of the microstrip line fabricated in the UTM layer with various widths and altitudes. Figure 7b depicts the insertion loss according to the UTM positions. One can understand how to find an optimum UTM position for one's target applications by observing Figure 7.

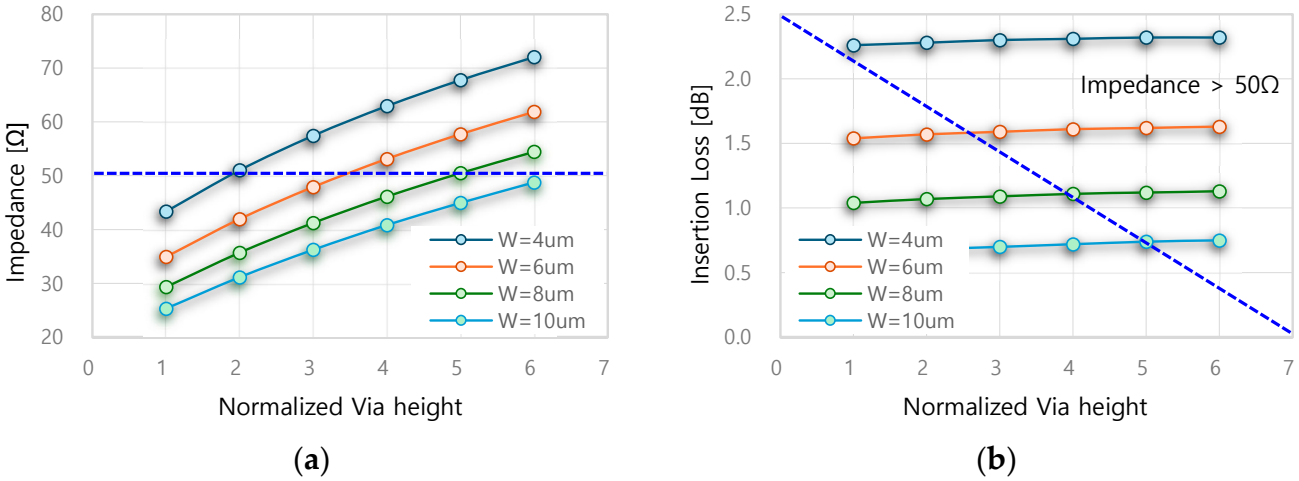


Figure 7. Optimization of via height for microstrip line: (**a**) characteristic impedance of microstrip line; (**b**) insertion loss of microstrip line.

4.3. Measurement Results of Passive Components

Figure 8 demonstrates the performance improvement of an inductor fabricated in a UTM layer at the targeted position, and one can notice the 14.8% Q-factor enhancement

and the 13.1% SRF increase as a result of nothing but the elevated UTM position, as shown in Figure 8a and b, respectively. The experiment with a microstrip line also achieves a higher characteristic impedance with a lower insertion loss (IL), as shown in Figure 8c and d, respectively. Tables 3 and 4 summarize the measurements of the fabricated inductor and microstrip line with only elevated UTM processes.

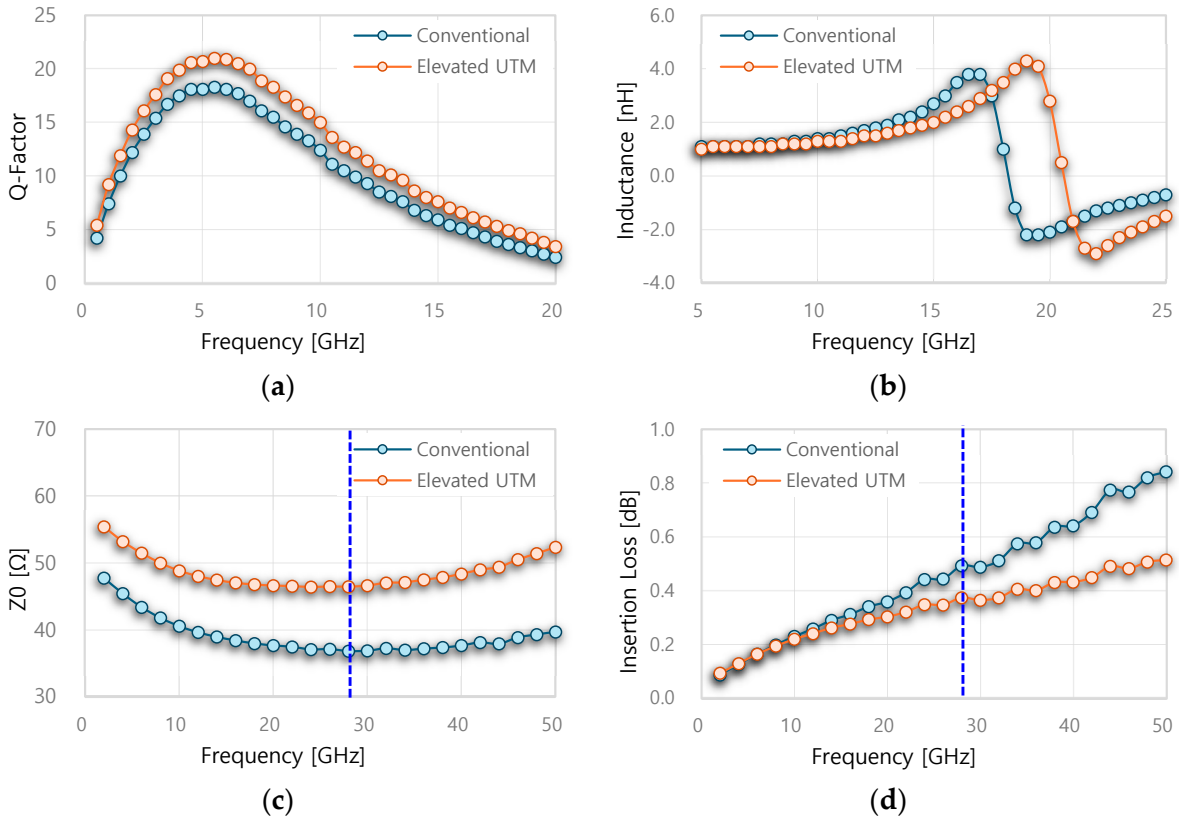


Figure 8. Measurement results of the proposed elevated UTM process: (**a**) Q-factor of inductor; (**b**) inductance of inductor; (**c**) characteristic impedance of microstrip line; (**d**) insertion loss of microstrip line.

Table 3. Measured inductor characteristics.

	Conventional	Elevated UTM
Normalized Inductance	1.00	1.05
Normalized Q_{max}	1.00	1.15
Normalized SRF	1.00	1.13

Table 4. Measured microstrip characteristics.

	Conventional	Elevated UTM
Normalized Impedance	1.00	1.26
Normalized Insertion Loss	1.00	0.75

4.4. Measurement Results of RF Circuit

For the demonstration of the effectiveness of the escalated UTM position, we fabricated a low-noise amplifier (LNA) [9,10] tuned at 29 GHz in a 28 nm FD-SOI process, as shown in Figure 9a,b. A cascoded LNA topology is chosen for its simplicity and the footprints of all device components are untouched both before and after the process modification, except for the via layer elevating the UTM. Therefore, one can assume the majority of performance

improvements are in relation to the process change only. Note that the processing cost change is negligible, since no additional layers are used.

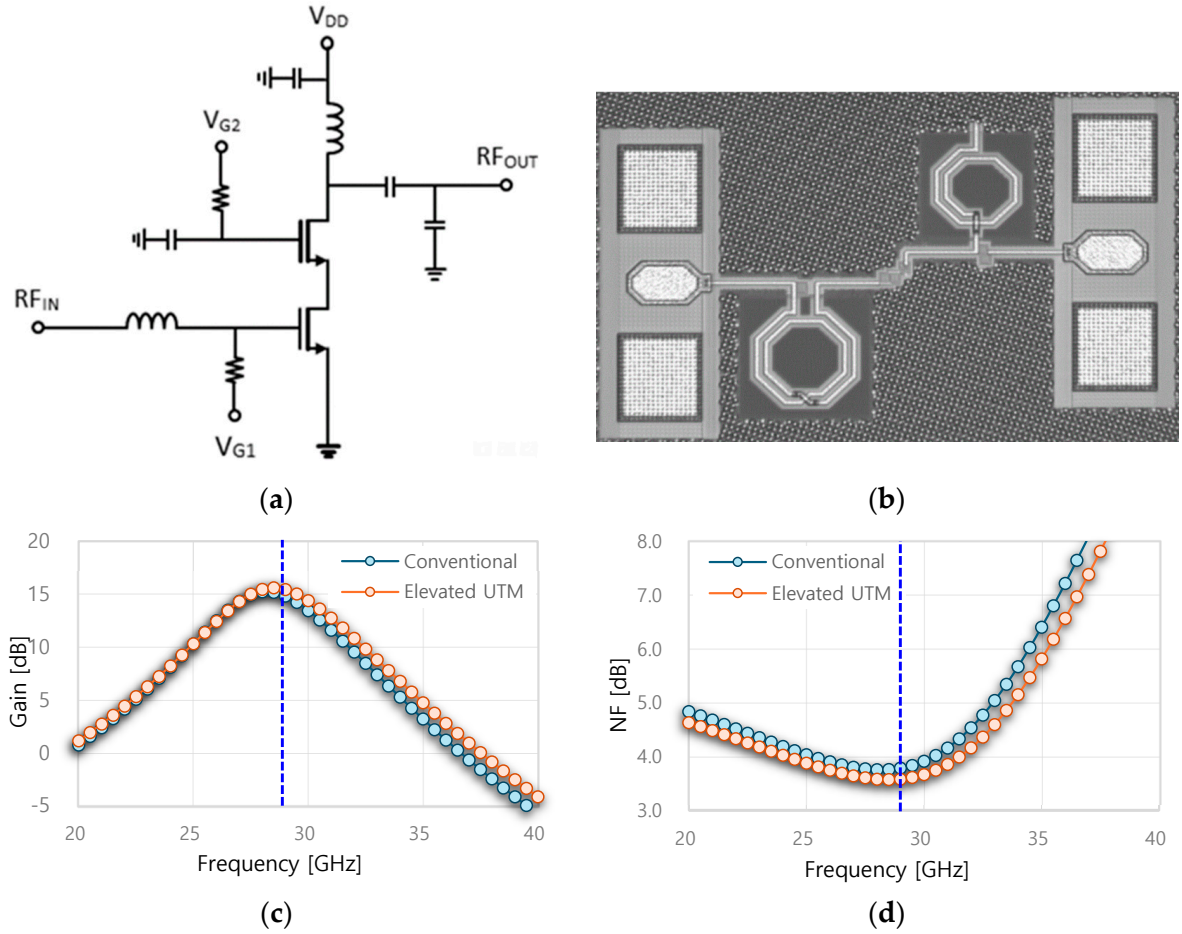


Figure 9. Test results of 29GHz LNA: (**a**) topology of 29GHz LNA; (**b**) chip image; (**c**) gain; and (**d**) noise figure.

We measured more than 30 chips at the same wafer and location. Among them, this is a demonstration of the data of a chip with a medium value. The reduction in the IL in the input and output matching networks contributes to the signal gain, S_{21}, by as much as 31.8%, as shown in Figure 9c and Table 5. Also, the process change drops the min-imum noise figure by 9.1% thanks to the reduced input IL, according to Figure 9d and Table 5.

Table 5. Summary of 29 GHz LNA.

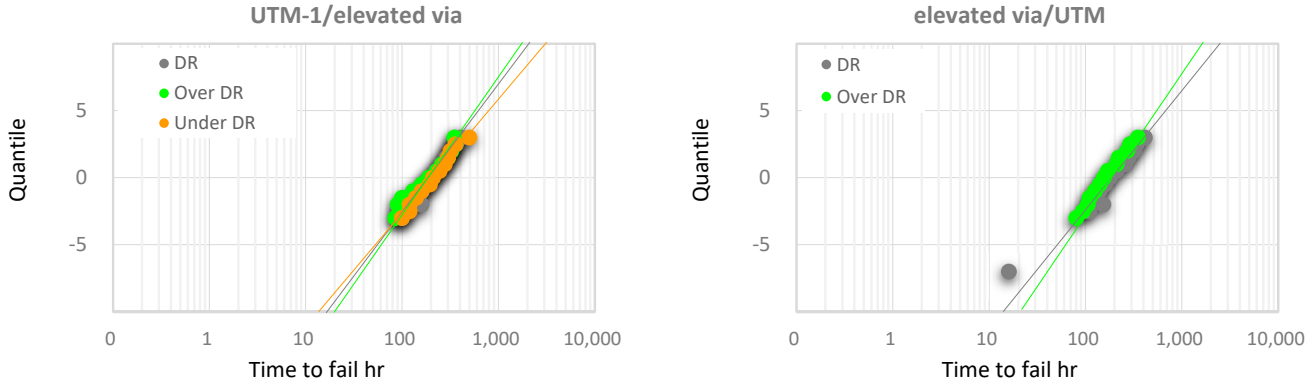
	Conventional	Elevated UTM
Normalized Gain	1.00	1.32
Normalized Noise Figure	1.00	0.91

4.5. Measurement Results of Reliability

In this paper, the minimum via spacing according to via height was determined to satisfy reliability requirements such as time-dependent dielectric breakdown. And the via resistance of the optimized process is lowered by 1/3, which can be expected to improve the performance of the logic circuit.

The reliability of the proposed elevated UTM process was tested in the 28FDS process, and the back-end-of-line reliability focuses on electro migration (EM), stress migration (SM), and time-dependent dielectric breakdown (TDDB).

EM measures the change in resistance caused by the movement of matter due to the continuous movement of ions within a conductor, which, in turn, is caused by changes in momentum between conducting electrons and diffusing metal atoms. Figure 10 shows that the EM structure within the process window passed the accelerated reliability test. This guarantees that devices manufactured using the proposed process can be used for more than 10 years.



(**a**) (**b**)

Figure 10. Reliability test result: (**a**) EM results of UTM-1/elevated via; (**b**) EM results of elevated via/UTM. Criteria: J_{max} for 10 year lifetime at t0.1(TTF @0.1%) and T_{USE} (=125 °C), resistance shift <10% @10 year.

SM is a measurement that checks for voids, hillocks, and openings in metal wiring due to stress. Table 6 shows that all SM structures passed the 500 h accelerated reliability test. It was confirmed that the interconnection of the proposed elevated UTM process was reliable. And it shows improved reliability results due to the increase in via contact area.

Table 6. SM results.

Structure	Metal Layer	SM 500 h
EM meas.	UTM-1	Pass
	UTM	Pass
Isolation via	UTM Via	Pass
Via chain	UTM-1/UTM Via/UTM	Pass
Crack detection	UTM-2/UTM-1/UTM	Pass

Criteria: J_{max} for 10 year lifetime at t0.1 and T_{USE} (=200 °C), cumulative failure <1% @1000 h.

TDDB is an item that measures the oxide breakdown phenomenon and oxide life-time over time by applying a high temperature and a high voltage to the capacitor. As shown in Table 7, all TDDB structures passed the reliability test. This shows that there is no leakage current flowing into the hard breakdown of the capacitor during electrical stress.

Table 7. TDDB results.

Structure	Metal Layer	TDDB 500 cyc	TDDB 1000 cyc
EM meas.	UTM-1	Pass	Pass
	UTM	Pass	Pass
Isolation via	UTM Via	Pass	Pass
Via chain	UTM-1/Via/UTM	Pass	Pass
Crack detection	UTM-2/UTM-1/UTM	Pass	Pass

Criteria: 1.45 for(+) QT electrode, 1 V for general @125 °C, 1000 ppm, lifetime >10 yrs.

5. Conclusions

In this paper, the distance of the UTM layer to the substrate is increased by elevating the via height. This distance increase is carried out without additional mask processes by increasing the via height in order to maintain the same aspect ratio and is conducted with the same equipment. And a methodology for selecting the optimal width/height is performed, while maintaining the stability of the etch process by keeping the aspect ratio. Through this, the R_c per unit area was kept lower than before.

It is possible to fabricate a 50 ohm transmission line using UTM-1 and UTM-2 by increasing the height of the via below the UTM layer and the performance of the inductor could be dramatically improved. The effectiveness of the escalated UTM is shown using inductor and transmission line measurements using 28FDS technology, and has also been studied in LNA design with/without the escalated UTM and the elevated UTM via. The measurement of the LNA design reports an overall 30% improvement in loss counting integration loss by UTM via, the electric loss in the inductor, and the magnetic loss appearing in the transmission line for PAD connection.

The simple modification in UTM position gains a significant amount of performance improvements on interconnects and passive components without paying for extra process steps. The well-designed BEOL configuration can improve the performance with the cost of a negligible increase in turnaround time.

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Conflicts of Interest: Authors Sutae Kim and Hyungjin Lee were employed by the company Samsung. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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