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Investigation on newly designed low resistivity polyimide-type alignment layer for reducing DC image sticking of in-plane switching liquid crystal display

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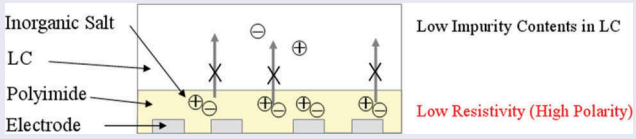
ABSTRACT

Soluble polyimide-type alignment layer is widely used in in-plane switching (IPS) liquid crystal display (LCD) because of its excellent reliability owing to high imidisation ratio during long-term driving, high voltage-holding ratio and low ion density. Nevertheless, it exhibits slow direct current (DC) discharging property due to its high resistivity, causing significant DC image-sticking problem. In this study, we doped inorganic salt to control the resistivity of soluble polyimide-type alignment layer and found that this approach reduced DC image sticking greatly without any loss of reliability property in IPS-LCD.



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In-plane switching; alignment layer; resistivity; image sticking

1. Introduction

Liquid crystal displays (LCDs) have grown into the most effective flat panel display (FPD) technology through satisfying various technological demands in wide applications. Especially, great improvements in image quality are achieved by overcoming narrow viewing angle characteristics of conventional twisted nematic [1] by several LC modes, such as multi-domain vertical alignment (MVA) [2–4], in-plane switching (IPS) [5–7] and fringe-field switching (FFS) [8–16]. Recently, the uses of LCDs for public information display are increasing gradually because LCDs have lots of merits, such as no burning effect, high brightness, low power consumption and high image quality. However, very long-time driving in this application causes unexpected non-uniformity in displayed image so-called mura in the image quality, as shown in Figure 1. Therefore, for this usage, LCDs require to have stronger reliability for long-term driving condition to prevent any kind of mura associated with image sticking and high temperature driving, compared to normal LCDs.

In general, the causes of both image sticking and mura during long-term driving are related to various sources including panel, mechanics and circuit design [17–19]. However, one of major origins of those mura is strongly related with liquid crystal (LC) and alignment layer in LCDs [20]. In real thin-film transistor (TFT)-LCD driving, a pure alternating current (AC) cannot be applied at all grey scales. In the driving, whenever a signal voltage is applied to a pixel via TFT, there is a voltage drop in the pixel named kick-back voltage, which is expressed as $\Delta V_p = C_{gd}\Delta V_g/[C_{gd} + C_{st} + C_{lc}(V)]$, where C_{gd} is the gate-drain parasitic capacitance of a TFT, C_{st} and C_{lc} represent the storage and LC capacitance, respectively, and V_g denotes the gate voltage [21]. The C_{lc} is voltage-dependent so that ΔV_p is not a constant value during displaying different grey scales. Consequently the driving method in TFT-LCDs renders common voltage (V_{com}) difference depending on grey scales, and thus having a single set of V_{com} value results in a net direct current (DC) voltage applied to LC layer. As a result, applied DC voltage will attract ions near electrodes and the accumulated ions at an interface between LC and alignment layer form residual DC (R-DC) voltage, which affects signal voltage applied to the LC layer, as shown in Figure 2 [22]. In general, a quite large amount of ions

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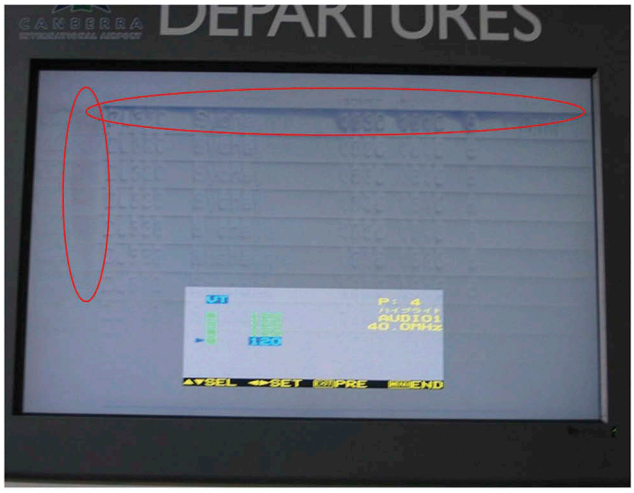

Figure 1. One example of exhibiting the appearance of uneven displayed image after long-term liquid crystal display (LCD) driving.

exist inside LC layer, and when AC voltage with 60 Hz is applied to the panel, ions do not accumulate near electrodes but instead they do diffuse inside LC layer [see Figure 2(a)]. However, when a net DC exists between electrodes via black and white checkboard pattern to observe image sticking in LCDs, ions can be attracted to the electrodes [see Figure 2(b)] and can be accumulated at an interface between LC and alignment layers [see Figure 2(c)]. The accumulated ions form net DC, such that amplitude of applied AC signal voltage will be distorted by the formed DC, result in distortion of the displayed image called image sticking.

Further, alignment layers influence strongly on the adsorption and discharge characteristics of ion impurities in the IPS/FFS cells [23,24]. Polyimide (PI) is widely used alignment material of recent commercial LCDs. In general, PI alignment materials are classified into soluble polyimide (SPI) type and polyamic acid (PAA) type with their main bond structure in a solution state. Especially, compared to PAA-type alignment layer [25], SPI-type alignment layer has higher resistivity than that of LC and excellent reliability during long-term LCD driving because of their high imidisation ratio, high voltage-holding ratio and low ion density [26]. In this work, the dependences of electrical properties and impurity properties of PI alignment layers on DC image sticking and long-term reliability in the IPS LCD have been investigated. In addition, we tried to find new approaches to improve the trade-off characteristics of the image sticking and long-term reliability with newly proposed alignment layer.

2. R-DC properties of IPS LCD related with resistivity of alignment layer

In general, the chemical structure and physical properties of alignment layer not only decide initial direction of LC, but also determine the charging and discharging rate in the liquid crystal layer of the IPS LC cell in accordance with its resistivity when the DC voltage is applied to the cell. Usually, R-DC in IPS LCD directly has a bad influence on DC image sticking and the level of R-DC is strongly related to resistivity of alignment layer [27]. DC charging and discharging property is explained using an equivalent circuit modelling of normal IPS cell structure, as shown in Figure 3. Pixel (PXL) and common (COM) electrodes exist in the same layer above passivation layer with proper

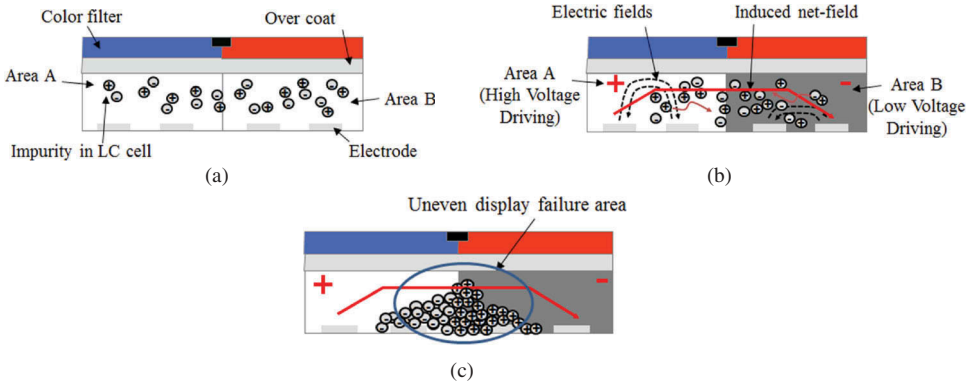

Figure 2. Schematic mechanism of displayed image in LCDs. (a) Initial state of image-sticking pattern driving: high electric field (full white driving voltage) is induced in the area A, low electric field (black driving voltage) is induced in area B, in which all ionic impurities are evenly existed in all LC areas. (b) Because of voltage difference between area A and area B, internal net field induced near border areas between A and B. (c) After long-term driving with image-sticking pattern, ion impurities move to DC trapped area and these impurities degrade the effective voltage in border area of LC cell, so, brightness change happened in this area. Furthermore, according to increase in driving time, this area is increased gradually.

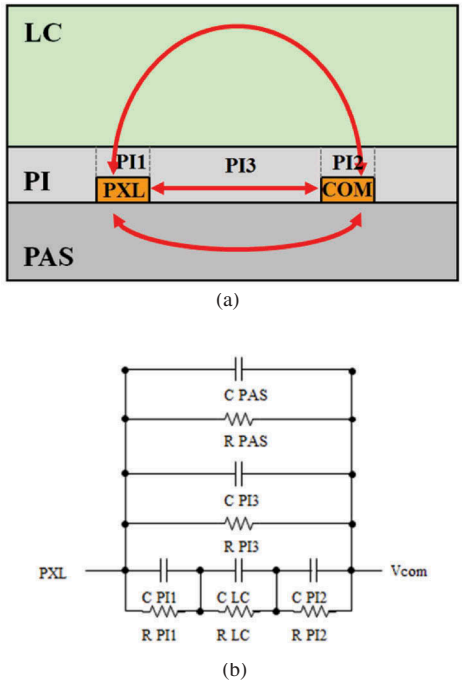

Figure 3. (colour online) (a) Cross-section figure of normal IPS mode structure. Here, LC is liquid crystal layer, PAS is passivation layer, PXL is pixel electrode, COM is common electrode, PI is alignment layer, PI1 is PI upon the pixel electrode, PI2 is PI upon the common electrode and PI3 is PI, and (b) its equivalent circuits.

electrode width and the distance between them, the alignment layer covers electrode and the LC layer exists above the alignment layer. Based on Gauss's law [28], the surface charge density δ led to the interface of LC and PI is

$$\begin{aligned}\delta &= D_{\mathrm{LC}} - D_{\mathrm{PI}} = \varepsilon_0(\varepsilon_{\mathrm{LC}}E_{\mathrm{LC}} - \varepsilon_{\mathrm{PI}}E_{\mathrm{PI}}) \\ &= \tfrac{\varepsilon_0 V_{\mathrm{DC}}}{2\rho_{\mathrm{PI}}d_{\mathrm{PI}}+\rho_{\mathrm{LC}}d_{\mathrm{LC}}}(\varepsilon_{\mathrm{LC}}\rho_{\mathrm{LC}} - \varepsilon_{\mathrm{PI}}\rho_{\mathrm{PI}}),\end{aligned} \tag{1}$$

where D_{LC} and D_{PI} are electric flux density of LC layer and PI layer, ρ_{LC} and ρ_{PI} are the resistivity of LC layer and PI layer, $\varepsilon_{\mathrm{LC}}$, $\varepsilon_{\mathrm{PI}}$ and ε_0 are dielectric constant of LC, PI and in vacuum, respectively, and d_{LC} is a distance between pixel electrode and common electrode, and d_{PI} is a thickness of PI. When the DC voltage (V_{DC}) is applied to between PXL and COM electrodes, the electric field crosses PXL–PI1–LC–PI2–COM layers, as shown in Figure 3(a), and when shorting of both electrodes is assumed, the voltage of PI layer ($V_{\mathrm{PI}} = V_{\mathrm{PI1}} = V_{\mathrm{PI2}}$) and voltage of LC layer (V_{LC}) satisfies the following relation:

$$0 = V_{\mathrm{PI}} + V_{\mathrm{LC}} + V_{\mathrm{PI}}. \tag{2}$$

From Equations (1) and (2), the surface charge density δ led to the interface of LC and PI is following relation:

$$\begin{aligned}\varepsilon_0\varepsilon_{\mathrm{LC}}E_{\mathrm{LC}} - \varepsilon_0\varepsilon_{\mathrm{PI}}E_{\mathrm{PI}} &= \varepsilon_0\varepsilon_{\mathrm{LC}}\frac{V_{\mathrm{LC}}}{d_{\mathrm{LC}}} - \varepsilon_0\varepsilon_{\mathrm{PI}}\frac{V_{\mathrm{PI}}}{d_{\mathrm{PI}}} \\ &= V_{\mathrm{LC}}\varepsilon_0\left(\frac{2\varepsilon_{\mathrm{LC}}d_{\mathrm{PI}} + \varepsilon_{\mathrm{PI}}d_{\mathrm{LC}}}{2d_{\mathrm{PI}}d_{\mathrm{LC}}}\right) \\ &= \delta.\end{aligned} \tag{3}$$

From Equations (1) and (3), initial voltage in LC layer (V_{LC0}) led by a DC voltage (V_{DC}) satisfies the following relation:

$$V_{\mathrm{LC0}} = V_{\mathrm{DC}}\left(\frac{2d_{\mathrm{PI}}d_{\mathrm{LC}}}{2\varepsilon_{\mathrm{LC}}d_{\mathrm{PI}} + \varepsilon_{\mathrm{PI}}d_{\mathrm{LC}}}\right)\left(\frac{\varepsilon_{\mathrm{LC}}\rho_{\mathrm{LC}} - \varepsilon_{\mathrm{PI}}\rho_{\mathrm{PI}}}{2\rho_{\mathrm{PI}}d_{\mathrm{PI}} + \rho_{\mathrm{LC}}d_{\mathrm{LC}}}\right). \tag{4}$$

As an electric current I flown to PXL–PI1–LC–PI2–COM is direct electric current, all electric currents I_{PI1}, I_{LC} and I_{PI2} passed to PI1, LC and PI2, respectively, are the same to each other:

$$\begin{aligned}I_{\mathrm{PI1}} = I_{\mathrm{PI2}} = I_{\mathrm{PI}} = I_{\mathrm{LC}} = I &= i_R + i_C \\ &= \frac{V}{R} + C\frac{\mathrm{d}V}{\mathrm{d}t},\end{aligned} \tag{5}$$

$$I = \frac{V_{\mathrm{PI}}}{R_{\mathrm{PI}}} + C_{\mathrm{PI}}\frac{\mathrm{d}V_{\mathrm{PI}}}{\mathrm{d}t} = \frac{V_{\mathrm{LC}}}{R_{\mathrm{LC}}} + C_{\mathrm{LC}}\frac{\mathrm{d}V_{\mathrm{LC}}}{\mathrm{d}t}, \tag{6}$$

$$\frac{\mathrm{d}V_{\mathrm{LC}}}{\mathrm{d}t} = -\left(\frac{R_{\mathrm{LC}} + 2R_{\mathrm{PI}}}{R_{\mathrm{LC}}R_{\mathrm{PI}}(C_{\mathrm{PI}} + 2C_{\mathrm{LC}})}\right)V_{\mathrm{LC}}. \tag{7}$$

Then, we get

$$V_{\mathrm{LC}} = V_{\mathrm{LC0}}e^{-t/\tau}\,\tau = R_{\mathrm{LC}}R_{\mathrm{PI}}\left(\frac{C_{\mathrm{PI}} + 2C_{\mathrm{LC}}}{R_{\mathrm{LC}} + 2R_{\mathrm{PI}}}\right), \tag{8}$$

where C_{LC} and C_{PI} are the capacitance of LC and PI layer, R_{LC} and R_{PI} are the resistance of LC layer and PI layer, respectively, and V_{LC0} is initial applied DC voltage to LC cell. Since R_{LC} and R_{PI} are equal to $\rho_{\mathrm{LC}}d_{\mathrm{LC}}$ and $\rho_{\mathrm{PI}}d_{\mathrm{PI}}$, respectively, and C_{PI} and C_{LC} are also equal to $\varepsilon_{\mathrm{PI}}\varepsilon_0/d_{\mathrm{PI}}$ and $\varepsilon_{\mathrm{LC}}\varepsilon_0/d_{\mathrm{LC}}$, respectively, time constant τ of residual DC is given by the following relation:

$$\begin{aligned}\tau &= R_{\mathrm{LC}}R_{\mathrm{PI}}\left(\frac{C_{\mathrm{PI}} + 2C_{\mathrm{LC}}}{R_{\mathrm{LC}} + 2R_{\mathrm{PI}}}\right) \\ &= \rho_{\mathrm{LC}}\rho_{\mathrm{PI}}\left(\frac{d_{\mathrm{LC}}\varepsilon_{\mathrm{PI}}\varepsilon_0 + 2d_{\mathrm{PI}}\varepsilon_{\mathrm{LC}}\varepsilon_0}{d_{\mathrm{LC}}\rho_{\mathrm{LC}} + 2d_{\mathrm{PI}}\rho_{\mathrm{PI}}}\right).\end{aligned} \tag{9}$$

Therefore, in case of DC discharging state in a condition that DC voltage (V_{DC}) flows into this circuit, residual DC (V_{LC}) led after the stabilisation is defined as

$$V_{\mathrm{LC}} = V_{\mathrm{DC}}\left(\frac{2d_{\mathrm{PI}}d_{\mathrm{LC}}}{2\varepsilon_{\mathrm{LC}}d_{\mathrm{PI}} + \varepsilon_{\mathrm{PI}}d_{\mathrm{LC}}}\right)\left(\frac{\varepsilon_{\mathrm{LC}}\rho_{\mathrm{LC}} - \varepsilon_{\mathrm{PI}}\rho_{\mathrm{PI}}}{2\rho_{\mathrm{PI}}d_{\mathrm{PI}} + \rho_{\mathrm{LC}}d_{\mathrm{LC}}}\right) e^{-\frac{t}{\rho_{\mathrm{LC}}\rho_{\mathrm{PI}}}\left(\frac{d_{\mathrm{LC}}\rho_{\mathrm{LC}} + 2d_{\mathrm{PI}}\rho_{\mathrm{PI}}}{d_{\mathrm{LC}}\varepsilon_{\mathrm{PI}}\varepsilon_0 + 2d_{\mathrm{PI}}\varepsilon_{\mathrm{LC}}\varepsilon_0}\right)}. \tag{10}$$

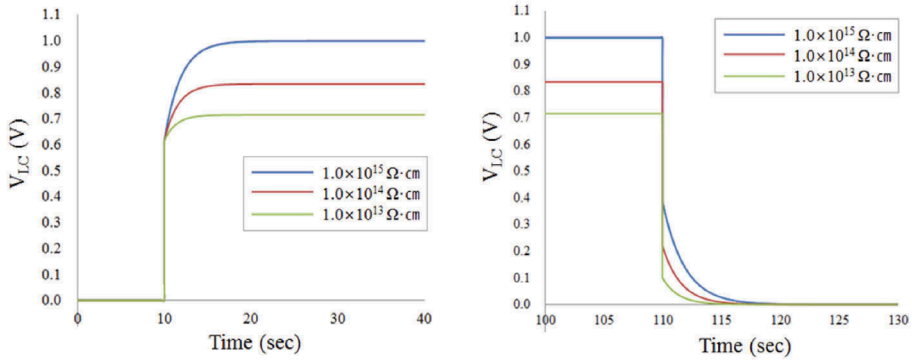

Figure 4. (colour online) The DC charging–discharging simulation results [all capacitances and resistivities used real value in calculation. Here, resistivity of PI is changed with three cases (1.0×10^{13}, 1.0×10^{14} and 1.0×10^{15} Ω cm)]. (a) Fitted graph of the voltage induced at LC layer versus time. (a) During DC charging period: 0 V driving proceeds for 10 s, and then proceed to 1 V DC driving during 100 s. (b) During DC discharging period: after driving condition (a), LC cell was conducted 0 V driving in the last 30 s.

On the other hand, in case of charging in a condition that DC voltage (V_{DC}) flows into this circuit, charged DC in LC layer (V_{LC}) is defined as

$$V_{LC} = V_{DC}\left(\frac{2d_{PI}d_{LC}}{2\varepsilon_{LC}d_{PI} + \varepsilon_{PI}d_{LC}}\right)\left(\frac{\varepsilon_{LC}\rho_{LC} - \varepsilon_{PI}\rho_{PI}}{2\rho_{PI}d_{PI} + \rho_{LC}d_{LC}}\right) e^{-\frac{\rho_{LC}\rho_{PI}}{t}\left(\frac{d_{LC}\varepsilon_{PI}\varepsilon_0 + 2d_{PI}\varepsilon_{LC}\varepsilon_0}{d_{LC}\rho_{LC} + 2d_{PI}\rho_{PI}}\right)}. \quad (11)$$

From Equations (10) and (11), one can understand that R-DC (V_{LC}) and time constant τ depend on resistivity, thickness and dielectric constant of PI layer and LC layer, in a condition that there are no new ion impurities generated in each layer [29].

Based on the modelling, charging and discharging rate of the DC voltage in LC layer according to magnitude of resistivity of PI layer are calculated. As clearly observed in Figure 4, the lower the resistivity of PI layer, the faster the charging and discharging rate is. Therefore, the alignment layer with low resistivity is favoured to reduce DC image sticking in the IPS LCD. On the other hand, high reliability is also strongly required in LCDs, and thus the alignment layer with low impurity is also required to meet the requirements. Conclusively speaking, an alignment layer which has a fast residual DC discharging property and low impurity property for both low DC image sticking and high reliability must be designed.

3. Experimental conditions including cell and materials information

At first, four different types of PI materials with different resistivities were prepared in order to find out the correlation between DC image-sticking property/reliability property and resistivity of PI layer. All PI materials tested are commercially available: PI-A (JALS-146, Japan Synthetic Rubber, Japan), which is SPI type, PI-B (X784, Chisso, Japan), PI-C (X785, Chisso, Japan), and PI-D (X755, Chisso, Japan) which are PAA type. The resistivity of each alignment layer is 8.0×10^{15} Ω cm for PI-A, 9.4×10^{12} Ω cm for PI-B, 2.8×10^{12} Ω cm for PI-C and 6.3×10^{13} Ω cm for PI-D.

In the synthesis of an alignment layer with polyimide, it is not easy to have the materials having both low resistivity and low ion density simultaneously because of trade-off relationship between amount of ion impurity and resistivity. In other words, the layer should have some ions to lower the resistivity of PI layer, however, such ions might penetrate into LC layer, resulting in bad reliability of LCDs. Usually, the alignment layer with PAA type has both low resistivity and high ion density so that the use of it in the IPS LCD results in low image sticking and bad reliability, and on the contrary, the alignment layer with SPI type has both high resistivity and low ion density so that it results in image-sticking problem even though it shows good reliability in IPS LCDs. The reason why the SPI-type alignment layer has excellent reliability is because of their high imidisation ratio, high voltage-holding ratio (VHR) and low ion density, which gives rise to very high resistivity over 10^{15} Ω cm.

Now the question arises how we can reduce the resistivity of SPI-type alignment layer to make R-DC discharge faster while keeping high reliability characteristic. In our proposed approaches, various types of inorganic salts were doped to commercially available SPI-type PI solution (JALS-146 for homogeneous

alignment, Japan Synthetic Rubber, Japan) for lowering resistivity of PI without any changes in impurity property. To prepare proper material which should have a good solution coating property and uniform dispersion property within all PI layers, we used three kinds of inorganic salt ($MgSO_4$, KBr and NaCl). At first, 0.025 and 0.25 g of inorganic salts each were mixed separately into 1.0 g of water, and then mixed these solutions into 25 g of SPI-type PI solution. With this procedure, we could obtain perfectly clear inorganic salt doped PI solution with KBr salt, however, we could not obtain clear solution with $MgSO_4$ and NaCl because of its low solubility, as shown in Figure 5. Once KBr-doped SPI-type polyimides with 100 and 1000 ppm, and various polyimides (PI-A, PI-B, PI-C and PI-D) were prepared, VHR, ion density, residual DC or DC stability for forecasting image sticking and reliability were evaluated.

For an LC, a superflurinated LC mixture with physical properties (MAT-09-190 Merck, birefringence Δn = 0.1030 at 589 nm, dielectric anisotropy $\Delta\varepsilon$ = 7.6 at 1 kHz, resistivity 2.9×10^{14} Ω cm, 20°C) was used.

The size of IPS mode LC cell is 50 mm × 50 mm with its active area of 20 mm by 8 mm. On the bottom substrate, the come-like electrodes made of transparent indium tin oxide (ITO) in the active area have wedge shape for two domains with ±20° with respect to the vertical axis, in which one group is pixel electrode and the other is common electrode with electrode width and the distance between them of 10 μm each, as shown in Figure 6. The top substrate is just bare glass. The alignment layers were deposited on both substrates first by spin-coating of dilute solution of PIs with gamma-butyrolactone and precured at 80°C for 5 min, and then cured at 220°C for 1 h. The thickness of PI films was kept to be 100 nm. Both

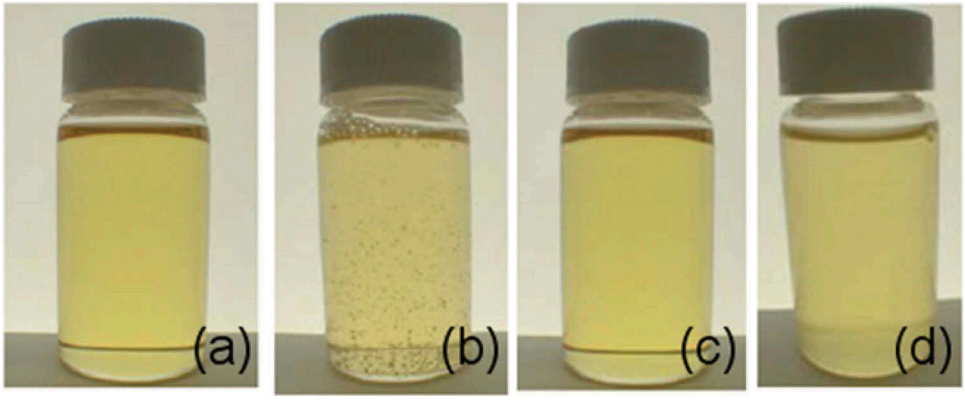

Figure 5. (colour online) Photographs of real bottle images with each mixing condition: (a) KBr 100 ppm solution: inorganic salt was clearly dissolved in solution, (b) $MgSO_4$ 100 ppm solution: almost clear solution. But lots of insoluble powder was observed at the bottom of solution, (c) KBr 1000 ppm solution: inorganic salt was clearly dissolved in solution and (d) NaCl 100 ppm solution: turbid solution.

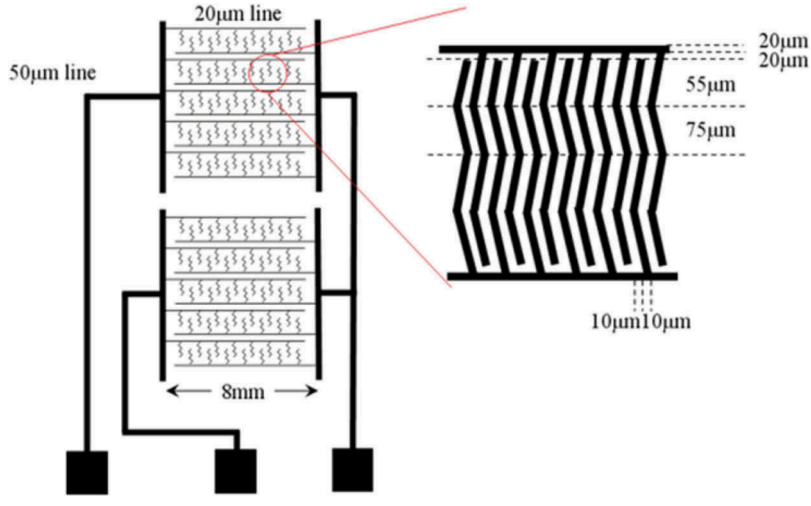

Figure 6. (colour online) Detailed IPS electrode structure for unit cells.

substrates were rubbed in anti-parallel directions. To maintain the cell gap of 3.2 μm of the LC cell, ball spacers are used.

To study a long-term reliability, VHR and ion density were measured with a measurement unit (Toyo Corporation, Model 6254) as a function of time. The VHR was measured at 100°C under 1 V with conditions of 60 μs pulse and frame period of 100 ms during 30 h, and ion density was also measured at the same condition under 10 V with 0.1 Hz pulse condition. On the other hand, to predict a DC image-sticking property, the DC discharging curves of IPS Test cells were measured at room temperature with proper luminance measurement unit (PX-03 M). First, for stabilising test cells, we apply an AC voltage (V10), which gives rise to 10% transmittance in voltage-dependent transmittance curve for 10 min with common voltage of 5 V. Then, we apply a V10 AC voltage with 1 V DC offset voltage with same common voltage for 10 min. And finally, we again apply a V10 AC voltage with 5 V common voltage for 10 min. The luminance of the test cell was measured over whole driving time range for total 30 min.

The R-DC was also measured for evaluating DC discharging characteristics by monitoring the change of the remained DC in test cells. In general, R-DC test with voltage-short method has an unusual behaviour during initial DC discharging range because of desorption force of ion impurities. In order for DC discharging rate not to be affected by a desorption force of ion impurities, R-DC test without voltage-short method was performed. The R-DC was measured during 2 h at 60°C after inducing 10 V DC voltage for 2 h by dielectric adoption method with proper measurement unit (Toyo 6254).

4. Results and discussion

At first, we attempted to clarify the correlation between resistivity of alignment layer and DC image sticking of IPS cell. DC discharging test and R-DC test were proceeded with various PIs (PI-A, PI-B, PI-C and PI-D). In general, the DC discharging test is a proper method for evaluating DC image-sticking property by monitoring the change of luminance while applying DC voltage to IPS cell. In the cell, DC charge across LC layer moves to alignment layer, following RC value in each layer and then a relative luminance is changed according to discharging level of DC voltage. It is quite obvious that the DC image sticking is less, as the DC discharging rate is fast.

In a previous work [30], it was estimated that the lower the resistivity of PI, DC discharging rate and

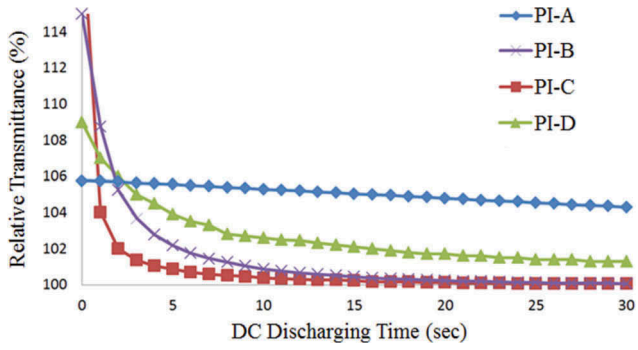

Figure 7. (colour online) DC discharging test results of each cell with different PIs: resistivity is 8.0×10^{15} Ω cm for PI-A, 9.4×10^{12} Ω cm for PI-B, 2.8×10^{12} Ω cm for PI-C and 6.3×10^{13} Ω cm for PI-D.

Table 1. Comparison of voltage-holding ratio (VHR) and ion density of three alignment layers (PI-A, PI-B and PI-D).

			VHR (%)		Ion density (pC/cm^2)	
	PI type	Resistivity (Ω cm)	Initial	After 30 h	Initial	After 30 h
PI-A	SPI	8.0×10^{15}	97.9	96.3	99.8	143.2
PI-B	PAA	9.4×10^{12}	96.3	86.2	145.6	408.5
PI-D	PAA	6.3×10^{13}	95.2	89.6	150.1	396.7

R-DC discharging rate become faster. Figure 7 and Table 1 summarised discharging behaviours of ions and as indicated, DC discharging rate and R-DC discharging rate became faster (discharging rate: PI-B ≈ PI-C >PI-D >PI-A) as the resistivity of PI became lower (resistivity: PI-B ≈ PI-C <PI-D <PI-A). The results clearly indicated that decreasing the resistivity of a PI can effectively help to reduce DC image sticking in LCD panels. In addition, SPI-type alignment layer (PI-A) has higher resistivity than PAA-type alignment layer (PI-B, PI-C and PI-D) and as a result, SPI-type alignment layer shows a bad DC image-sticking property.

We also measured VHR and ion density of all IPS cells. In general, measuring VHR and ion density at a high temperature condition is a very useful evaluation method that can predict the reliability of real IPS LCD. When VHR has a high initial value with a low decreasing rate at thermal stress condition, it indicates a good reliability feature [31–33]. On the other hand, if ion density has a low initial value with low increasing rate during thermal stress, it also indicates a good reliability feature. As summarised in Table 1, the IPS test cell made with SPI-type alignment layer (PI-A) represented a superior result in the reliability. However, other test cells made with PAA-type alignment layer (PI-B, PI-C and PI-D) showed low reliability regardless of their

Table 2. Comparison of electrical properties of alignment layers and its reliability and image-sticking properties of real in-plane switching (IPS) liquid crystal display (LCD) panels.

	Electrical properties				Panel properties	
	VHR (%) after 30 h stress	Ion density after 30 h stress	Resistivity	Residual DC decay	Image sticking	Long-term reliability
SPI type	>95%	Low	High	Slow	Bad	Good
PAA type	<90%	High	Low	Fast	Good	Bad
Ideal	>98%	Low	Low	Fast	Good	Good

resistivity. These results were also compared with the characteristics of the actual panel and we could know that the ideal alignment layer for low image sticking and high reliability must have low resistivity property with low impurities (low ion density), as shown in Table 2.

As mentioned earlier, as a solution to overcome a unique trade-off property of PI material, we prepared inorganic salt doped SPI-type alignment layers to decrease the resistivity without increasing impurities.

The measured VHR and ion density of all LC cells as a function of times are shown in Figure 8. The VHR and ion density of LC cells with KBr doped PI showed almost the same initial value and about the same decay rate compared to values of normal soluble PI test cell. From the results, we could confirm that inorganic salt doped PI system does not decrease reliability of the IPS cells, that is doping inorganic salt contents inside PI does not deteriorate electrical characteristics of the IPS cells, which was quite unexpected surprising result. A suggested modelling of this result in which inorganic salts in bulk PI does not decrease VHR and ion density of the IPS cells is that, as shown in Figure 9, the inorganic salt in alignment layer has high polarity so that they strongly interact with polar groups in PI

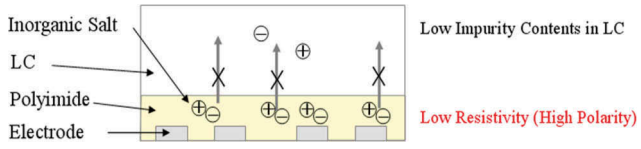

Figure 9. (colour online) Schematic modelling showing inorganic salt-doping effect in LC cell. The salt is imbedded only in PI so that the resistivity of alignment is reduced while preventing it to permeate into LC layer.

structure and thus they cannot permeate into LC layer. Conclusively speaking, the IPS LC cell with inorganic salt doped PI showed almost the same reliability as that of normal SPI-type alignment layer.

R-DC discharges of all LC cells were also measured for predicting a DC image-sticking property, as shown in Figure 10. As expected, the cell with PAA-type alignment layer showed the fastest discharging property whereas the cell with SPI-type alignment layer showed the slowest one. Interestingly, R-DC discharging property was enhanced in the cells with inorganic salt doped in PI, and also its discharging speed increased with increasing inorganic salt contents. The higher the doping amount of KBr, the discharging rate becomes faster. This result indicates

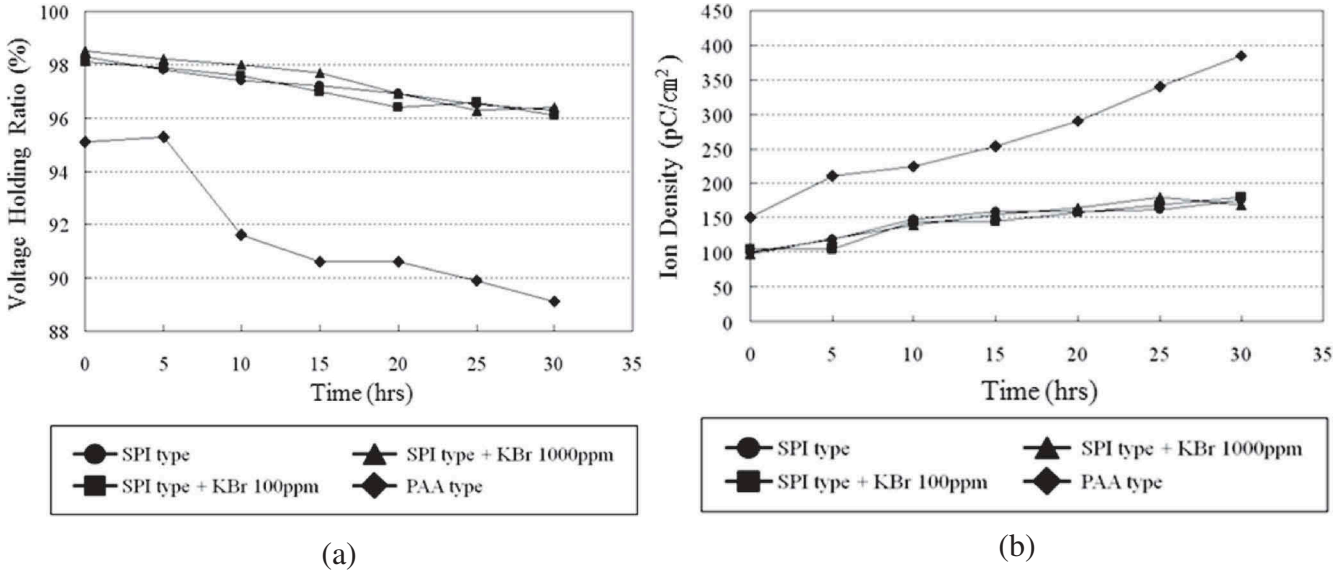

Figure 8. Measured (a) VHR and (b) ion density in each cell condition.

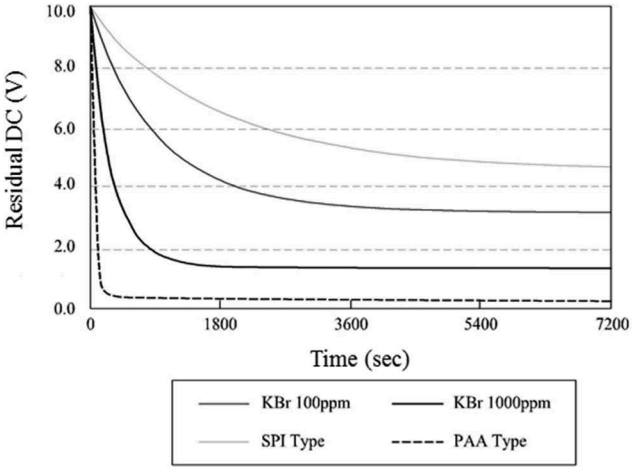

Figure 10. Fitted R-DC graph of each cell conditions.

that increasing the KBr contents can effectively help to reduce DC image sticking in LCD panels. However, for higher KBr contents, we found the solubility issue of KBr in soluble PI such that it took a very long time to get a homogenous mixture. Especially, the IPS cell with 1000 ppm KBr-doped condition exhibited almost four times faster discharging speed than that with the original SPI type and also its discharging speed is almost the same as that of the cell with PAA-type alignment layer although the discharging is more complete in the cell with PAA-type alignment layer. However, in real TFT-LCD panel, both showed almost the same discharging behaviour. The improved discharging property in the cell with inorganic salt-doping method is attributed to the decrease in effective resistivity of SPI-type alignment layer. Finally, we also analysed the electro-optic properties of ion doped LC cell to check if a surface anchoring energy changes or not. However, newly proposed ion-doped LC cell only change DC stability and VHR (%) without any electro-optical changes caused by azimuthal anchoring energy, because it just changes resistivity of alignment layer.

In summary, the results clearly show that the resistivity of PI was strongly related to the DC image-sticking property of IPS LCD panel. In addition, we could confirm that the ionic salts doping into SPI-type alignment layer results in lowering resistivity of PI material without increasing cell impurities, and the introduction of the KBr salt doping into SPI-type alignment layer can improve DC image-sticking level in IPS LC cell with good long-term reliability. With this approach, we successfully developed the new PI with low resistivity and low impurity and adopted this material to a conventional real 17 in. WXGA IPS panel with process optimisation and successfully made a new IPS LCD panel with a good image sticking and high reliability for long-term driving. As shown in Table 3, short term and long-term image sticking appeared in the panel with SPI alignment layer whereas it disappeared fast enough in the panel with PAA alignment layer. On the other hand, in long term (2000 h) driving reliability test proceeded at 60°C, uneven images in displayed area appeared in the panel with PAA alignment layer whereas it did not appear in the panel with SPI alignment layer. However, with the adoption of inorganic salt-doped SPI, not only short and long-term image sticking exhibited the same level as that with PAA alignment layer but also long-term reliability test exhibited the same level as that with SPI alignment layer.

5. Conclusions

Conventional soluble PI-type alignment layer showed excellent reliability performance in IPS LCD but it was not suitable due to serious DC image sticking, whereas PAA-type alignment showed excellent performance in DC image-sticking release but it had long-term reliability issues. In order to understand residual DC discharging behaviour, we studied its discharging characteristics in relation to electrical properties of an alignment layer, and suggested new type of alignment layer in which inorganic salt was doped into the soluble PI-type alignment layer to improve DC discharging property without increasing impurity in the panel.

With these approaches, we have successfully developed new IPS LCD for information display usage, having

Table 3. Comparison of image sticking and reliability properties of 17 in. WXGA LCD panel with ion-doping soluble polyimide (SPI)-type alignment layer.

			17 in. WXGA LCD Panel		
	Stress time with chess board sticky pattern (h)	Driving temperature	PAA type	SPI type	SPI + KBr 1000 ppm
Short-termimage sticking	1	RT	<1 min	>10 min	<1 min
Long-termimagesticking	12	RT	<1 min	>1 h	<1 min
Reliability (uneven display appearedin long-term driving)	2000	60°C	Appeared	Not appeared	Not appeared

both long-term reliability and low image-sticking level. Conclusively speaking, we could confirm that inorganic salt-doping method can reduce bulk resistivity of bulk PI layer without increasing ionic impurities in LC layer. No doubt, this new technology will simply provide the better performance for long-term driving usage of IPS LCD.

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Disclosure statement

No potential conflict of interest was reported by the authors.

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