

Ph.D Dissertation

**Linearization Techniques of RF  
Power Amplifiers Using Negative  
Group Delay Characteristics**

마이너스 군지연 특성을 이용한  
RF 전력 증폭기의 선형화 기법

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Academic Advisor: Professor Yongchae Jeong

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2011. 03. 28

**Graduate School of  
Chonbuk National University**

**Department of Electronics and  
Information Engineering**

**Heungjae Choi**

The Ph.D dissertation of Heungjae Choi  
is approved by

Chair, Professor, Hang-Geun Jeong  
Chonbuk National University

*Hanggeun Jeong*

Vice Chair, Professor, Songcheol Hong  
KAIST

*Songcheol Hong*

Professor, Dal Ahn  
Soonchunhyang University



Professor, Hae-Won Son  
Chonbuk National University

*Hae-Won, Son*

Advisor, Professor, Yongchae Jeong  
Chonbuk National University

*Yongchae Jeong*

2011. 06. 15

Graduate School of  
Chonbuk National University

*To my beloved family*

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# ABSTRACT

Heungjae Choi

Department of Electronics and Information Engineering

The Graduate School

Chonbuk National University

There are many well-known RF power amplifier linearization techniques such as the feedforward and feedback topologies, which include signal suppression loop to generate the desired error signal. The feedforward technique provides the widest cancellation bandwidth with excellent linearization performance in expanse of complexity and efficiency degradation. Especially, the insertion loss from the main path delay element takes great part in the overall efficiency degradation. The distortion feedback topology is also a good candidate for linearizing nonlinear power amplifier. However, the cancellation bandwidth of only up to a few MHz could be obtained due to the time delay mismatching issue of the feedback loop.

Unfortunately, those two issues have been left unsolved for a long time because they result from their own structure, not from the imperfection of the device in use. Especially, the latter problem has caused the feedback to remain as little more than an academic curiosity.

I have solved the group delay issues by introducing the time advance lookalike property of the negative group delay circuits into the signal suppression loop. From the prototype design and measurement, two issues as 1) to remove the main path delay in a feedforward amplifier and achieve the efficiency enhancement, and 2) to provide the perfect group delay matching in the feedback amplifier to enhance the cancellation bandwidth, have been validated. In case of the feedforward amplifier, the highest efficiency of 19.5 % can be achieved while satisfying the commercial specification. In case of the feedback amplifier, the widest cancellation bandwidth of over 50 MHz can be achieved.

**Keywords:** feedback, feedforward, negative group delay, power amplifier.

# ABSTRACT IN KOREAN

## 요약

일반적으로 널리 사용되는 RF 전력 증폭기의 선형화 기법으로 피드포워드, 피드백 구조를 들 수 있으며, 이 기법들은 원하는 오차 신호를 생성하는 신호 상쇄 루프를 포함하고 있다. 피드포워드 기법은 가장 뛰어난 선형화 대역폭과 선형성 개선 특성을 가지고 있음에도 불구하고 상대적으로 회로가 복잡해지고 효율이 감소된다는 단점을 가지고 있다. 특히 이러한 효율 저하에 있어서 주 전력 증폭기 출력 단에 존재하는 지연 선로의 삽입 손실이 큰 비중을 차지한다. 또 다른 선형화 방식으로 피드백을 들 수 있다. 그러나 피드백 루프에서 발생하는 군지연 시간 부정합 문제 때문에, 기껏해야 수 MHz 의 상쇄 대역폭만을 얻는 치명적인 단점이 있다.

불운하게도, 군지연 정합에 관하여 발생하는 이 두 가지 문제점은 오랜 시간 동안 해결되지 못하고 있다. 그 이유는 이러한 문제점이 선형화 기법에 사용되는 소자들의 불완전성에 의해 발생하는 것이 아니라 선형화 기법 자체가 갖는 구조적인 문제점이기 때문이다. 특히, RF 피드백 기법은 실질적인 연구가 거의 이루어지지 않고 있다.

본 논문에서는 시간 선행의 특성을 갖는 마이너스 군지연 회로를 신호 상쇄 루프에 도입함으로써 이러한 군지연 정합에 관한 문제를 해결하고자 하였다. 설계 및 실험 결과로써, 1) 피드포워드 기법에서 전력 증폭기 출력 단에 존재하는 지연 선로의 제거를 통해 효율을 증대시켰으며, 2) 피드백 구조에서 완벽한 군지연 정합 조건을 만족시킴으로써 대역폭을 확장할 수 있음을 보였다. 피드포워드 증폭기의 경우 상용 기지국의 출력 전력 및 선형성 규격을 만족시키며 19.5 %의 효율을 얻었으며, 피드백 증폭기의 경우 50 MHz 이상의 선형화 대역폭을 얻을 수 있었다.

**주요어:** 마이너스 군지연, 피드포워드, 피드백, 전력 증폭기

# ABBREVIATIONS

ACLR	adjacent channel leakage ratio
ADS	advanced design system
AM-AM	amplitude to amplitude distortion
AM-PM	amplitude to phase distortion
BJT	bipolar junction transistor
BPF	band pass filter
CDMA	code division multiple access
CMOS	complementary metal oxide silicon
CPL	coupler
CRLH	composite right/left handed
CW	continuous wave
DGS	defected ground structure
DPD	digital predistortion
DSP	digital signal processor
DE	distributed element
EPA	error power amplifier
FA	frequency allocation
FB	feedback
FET	field effect transistor

FFW	feedforward
GaN	gallium nitride
GD	group delay
HEMT	high electron mobility transistor
HF	high frequency
HFSS	high frequency structure simulator
HO	half-wave open
HPA	high power amplifier
HS	half-wave short
IMD	intermodulation distortion
LE	lumped element
LDMOS	laterally diffused metal oxide silicon
LH	left-handed
LTCC	low temperature co-fired ceramic
MPA	main power amplifier
NGD	negative group delay
NGDC	negative group delay circuit
OFDM	orthogonal frequency division multiplexing
PA	power amplifier
PAE	power added efficiency

PAPR	peak to average power ratio
PD	predistortion
QO	quarter-wave open
QS	quarter-wave short
RF	radio frequency
RH	right-handed
RP	reflective parallel
RS	reflective series
SLR	stepped impedance resonator
SP	series parallel
SS	shunt series
TL	transmission line
TLR	transmission line resonator
VHF	very high frequency
VM	vector modulator
WCDMA	wideband code division multiple access
WiMAX	world-wide interoperability for microwave access



# CHAPTER 1

## INTRODUCTION

### *1.1 The Need for Highly Efficient and Linear RF Power Amplifiers*

Power amplifiers (PAs) are essential components in a communication system and are inherently nonlinear. The nonlinearity generates spectral regrowth, which leads to adjacent channel interference and violations of the out-of-band emission requirements [1]-[4].

Since its first introduction by Black [5][6] and the experiment by Seidel [7], the feedforward amplifier system has played a leading role for linear transmitters, especially in the base-station applications used in a modern wireless communication environment. In addition to the feedforward method, there are various linearization techniques, including analog predistortion, digital predistortion, and by direct or indirect feedback, such as in a polar method or in a Cartesian loop. Digital predistortion (DPD) can provide good linearity at the digital domain, but this results in very complicated algorithm, limited bandwidth, and expensive solution. Nevertheless, the feedforward technique has become a preferred technique and is well known for its broad bandwidth capability, good linearization performance, and its stable

operation. This is due to the fact that it operates by the utilization of forward loops. However, poor system efficiency is the critical disadvantage of the feedforward amplifier.

Extensive researches on the analysis and design of the feedforward amplifier system have been performed. Potheary [3], Kenington [4] and other researchers [8]-[10] have analyzed the effects of amplitude, out-of-phase, and group delay (GD) mismatches on the suppression and efficiency performance of these amplifiers. Andrenko *et al.* [11] and also Larose and Ghannouchi [12][13] have proposed efficiency optimizations of the feedforward amplifier. As a system model, Rummery *et al.* [14] have proposed the first order closed form equation for the feedforward design constraints and sensitivity analysis. Jeong *et al.* [15] have proposed an equal group-delay signal canceller to improve the inherent bandwidth limitation of the signal subtraction circuit by using an in-phase combiner/divider with a  $180^\circ$  phase difference. Hau *et al.* [16] have proposed a phase equalizer to reduce the nonlinear phase imbalances within the suppression loops. Braithwaite [17] has described a novel pilot generation and detection system for an adaptive feedforward amplifier. Choi *et al.* [18] expanded the feedforward amplifier to a dual-band operation, and also proposed the cross cancellation technique for the

feedforward amplifier [19], used as a linearity enhancement technique for a balanced power amplifier.

Major sources of efficiency degradation for the feedforward amplifier are found in the error power amplifier (EPA) employed at the distortion suppression loop and passive components connected at the output of the main power amplifier (MPA), especially the insertion loss of a delay element [20]-[24]. The delay element is unavoidable and essential to the broadband signal suppression loop design as long as there is a propagation time for the EPA, and the accompanying adjustable devices required for loop balancing.

In addition to the feedforward method, Seidel also introduced a feedback amplifier [25][26], which utilizes the MPA and EPA with three signal coupling devices used to degenerate the error signal generated by the MPA by introducing a feedback loop. McRory *et al.* [27] mathematically analyzed the same structure based on the Volterra series. Kim *et al.* [28] proposed a modified version of the feedback topology and named the circuit ‘feedback predistortion’. Qiang *et al.* [29] also analyzed the structure introduced by Seidel based on power series expansion. There are notable advantages in the feedback amplifier when compared to the feedforward amplifier: 1) the EPA requires lower output power since the error signal is injected to the input of the MPA, and 2) the RF output loss is smaller because there is no lossy

group delay element at the output of the MPA. Regardless of all these advantages, an extremely narrow operating bandwidth, which is only capable of covering a few megahertz, was the key limiting factor that discouraged the utilization of the feedback topology [30][31]. This is especially true in the recent wireless communication environment, which utilizes several digital modulation schemes involving modulated signals with a broad bandwidth, such as wideband code division multiple access (WCDMA) and worldwide interoperability for microwave access (WiMAX). This limited bandwidth of feedback amplifier originates from the group delay mismatching generated in the feedback loop by the feedback transmission time. In the conventional researches the minimum feedback time is assumed, but in a practical situation the assumption is not valid because of the transmission time of the MPA, EPA, and other signal adjusting devices including the band-pass filter.

Recently, interesting experimental validation on the negative group delay (NGD) concept has been reported, and its electronic circuit application has been proposed [32]-[59]. The NGD concept is quite intriguing, and sometimes confusing, in that typical materials under normal conditions do not usually behave in a manner consistent with the observed behaviors [32]. In a specific frequency band of an anomalous dispersion, the group velocity is observed to be greater than that of  $c$ , the speed of light in vacuum, or even a negative

value [33]. This phenomenon was defined as the superluminal group velocity [34]. A number of researchers were involved in the experimental study of the superluminal group velocity [35]-[43]. Researchers have investigated on the design [44] and application [45]-[50] of NGD to various electronic circuits. In [46]-[49], various applications of the NGD circuits with an active topology have been proposed such as on the baseband propagation delay reduction [48] and broadband and constant phase shifters [49]. In [50], a trial to design a passive NGD circuit for the feedforward power amplifier application was reported. However, the previous work was not suitable for a commercial LPA system amplifying broadband modulated signals, such as the WCDMA signals in which the signal bandwidth is roughly 5 MHz. This is due to a narrow signal bandwidth (2 MHz of two-tone spacing), poor input/output reflection coefficients, design inaccuracy induced by the limited availability of lumped elements, and the fact that there was no intuitive general NGD circuit design equation. Considering the inter-modulation distortion (IMD) signal, the cancellation bandwidth requirements would be much harder to satisfy in practical applications.

This paper presents novel topologies of the feedforward amplifier without the main path delay element, and the feedback amplifier with considerably enhanced cancellation bandwidth, by employing a distributed element NGD

circuit. The major benefit that can be achieved with the proposed feedforward topology is an efficiency enhancement accomplished by eliminating the delay element at the output of the MPA, one of the major sources of efficiency degradation, without affecting the linearization performance. The major benefit that can be achieved with the proposed feedback topology is a bandwidth enhancement accomplished by providing group delay matching at the feedback loop, without affecting the linearization performance.

## ***1.2 Dissertation Focus and Organization***

The rest of this dissertation is organized as follows. Chapter 2 briefly describes the fundamental principle of RF PA linearization techniques. Main techniques to be discussed are the predistortion, the feedforward, and the feedback. The advantages and practical limitation of each approach will be discussed, especially regarding the efficiency issues in the feedforward and bandwidth issues in the feedback.

Chapter 3 describes the NGD concept, research history and mathematical analysis as well as the practical applicability. Based on the research literatures, causality issues related to the NGD concept are discussed. Then, four types of basic lumped element resonant circuit are analyzed to find the

condition to generate the NGD. For practical design, circuit conversion method from the lumped element to the distributed element is explained. NGD circuit based on the balanced and reflection topologies are proposed. In addition, the time advance property is experimentally validated by using an arbitrary time domain waveform.

Chapter 4 is devoted to the practical application of the NGD characteristics to the performance improvement of RF PA linearization technique. Discussion begins with the design and measurement of high efficiency PAs to be used as a nonlinear main PA and linear error PA. And the principle of operation of the feedforward amplifier employing the NGD circuit is explained. Loop suppression analysis is given to highlight the significance of the group delay matching in RF linearization technique. The effect of NGD circuit on the efficiency performance of the feedforward amplifier is discussed through various experimental results. In the next subsection, NGD is applied to the feedback technique to enhance the bandwidth performance. Linearization bandwidth of the proposed feedback topology employing the NGD circuit is considerably increased when compared to the previous results. Finally, Chapter 5 summarizes the contributions of the dissertation and provides ideas for future research in this area.

## CHAPTER 2

# OVERVIEW OF KEY RF POWER AMPLIFIER LINEARIZATION TECHNIQUES

In this chapter, the fundamental principle and the problems related to the representative RF PA linearization techniques such as predistortion, feedforward and feedback will be briefly discussed.

### *2.1 Predistortion*

Fig. 2.1 shows the schematic of an RF amplifier and predistorter [1]-[4]. The basic concept of a predistortion system involves the insertion of a nonlinear element prior to the RF PA such that the combined transfer characteristic of both is linear, as shown in Fig. 2.2. The predistortion can be accomplished at either RF or baseband.

The block diagram of a simple RF predistorter is shown in Fig. 2.3. A comprehensive characteristic, created by the nonlinearity in the lower path is subtracted from a linear characteristic to generate an expansive characteristic. Predistortion bandwidths tend to be limited by similar factors to that of feedforward, namely gain and phase flatness of the predistorter itself and of the RF PA. In addition, memory effects in the PA and the predistorter limit



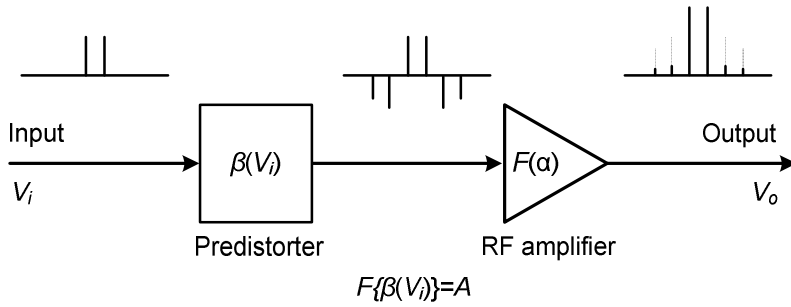


Figure 2.1: Schematic of RF amplifier and predistorter.

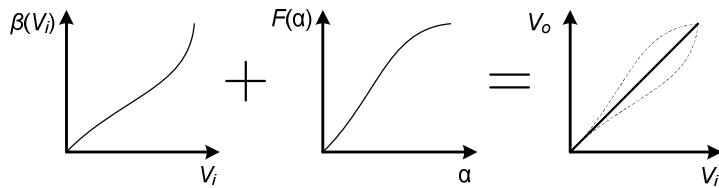


Figure 2.2: Operation of a predistortion linearizer.

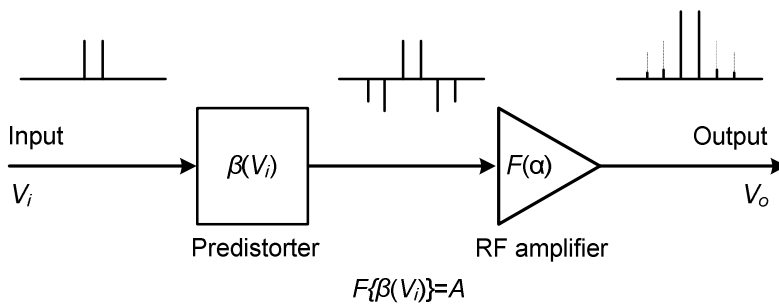


Figure 2.3: Schematic of a Cubic RF predistorter.

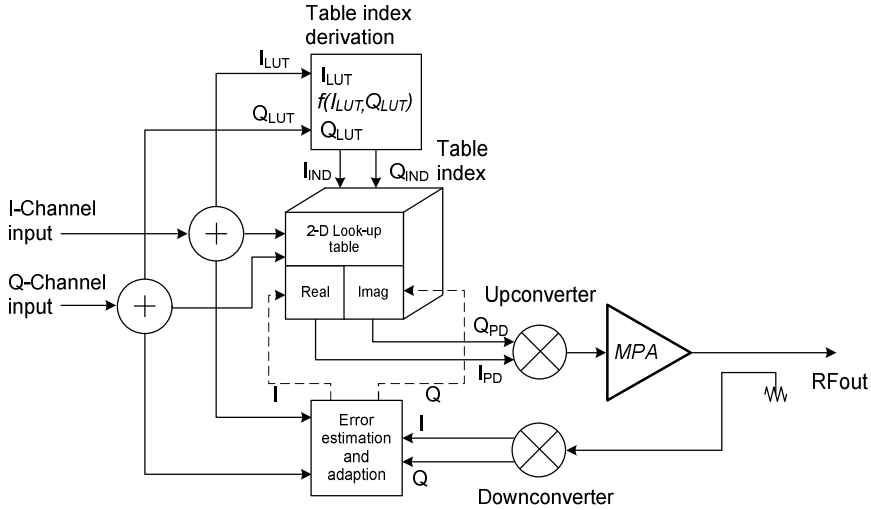


Figure 2.4: Baseband mapping digital predistorter.

the degree of cancellation, and these tend to become poorer with increasing bandwidth.

Digital predistortion techniques exploit the considerable processing power now available from DSP devices, which allows them both to form and to update the required predistortion characteristic [1]. They can operate with analog-baseband, digital-baseband, analog-IF, digital-IF, or analog-RF input signals. Digital-baseband and digital-IF processing are most common. The two most common types of digital predistorter are termed mapping predistorters. A mapping predistorter utilizes two look-up tables, each of which is a function of two variables ( $I_{IN}$  and  $Q_{IN}$ ), as shown in Fig. 2.4. This type of predistorter is capable of excellent performance. However, it requires

a significant storage and/or processing overhead for the look-up tables and their updating mechanism, and has a low speed of convergence. The low convergence speed results from the need to address all points in the I/Q complex plane before convergence can be completed.

## ***2.2 Feedforward***

### **2.2.1 Basics of Feedforward Linearization**

The very wide bandwidths (10 to 100 MHz) required in multicarrier applications can render feedback and DSP impractical. In such cases, the feedforward technique can be used to achieve ultra-linear operation. In its basic configuration, the feedforward typically gives improvements in distortion ranging from 20 to 40 dB.

In its basic form (Fig. 2.5), the feedforward amplifier consists of two amplifiers (the MPA and EPA), directional couplers, delay lines and loop control networks [4]. The directional couplers are used for power splitting/combining, and the delay lines ensure the operation over a wide bandwidth. Loop-control networks, which consist of amplitude- and phase-shifting networks, maintain the signal and distortion cancellation within the various feedforward loops.

The input signal is first split into two paths, with one path going to the high-power MPA while the other signal path goes to a delay element. The output signal from the MPA contains both the desired signal and distortion. These signals are sampled and scaled using attenuators before being combined with the delayed portion of the input signal, which is regarded as distortion-free. The resulting “error signal” ideally contains only the distortion components in the output of the MPA. The error signal is then amplified by the low-power, high-linearity EPA, and then combined with a delayed version of the MPA output. This second combination ideally cancels the distortion components in the MPA output while leaving the desired signal unaltered. In practice, there is always some residual desired carrier signal passing through the EPA. This is in general not a problem unless the additional power is sufficient in magnitude to degrade the linearity of the EPA and hence the linearity of the feedforward transmitter.

Successful isolation of an error signal and the removal of distortion components depend upon precise signal cancellation over a band of frequencies. In practice, cancellation is achieved by the vector addition of signal voltages.

The allowable amplitude and phase mismatches for different signal suppression levels are shown in Fig. 2.6. For manufactured equipment,

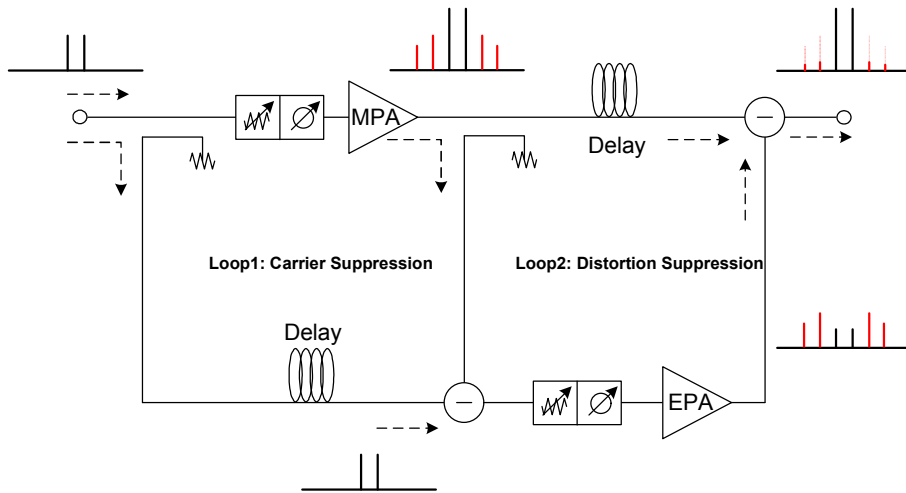


Figure 2.5: Feedforward transmitter in its basic form.

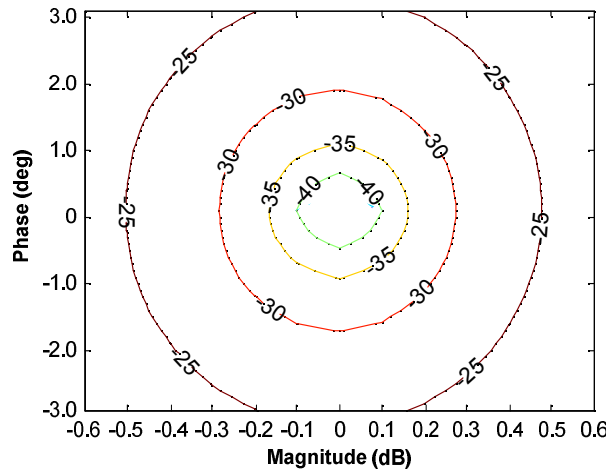


Figure 2.6: Gain and phase matching requirements for signal suppression.

realistic values of distortion cancellation are around 25 to 30 dB. The limiting factor is nearly always the bandwidth over which a given accuracy can be obtained.

The outputs of the MPA and EPAs are typically combined in a directional coupler that both isolates the PAs from each other and provides resistive input impedances. For a typical 10 dB coupling ratio, 90 percent of the power from the MPA reaches the output. For the same coupling ratio, only 10 percent of the power from the EPA reaches the load, thus the EPA must produce ten times the power of the distortion in the MPA. The peak-to-average ratio of the error signal is often much higher than that of the desired signal, making amplification of the error signal inherently much less efficient than that of the main signal. As a result, the power consumed by the EPA can be a significant fraction (e.g., one third) of that of the MPA. In addition, it may be necessary to operate one or both amplifiers well into back-off to improve linearity. The overall average efficiency of a feedforward transmitter may therefore be only around 10 percent for typical multicarrier signals.

### 2.2.2 Recent Literatures

Since its first introduction by Black [5][6] and the experiment by Seidel [7], the feedforward amplifier system has played a leading role for linear

transmitters, especially in the base-station applications used in a modern wireless communication environment.

Extensive researches on the analysis and design of the feedforward amplifier system have been performed. Potheary [3], Kenington [4] and other researchers [8]-[10] have analyzed the effects of amplitude, out-of-phase, and group delay (GD) mismatches on the suppression and efficiency performance of these amplifiers. Andrenko *et al.* [11] and also Larose and Ghannouchi [12][13] have proposed efficiency optimizations of the feedforward amplifier. As a system model, Rummery *et al.* [14] have proposed the first order closed form equation for the feedforward design constraints and sensitivity analysis. Jeong *et al.* [15] have proposed an equal group-delay signal canceller to improve the inherent bandwidth limitation of the signal subtraction circuit by using an in-phase combiner/divider with a  $180^\circ$  phase difference. Hau *et al.* [16] have proposed a phase equalizer to reduce the nonlinear phase imbalances within the suppression loops. Braithwaite [17] has described a novel pilot generation and detection system for an adaptive feedforward amplifier. Choi *et al.* [18] expanded the feedforward amplifier to a dual-band operation, and also proposed the cross cancellation technique for the feedforward amplifier [19], used as a linearity enhancement technique for a balanced power amplifier.

Major sources of efficiency degradation for the feedforward amplifier are found in the error power amplifier (EPA) employed at the distortion suppression loop and passive components connected at the output of the main power amplifier (MPA), especially the insertion loss of a delay element [20]-[24]. The delay element is unavoidable and essential to the broadband signal suppression loop design as long as there is a propagation time for the EPA, and the accompanying adjustable devices required for loop balancing.

### 2.2.3 Practical Limitation

As already discussed in the previous sections, the major sources of efficiency degradation for the feedforward amplifier are the DC power consumption of the EPA employed at the distortion suppression loop and the insertion loss of the passive components (DELAY 2) connected at the output of the MPA, as shown in Fig. 2.7 (a). The other example, Fig. 2.7 (b), shows the PA linearized by the cross cancellation technique [19]. In this case, there is also a delay element (DELAY 3) at the output of  $MPA_{1C}$  to compensate for the group delay due to  $EPA_C$ .

It is evident that the loss in the main-path delay element can be a significant factor in determining the overall power efficiency of a feedforward system. Therefore, the loss in this element should be kept to a minimum, in

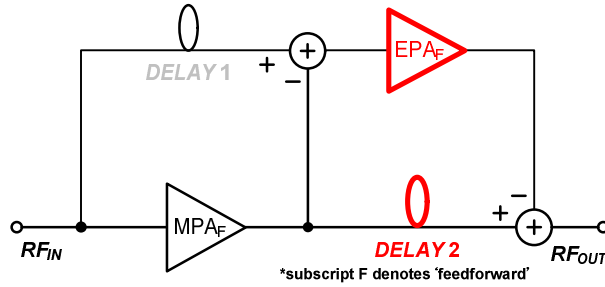


order to provide maximum efficiency and in order to minimize the power rating required for the MPA.

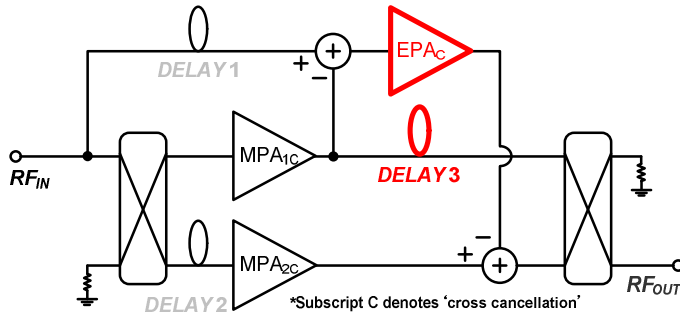
There are two methods by which this aim may be achieved [4]:

- 1) Utilize ultra low-loss coaxial cable. However, the use of high-power, low-loss cables results in an inevitable size penalty, as such cables tend to be very thick and occupy large area. A further problem is that of cost.
- 2) Reduce (or eliminate) the main-path delay element and consequently its loss. The reduction or elimination of the main path delay element will consequently reduce the size, weight and cost of a feedforward system. It will also make the system easier to integrate, making the technique potentially applicable for mobile equipment. It will also improve the overall power efficiency.

By carefully defining the class of operation, the power capacity ratio of the MPA to EPA, and the desired amount of IMD suppression, the DC power consumption and efficiency can be optimized. However, the delay element is unavoidable and essential to achieve broadband signal suppression as long as there is a propagation time for the EPA and the accompanying adjustable devices, such as the vector modulators required for loop balancing. By minimizing or eliminating the delay of the EPA path, the insertion loss of the



(a)



(b)

Figure 2.7: Block diagrams of: (a) typical feedforward power amplifier and (b) cross cancellation technique.

delay element can be minimized. As a result, the desired efficiency enhanced feedforward PA can be realized.

## 2.3 Feedback

### 2.3.1 Basics of Feedback Linearization

Feedback linearization can be applied either directly around the RF amplifier (RF feedback) or indirectly upon the modulation (envelope/phase, or I/Q components) [1]-[4], [25]-[34].

The basis of this technique is similar to its audio-frequency counterpart [1]. A portion of the RF-output signal from the amplifier is fed back to, and subtracted from, the RF-input signal without a detection or down-conversion. Considerable care must be taken when using the feedback at RF as the delays involved must be small to ensure stability. In addition, the loss of gain at RF is generally a more significant sacrifice than it is at audio frequencies. For these reasons, the use of RF feedback in discrete circuits is usually restricted to HF and lower VHF frequencies. It can be applied within MMIC devices, however, well into the microwave region. In an active RF feedback system, the voltage divider of a conventional passive-feedback system is replaced by an active (amplifier) stage. The gain in the feedback path reduces the power dissipated in the feedback components. While such systems demonstrate IMD reduction, they tend to work best at a specific signal level.

Another attempt to overcome the shortcomings of the conventional feedback when applied to RF amplifiers, in this case by cancelling the fundamental frequency components forms the fed-back signal in a manner akin to that used in a feedforward system. Thus only the nonlinear distortion components remain in the fed-back signal, hence providing an improvement in nonlinear distortion performance of the overall amplifier. However, no

improvement in linear distortion such as gain or phase performance with frequency is achieved.

A block diagram of the distortion feedback approach is shown in Fig. 2.8. It suffers from many of the inherent problems of the feedforward technique, since its performance is dependent to some extent on the quality of a cancellation process [1].

Only modest improvements in linearity have been achieved to date by using this technique. Gajda and Douville report a reduction in the third order IMD level of 6 dB when applying the technique to an amplifier at 300 MHz with a 10 MHz bandwidth. Significantly better performance would be necessary to justify the complexity involved in any sort of control technique to be used in conjunction with this type of amplifier [1].

The problem of delay in RF feedback is alleviated to a large extent by utilizing the signal envelope as the feedback parameter [4]. This approach takes care of in-band distortion products associated with amplitude nonlinearity. Harmonic distortion products, which are corrected by RF feedback, are generally not an issue as they can easily be removed by filtering in most applications. Envelope feedback is therefore a popular and simple technique. Envelope feedback can be applied a single PA (Fig. 2.9). The principles of operation are similar and both are described in detail in [4]. The

RF input signal is sampled by an input coupler and the envelope of the input sample is detected. The resulting envelope is then fed to one input of a differential amplifier, which subtracts it from a similarly obtained sample of the RF output. The difference signal, representing the error between the input and output envelopes, is used to drive a modulator in the main RF path. This modulator modifies the envelope of the RF signal which drives the RF PA. The envelope of the resulting output signal is therefore linearized to a degree determined by the loop gain of the feedback process.

The degree of linearity improvement that can be obtained when using this technique depends upon the relative levels of the AM-AM and AM-PM conversion in the amplifier. For a VHF BJT amplifier, AM-AM distortion is dominant and two-tone IMD is typically reduced by 10 dB. Since AM-PM distortion is not corrected by envelope feedback, no linearity improvement is observed if the phase distortion is the dominant form of nonlinearity. This is often the case in, for example, Class-C and LDMOS PAs. The use of the envelope feedback is therefore generally restricted to relatively linear Class-A or AB amplifiers.

The Cartesian-feedback technique overcomes the problems associated with the wide bandwidth of the signal phase by applying modulation feedback in I and Q (Cartesian) components. Since I and Q components are the natural

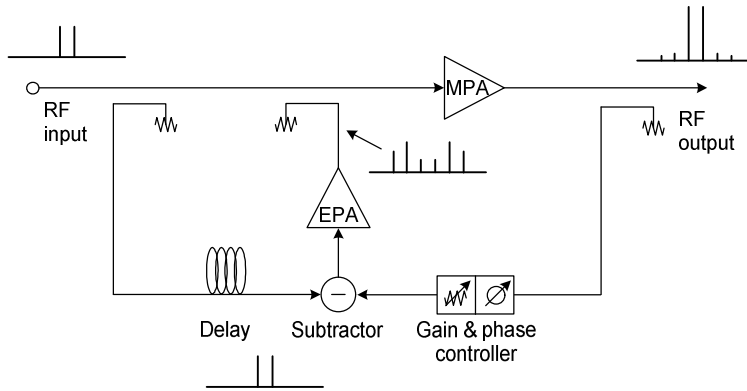


Figure 2.8: Block diagram of the distortion feedback amplifier.

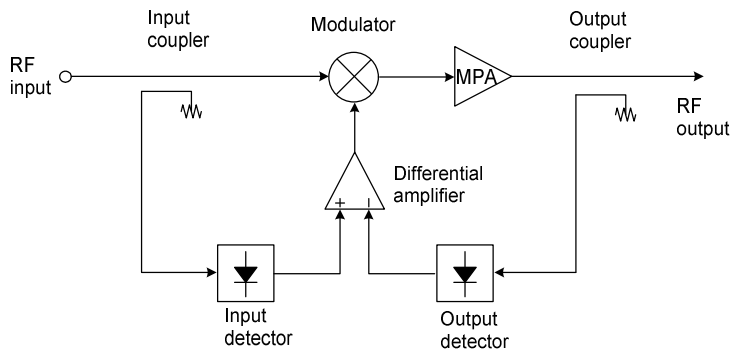


Figure 2.9: Envelope feedback linear transmitter structure.

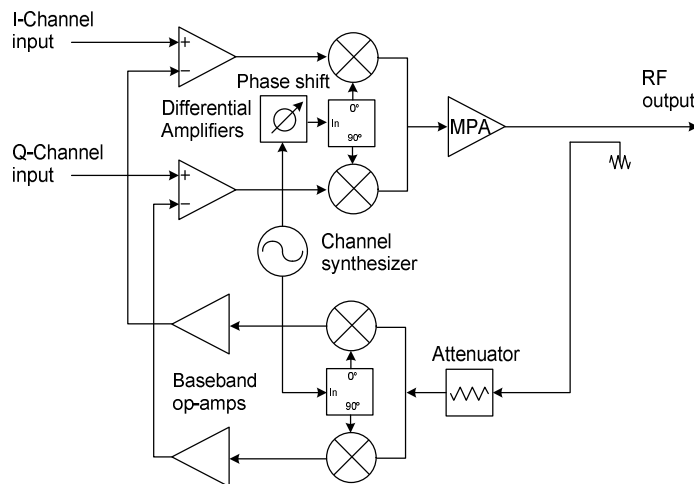


Figure 2.10: Transmitter structure employing Cartesian-loop feedback.

outputs of a modern DSP, the Cartesian loop is widely used in private mobile radio and specialized mobile radio systems. The basic Cartesian loop (Fig. 2.10) consists of two identical feedback processes operating independently on the I and Q channels. The inputs are applied to differential integrators (in the case of a first-order loop) with the resulting difference (error) signals being modulated onto I and Q subcarriers and up-converted to drive the PA. A sample of the output from the PA is attenuated and quadrature-down-converted (synchronously with the up-conversion process). The resulting quadrature feedback signals then form the second inputs to the input differential integrators, completing the two feedback loops. The phase shifter shown in the up-converter local-oscillator path is used to align the phases of the up- and down-conversion processes, thereby ensuring that a negative feedback system is created and that the phase margin of the system is optimized.

### **2.3.2 Recent Literatures on the Distortion Feedback Technique**

PAs are essential components in a communication system and are inherently nonlinear. The nonlinearity generates spectral regrowth, which leads to adjacent channel interference and violations of the out-of-band emission requirements. Digital predistortion (DPD) can provide good linearity at the

digital domain, but this results in very complicated algorithm, limited bandwidth, and expensive solution. Since its introduction by Black and the experiment by Seidel, the feedforward amplifier system has played a leading role in linear transmitters, especially in the base-station applications used in a modern wireless communication environment. The feedforward linearization is well known for its broad bandwidth capability, good linearization performance, and its stable operation. However, the poor system efficiency is the critical disadvantage of the feedforward amplifier.

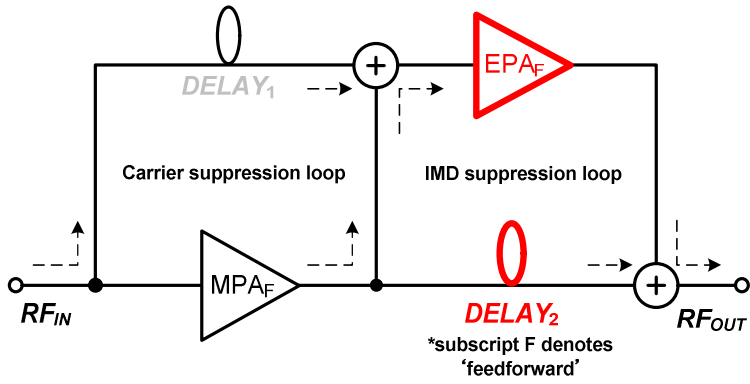
In addition to the feedforward method, Seidel also introduced a feedback amplifier [25][26], which utilizes the MPA and EPA with three signal coupling devices used to degenerate the error signal generated by the MPA by introducing a feedback loop. McRory *et al.* [27] mathematically analyzed the same structure based on the Volterra series. Kim *et al.* [28] proposed a modified version of the feedback topology and named the circuit ‘feedback predistortion’. Qiang *et al.* [29] also analyzed the structure introduced by Seidel based on power series expansion. There are notable advantages in the feedback amplifier when compared to the feedforward amplifier: 1) the EPA requires lower output power since the error signal is injected to the input of the MPA, and 2) the RF output loss is smaller because there is no lossy group delay element at the output of the MPA. Regardless of all these



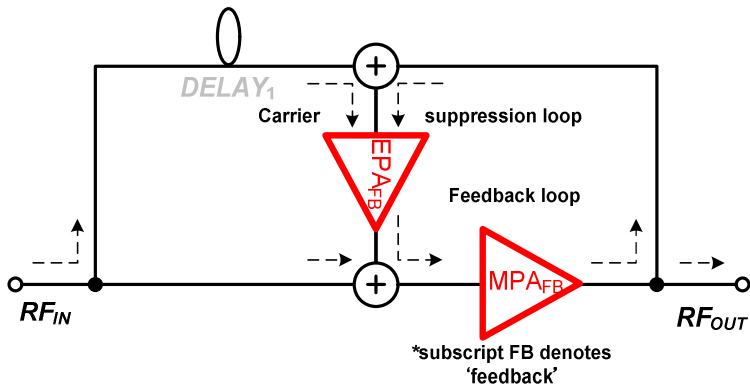
advantages, an extremely narrow operating bandwidth, which is only capable of covering a few megahertz, was the key limiting factor that discouraged the utilization of the feedback topology [30][31]. This is especially true in the recent wireless communication environment, which utilizes several digital modulation schemes involving modulated signals with a broad bandwidth, such as wideband code division multiple access (WCDMA) and worldwide interoperability for microwave access (WiMAX). This limited bandwidth of feedback amplifier originates from the group delay mismatching generated in the feedback loop by the feedback transmission time. In the conventional researches the minimum feedback time is assumed, but in a practical situation the assumption is not valid because of the transmission time of the MPA, EPA, and other signal adjusting devices including the band-pass filter.

### 2.3.3 Practical Limitation

Fig. 2.11 shows the feedforward and feedback architectures introduced by Seidel. Due to the forward loops as shown in Fig. 2.11 (a), the feedforward structure is unconditionally stable. Fig. 2.11 (b) shows the feedback amplifier structure. The RF output power loss is smaller than the feedforward structure since there is no group delay component at the output of the  $\text{MPA}_{\text{FB}}$ . In addition, the required power capability for the  $\text{EPA}_{\text{FB}}$  is smaller in



(a)



(b)

Figure 2.11: Comparison of the typical feedforward and feedback structures: (a) the feedforward amplifier and (b) the feedback amplifier.

the feedback structure because the error signal is injected into the input port of the  $MPA_{FB}$ , while the error signal in the feedforward structure is injected into the output port of the  $MPA_F$  which requires a higher power level, therefore degrading the system efficiency. Typically a band-pass filter must be utilized in the feedback loop to prevent a unwanted oscillation. Although in-band oscillation is suppressed by the negative feedback loop, out of band oscillation is possible when a positive feedback occurs.

According to Seidel's statement, however, the error-correcting technique, known as the feedback, attempts a causal contradiction: after an event has occurred, the feedback attempts to reshape the cause. Although he assumed the event would be slow enough and the feedback action fast enough, the group delay is unavoidable as long as there is a propagation time for the  $MPA_{FB}$ , the  $EPA_{FB}$  and the accompanying adjustable devices required for a loop balancing. Due to the group delay mismatch, the cancellation bandwidth of the feedback amplifier has been limited to a very narrow bandwidth, discouraging the use of this technique in the modern broadband wireless communications. This is discussed in more detail in the following subsection.

## ***2.4 Summary and Discussion***

Due to the nonlinear transfer function of an RF transistor, linearization technique is necessary to reduce the nonlinear distortion components. Key RF PA linearization techniques including predistortion, feedforward, and feedback topologies have been discussed. Among them, the feedforward technique provides wide cancellation bandwidth with excellent linearization performance in expense of complexity and efficiency degradation. Especially, the insertion loss from the main path delay element takes great part in the overall efficiency degradation. The distortion feedback topology is also a good

candidate for linearizing nonlinear PA in a transmitter if the time delay matching issue regarding the feedback loop can be solved. Unfortunately, those two issues have been left unsolved for a long time, up to date. It is because every electronic circuit involves its own propagation delay for a signal to be transmitted.

After the introduction of the NGD concept, a zero propagation time system that combines the NGD circuit and the conventional delay circuit has become an actual and achievable characteristic for RF and microwave circuits. The physical nature, causality issues, and electric circuit approach that apply to the NGD have been already analyzed and proved with experimental observations. By adopting the NGD concept, the delay element required for the signal suppression loop which is known to be the major source of efficiency degradation and bandwidth limitation can be totally eliminated, resulting in the efficiency and bandwidth enhancement of the PA linearization techniques. Detail explanation of the NGD will be discussed in the next chapter.

# CHAPTER 3

## THE NEGATIVE GROUP DELAY CHARACTERISTICS

In this chapter, the negative group delay concept, methods to obtain the NGD and experimental verification procedure will be discussed [51]-[58].

### *3.1 What is the Negative Group Delay?*

Recent optical experiments at Princeton NEC [34] have verified the prediction by the one of the authors and his co-workers that superluminal pulse propagation can occur in transparent media with optical gain [32]-[35]. These experiments have shown that a laser pulse can propagate with little distortion in an optically pumped cesium vapor cell with a group velocity greatly exceeding the vacuum speed of light  $c$ . In fact, the group velocity for the laser pulse in this experiment was observed to be negative: The peak of the output laser pulse left the output face of the cell before the peak of the input laser pulse entered the input face of the cell. This pulse sequence is counter-intuitive.

The earliest experiment to demonstrate the existence of faster-than- $c$  group velocities was performed by Chu and Wong at Bell Labs. They showed that

pico-second laser pulses propagated superluminally through an absorbing medium in the region of anomalous dispersion inside the optical absorption line [35]. This experiment was reproduced in the millimeter range of the electromagnetic spectrum by Segard and Macke [36]. These experiments verified the prediction of Garrett and McCumber [37] that Gaussian-shaped pulses of electromagnetic radiation could propagate with faster-than- $c$  group velocities in the regions of anomalous dispersion associated with an absorption line. The negative group velocities were also observed to occur in these early experiments.

These counter-intuitive pulse sequences were also seen to occur in experiments on electronic circuits [38]. In the first of these experiments, an electronic circuit was used, which consists of an operational amplifier with a negative feedback circuit containing a passive  $RLC$  network. This circuit produced the NGD similar to that observed in the optical experiment performed at Princeton NEC: The peak of the output voltage pulse left the output port of the circuit before the peak of the input voltage pulse entered the input port of the circuit. Such a seemingly anti-causal phenomenon does not in fact violate the principle of causality, since there is sufficient information in the early portion of any analytic voltage waveform to reproduce the entire waveform earlier in time. In [38], it is shown that

causality is solely connected with the occurrence of discontinuities, such as “fronts” and “backs” of signals, and not with the peaks in the voltage waveform, and, therefore, that causal loop paradoxes could never arise.

Researchers have investigated on the design [44] and application [45]-[50] of NGD to various electronic circuits. In [46]-[49], various applications of the NGD circuits with an active topology have been proposed such as on the baseband propagation delay reduction [48] and broadband and constant phase shifters [49]. In [50], a trial to design a passive NGD circuit for the feedforward power amplifier application was reported.

To understand the existence of NGD, the following equation can be revisited. In a medium of refractive index  $n(\omega)$ , the dispersion relation can be written as

$$k = \frac{\omega n}{c}, \quad (3-1)$$

where  $\kappa$  is the wave number. The group velocity ( $v_g$ ) which means the speed of the envelope signal, is then given by

$$v_g = \frac{c}{n + \omega \operatorname{Re}[dn/d\omega]}. \quad (3-2)$$

From (3-1) and (3-2), it can be inferred that if the refractive index decreases rapidly with regard to the frequency, the group velocity and the group delay can become negative. And this event does happen near an

absorption line or signal attenuation condition, where “anomalous” wave propagation effects can occur [39]. Typically, in the RF circuit design which is based on the dielectric laminate, the refractive index of the given material cannot be controlled. Therefore, it is only possible to obtain the NGD through the signal attenuation condition, which can be easily compensated with the small signal gain amplifier without reducing the amount of NGD.

## ***3.2 General Analysis and Design Technique to Generate the Negative Group Delay in RF Electronic Circuits***

### **3.2.1 Lumped Element Circuits**

Fig. 3.1 shows the lumped element shunt-series NGD circuit in 2-port transmissive configuration. After deriving the equivalent admittance of the shunt-series network, an ABCD matrix of this 2-port network can be calculated. By using the matrix conversion from the ABCD- to an S-matrix,  $S_{21}$  can be obtained. Finally, the equation for group delay can be obtained by partial differentiating the phase components of  $S_{21}$  with respect to  $\omega$  and substituting resonance condition as shown in (3-3).

From this equation, you can find that the group delay is always negative since all the parameters in the equation are positive in our real world. In (3-3), group delay is a function of inductance ( $L_{SS}$ ) and resistance ( $R_{SS}$ ).



$$\begin{aligned}
\tau \Big|_{\omega=\omega_0=1/\sqrt{L_{SS}C_{SS}}} &= -\frac{d\phi_{21}}{d\omega} \Big|_{\omega=\omega_0=1/\sqrt{L_{SS}C_{SS}}} \\
&= -\frac{d}{d\omega} \left\{ \arg(S_{21}) \right\} \Big|_{\omega=\omega_0=1/\sqrt{L_{SS}C_{SS}}} \\
&= -\frac{2Z_0L_{SS}}{(2R_{SS} + Z_0)R_{SS}}
\end{aligned} \tag{3-3}$$

Also, the magnitude of insertion loss ( $S_{21}$ ) and return loss ( $S_{11}$ ) can be mathematically obtained at the resonance frequency as in (3-4) and (3-5), respectively.

$$S_{21} \Big|_{\omega=\omega_0=1/\sqrt{L_{SS}C_{SS}}} = \frac{2R_{SS}}{2R_{SS} + Z_0} \tag{3-4}$$

$$\begin{aligned}
S_{11} \Big|_{\omega=\omega_0=1/\sqrt{L_{SS}C_{SS}}} &= 1 - S_{21} \Big|_{\omega=\omega_0=1/\sqrt{L_{SS}C_{SS}}} \\
&= \frac{Z_0}{2R_{SS} + Z_0}
\end{aligned} \tag{3-5}$$

For the intuitive understanding, (3-3) through (3-5) are represented in a graphical manner according to  $L_{SS}$  and  $R_{SS}$  by using MATLAB as in Fig. 3.2. The amount of NGD is inversely proportional to  $R_{SS}$  and proportional to  $L_{SS}$ , provided that the two parameters are positive, while  $L_{SS}$  is in resonance with  $C_{SS}$ . Also, it can be inferred that more NGD induces higher insertion loss and poorer return loss, delivering trade-off to the designer.

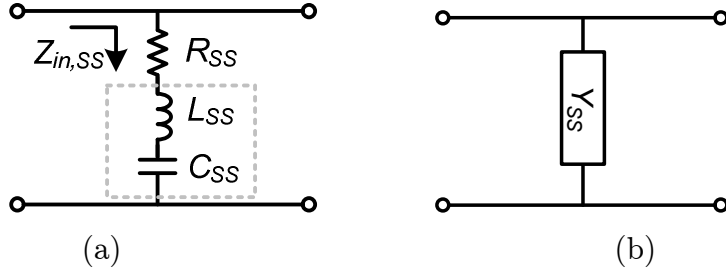


Figure 3.1: Lumped element NGD circuit in 2-port transmissive configuration: (a) shunt-series structure and (b) its equivalent admittance representation.

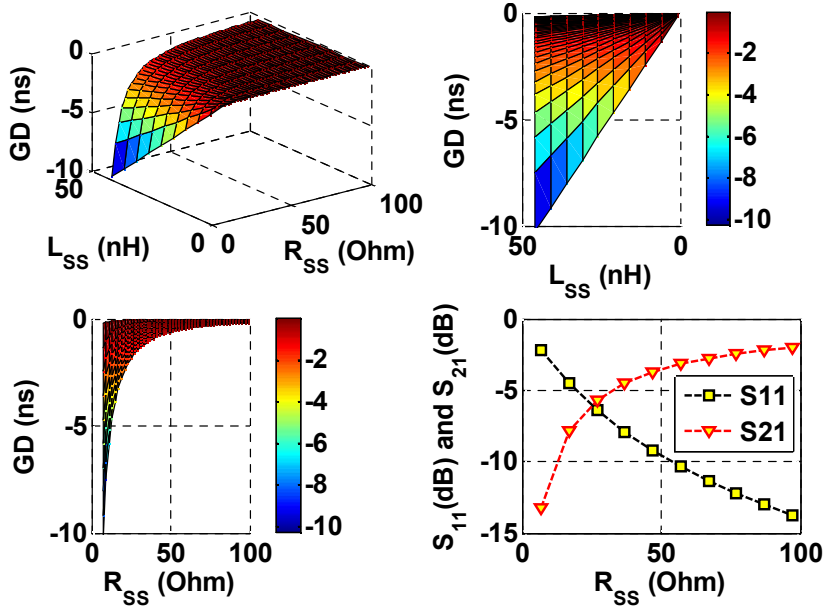


Figure 3.2: Calculated group delay, insertion loss, and return loss of shunt-series NGD circuit according to  $R_{SS}$  and  $L_{SS}$ . Color bar shows the amount of group delay.

Fig. 3.3 shows the circuit simulation result by using ADS of Agilent. The design frequency is 2.14 GHz, which is the center frequency of WCDMA base-station down-link. The group delay, insertion loss, and return loss of shunt-series NGD circuit are simulated at the frequency domain. NGD peak is observed at the resonance frequency. As explained earlier, this NGD is obtained in expense of signal attenuation, say, insertion loss in this case.

Fig. 3.4 shows the lumped element series-parallel NGD circuit in 2-port transmissive configuration. After deriving the equivalent impedance of the series-parallel network, the ABCD matrix of this 2-port network can be calculated. By using the matrix conversion from the ABCD- to S-matrix,  $S_{21}$  can be obtained. Finally, the equation for group delay can be obtained by partial differentiating the phase components of  $S_{21}$  with respect to  $\omega$  and substituting resonance condition as shown in (3-6).

From this equation, you can find that the group delay is always negative since all the parameters in the equation are positive in our real world. In (3-6), the group delay is a function of inductance ( $C_{sp}$ ) and parallel resistance ( $R_{sp}$ ). Also, the magnitude of insertion loss ( $S_{21}$ ) and return loss ( $S_{11}$ ) can be mathematically obtained at the resonance frequency as in (3-7) and (3-8), respectively.

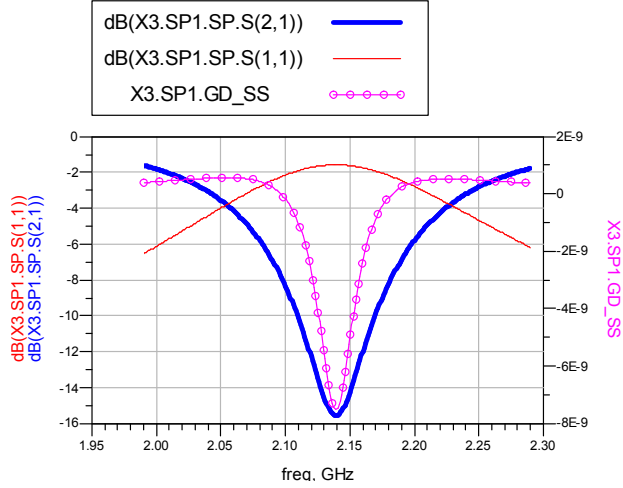


Figure 3.3: Simulated group delay, insertion loss, and return loss of shunt-series NGD circuit. ( $R_{SS}=5 \Omega$ ,  $C_{SS}=0.246 \text{ pF}$ ,  $L_{SS}=22.5 \text{ nH}$ )

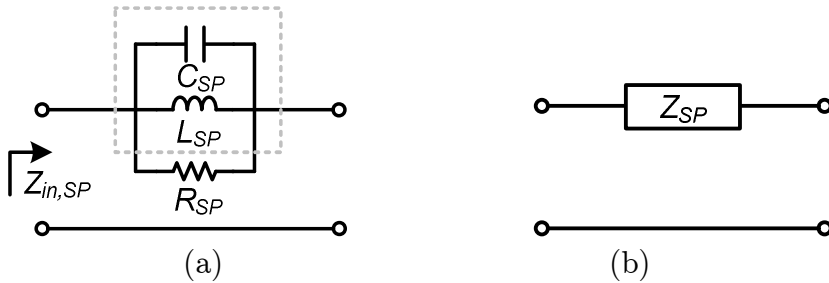


Figure 3.4: Lumped element NGD circuit in 2-port transmissive configuration: (a) series-parallel structure and (b) its equivalent impedance representation.

$$\begin{aligned}
\tau \Big|_{\omega=\omega_0=1/\sqrt{L_{SP}C_{SP}}} &= -\frac{d\phi_{21}}{d\omega} \Big|_{\omega=\omega_0=1/\sqrt{L_{SP}C_{SP}}} \\
&= -\frac{d}{d\omega} \left\{ \frac{\text{imag}(S_{21})}{\text{real}(S_{21})} \right\} \Big|_{\omega=\omega_0=1/\sqrt{L_{SP}C_{SP}}} \\
&= -\frac{2R_{SP}^2 C_{SP}}{2Z_0 + R_{SP}}
\end{aligned} \tag{3-6}$$

$$S_{21} \Big|_{\omega=\omega_0=1/\sqrt{L_{SP}C_{SP}}} = \frac{2Z_0}{R_{SP} + 2Z_0} \tag{3-7}$$

$$\begin{aligned}
S_{11} \Big|_{\omega=\omega_0=1/\sqrt{L_{SP}C_{SP}}} &= 1 - S_{21} \Big|_{\omega=\omega_0=1/\sqrt{L_{SP}C_{SP}}} \\
&= \frac{R_{SP}}{R_{SP} + 2Z_0}
\end{aligned} \tag{3-8}$$

For the intuitive understanding, (3-6) through (3-8) are represented in a graphical manner according to  $L_{SP}$  and  $R_{SP}$  by using MATLAB as in Fig. 3.5. The amount of NGD is proportional to  $R_{SP}$  and  $C_{SS}$ , provided that the two parameters are positive, while  $C_{SP}$  is in resonance with  $L_{SP}$ . Also, it can be inferred that more NGD induces higher insertion loss and poorer return loss, same as in shunt-series case.

Fig. 3.6 shows the circuit simulation result by using ADS of Agilent. For the same design frequency, the group delay, insertion loss, and return loss of shunt-series NGD circuit are simulated at the frequency domain. NGD peak is observed at the resonance frequency. As explained earlier, this NGD is obtained in expense of signal attenuation, say, insertion loss in this case.

Fig. 3.7 shows the lumped element reflective-series NGD circuit in 1-port reflective configuration. After deriving the input impedance of the reflective-series network, input reflection coefficient of this 2-port network,  $\Gamma_{RS}$  or the magnitude of  $S_{11}$  can be calculated. In this case, the termination impedance is assumed to be  $50 \Omega$ . Finally, the equation for group delay can be obtained by partial differentiating the phase components of  $S_{11}$  with respect to  $\omega$  and substituting the resonance condition as shown in (3-9).

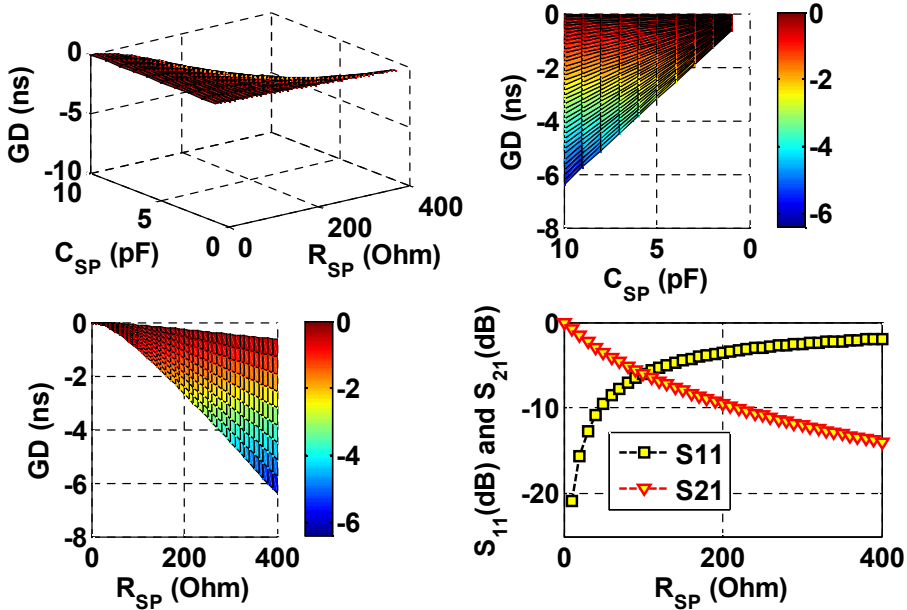


Figure 3.5: Calculated group delay and return loss of series-parallel NGD circuit according to  $R_{SP}$  and  $C_{SP}$ . Color bar shows the amount of group delay.

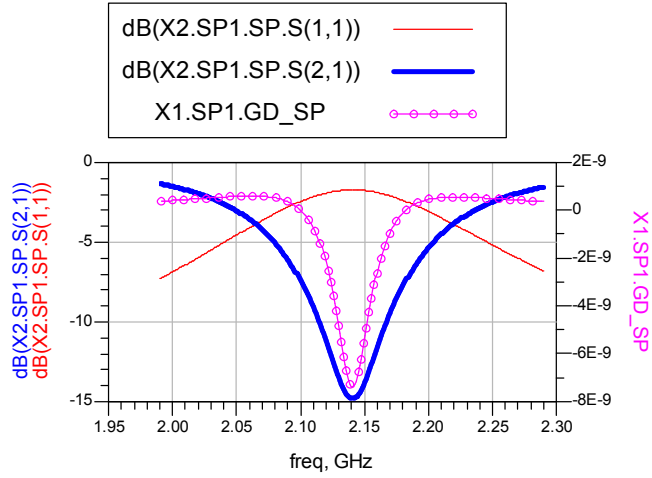


Figure 3.6: Simulated group delay, insertion loss, and return loss of series-parallel NGD circuit. ( $R_{SP}=450 \Omega$ ,  $C_{SP}=10.05 \text{ pF}$ ,  $L_{SP}=0.55 \text{ nH}$ )

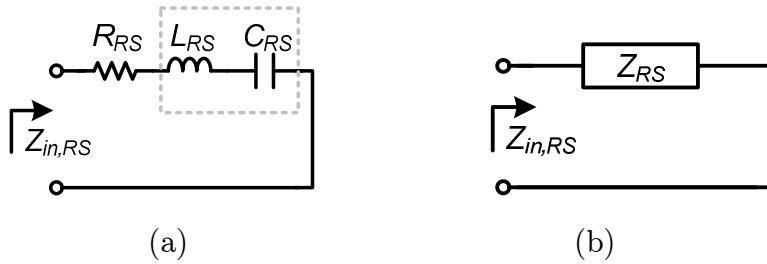


Figure 3.7: Lumped element NGD circuit in 1-port reflective configuration: (a) reflective-series structure and (b) its equivalent impedance representation.

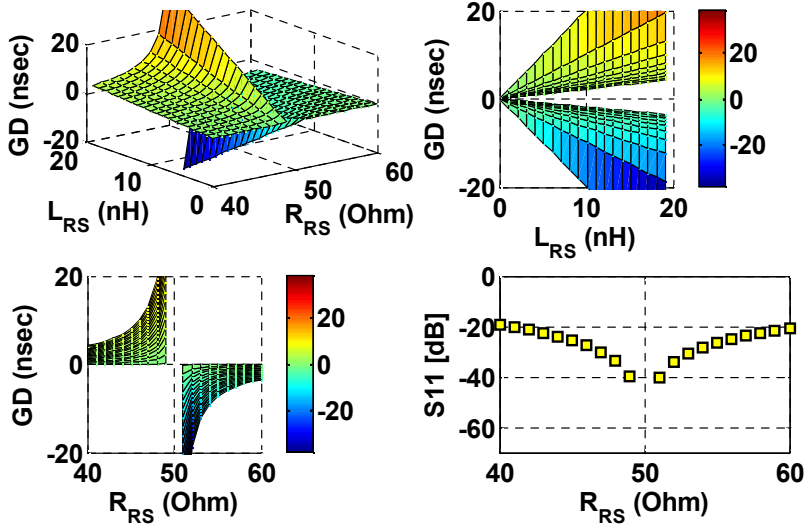


Figure 3.8: Calculated group delay and return loss of reflective-series NGD circuit according to  $R_{RS}$  and  $L_{RS}$ . Color bar shows the amount of group delay.

Also the magnitude of input reflection coefficient at the resonant frequency can be represented as (3-10). For the intuitive understanding, (3-9) and (3-10) are represented in a graphical manner according to  $L_{RS}$  and  $R_{RS}$  as in Fig. 3.8. In the 1-port reflective topology, the response is different from the 2-port configuration. In this case, there is an abrupt transition between the positive and NGD at  $R_{RS}=50 \Omega$ . The amount of NGD is proportional to  $L_{RS}$  and inversely proportional to  $R_{RS}$ , provided that  $R_{RS}$  is not smaller than  $50 \Omega$ .

$$\begin{aligned}
 \tau \Big|_{\omega=\omega_0=1/\sqrt{L_{RS}C_{RS}}} &= -\frac{d\phi_{RS}}{d\omega} \Big|_{\omega=\omega_0=1/\sqrt{L_{RS}C_{RS}}} \\
 &= -\frac{d}{d\omega} \left\{ \arg(\Gamma_{RS}) \right\} \Big|_{\omega=\omega_0=1/\sqrt{L_{RS}C_{RS}}} \\
 &= -\frac{4L_{RS}Z_0}{R_{RS}^2 - Z_0^2}
 \end{aligned} \tag{3-9}$$



$$\Gamma_{RS} \Big|_{\omega=\omega_0=1/\sqrt{L_{RS}C_{RS}}} = \frac{R_{RS} - Z_0}{R_{RS} + Z_0} \quad (3-10)$$

When  $R_{RS}$  is smaller than  $50 \Omega$ , NGD cannot be achieved even though there is a large amount of insertion loss. From Fig. 3.8, it can be inferred that more NGD induces more signal attenuation, challenging trade-off to the designer, since the reflection coefficient is equal to the insertion loss for the 1-port circuit.

Fig. 3.9 shows the circuit simulation result by using ADS of Agilent. For the same design frequency, the group delay, insertion loss, and return loss of reflective-series NGD circuit are simulated at the frequency domain. The NGD peak is observed at the resonance frequency. As explained earlier, this NGD is obtained in expense of signal attenuation, say, return loss in this case.

Fig. 3.10 shows the lumped element reflective-parallel NGD circuit in 1-port reflective configuration. Through the same procedure,  $\Gamma_{RP}$  or magnitude of  $S_{11}$  can be calculated. Finally, the equation for group delay can be obtained by partial differentiating the phase components of  $S_{11}$  with respect to  $\omega$  and substituting resonance condition as shown in (3-11).

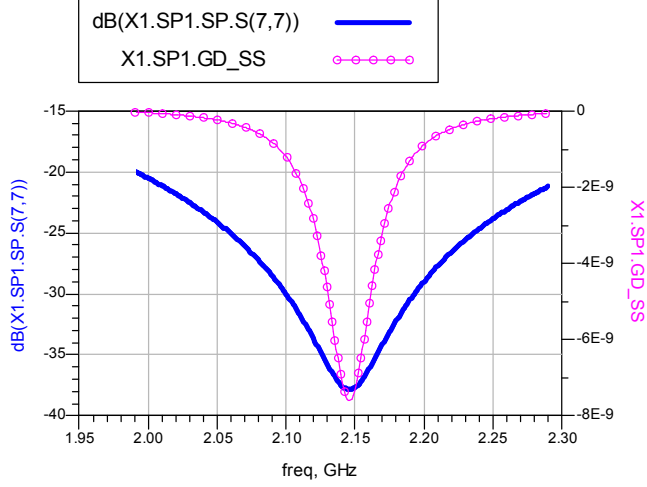


Figure 3.9: Simulated group delay, insertion loss, and return loss of reflective-series NGD circuit. ( $R_{RS}=50.7 \Omega$ ,  $C_{RS}=1.8437 \text{ pF}$ ,  $L_{RS}=3.0 \text{ nH}$ ).

Also the magnitude of input reflection coefficient at the resonant frequency can be represented as (3-12). For the intuitive understanding, (3-11) and (3-12) are represented in a graphical manner according to  $C_{RP}$  and  $R_{RP}$  as in Fig. 3.11. In this case, there is an abrupt transition between the positive and negative group delay at  $R_{RP}=50 \Omega$ . The amount of NGD is proportional to  $C_{RP}$  and  $R_{RP}$ , provided that  $R_{RP}$  does not exceed  $50 \Omega$ . When  $R_{RP}$  is larger than  $50 \Omega$ , NGD cannot be achieved even though there is the same amount

$$\begin{aligned}
 \tau \Big|_{\omega=\omega_0=1/\sqrt{L_{RP}C_{RP}}} &= -\frac{d\phi_{RP}}{d\omega} \Big|_{\omega=\omega_0=1/\sqrt{L_{RP}C_{RP}}} \\
 &= -\frac{d}{d\omega} \left\{ \arg(\Gamma_{RP}) \right\} \Big|_{\omega=\omega_0=1/\sqrt{L_{RP}C_{RP}}} \\
 &= \frac{4R_{RP}^2 Z_0 C_{RP}}{R_{RP}^2 - Z_0^2}
 \end{aligned} \tag{3-11}$$



Figure 3.10: Lumped element NGD circuit in 1-port reflective configuration: (a) reflective-parallel structure and (b) its equivalent admittance representation.

$$\Gamma|_{\omega=\omega_0=1/\sqrt{LC}} = \frac{Z_0 + R_{RP}}{Z_0 - R_{RP}} \quad (3-12)$$

of insertion loss. From Fig. 3.11, it can be inferred that more NGD induces more signal attenuation, challenging trade-off to the designer, since the reflection coefficient is equal to the insertion loss for the 1-port circuit.

Fig. 3.12 shows the circuit simulation result by using ADS of Agilent. For the same design frequency, the group delay, insertion loss, and return loss of reflective-series NGD circuit are simulated at the frequency domain. NGD peak is observed at the resonance frequency. As explained earlier, this NGD is obtained in expense of signal attenuation, say, return loss in this case.

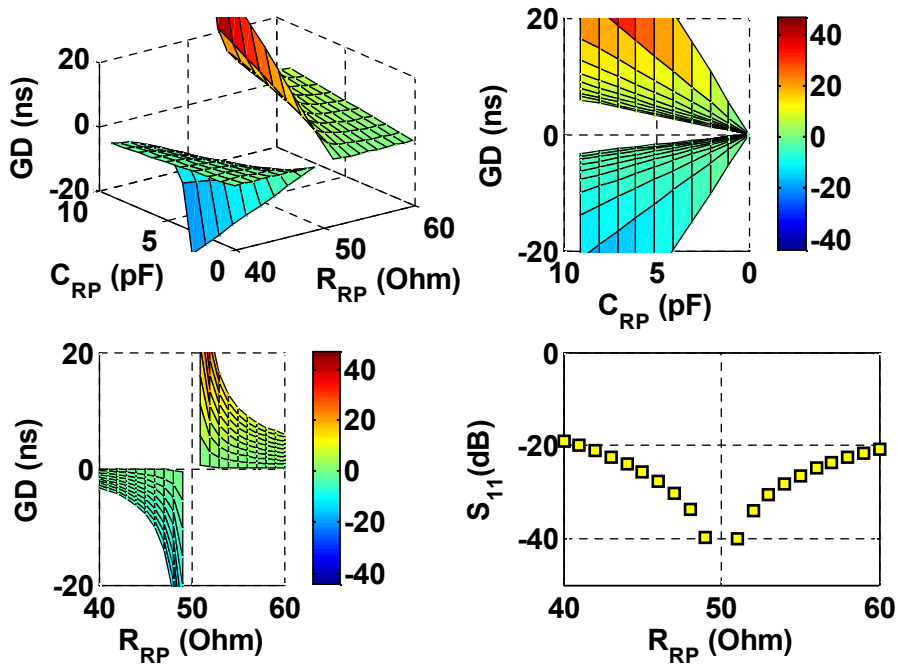


Figure 3.11: Calculated group delay and return loss of reflective-parallel NGD circuit according to  $R_{RP}$  and  $C_{RP}$ . Color bar shows the amount of group delay.

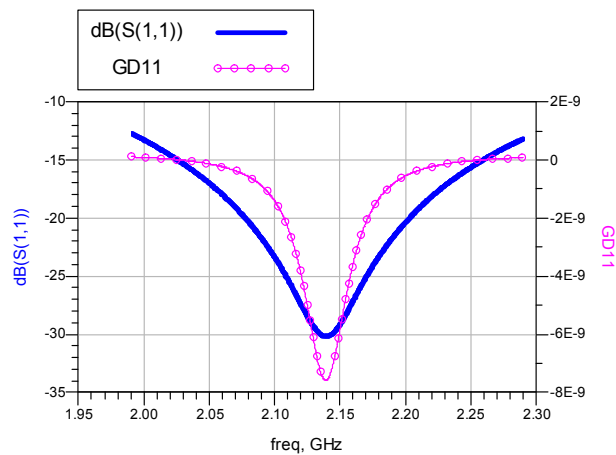


Figure 3.12: Simulated group delay, insertion loss, and return loss of reflective-parallel NGD circuit. ( $R_{RP}=47.2 \Omega$ ,  $C_{RP}=5 \text{ pF}$ ,  $L_{RP}=1.107 \text{ nH}$ )

### 3.2.2 Distributed Element Circuits

One major difficulty of the lumped element (LE) circuit is the feasibility of the designed component values. In the microwave circuit design, a specific length of open or short terminated transmission line is often used as a resonator, called a transmission line resonator (TLR). Fig. 3.13 shows the four types of distributed element (DE) NGD circuits converted from the LE prototype circuit. It is noted that Fig. 3.13 (a) and (c) have an odd multiple of the quarter-wavelength, and Fig. 3.13 (b) and (d) have a multiple of the half-wavelength, with  $n=1$  being chosen for small size. The 1-port RP network in Fig. 3.10 can be converted either into the quarter-wavelength short circuit (QS) of Fig. 3.13 (c) or the half-wavelength open circuit (HO) of Fig. 3.10 (d). The RS network in Fig. 3.7 can be converted either into the quarter-wavelength open circuit (QO) of Fig. 3.13 (a) or the half-wavelength short circuit (HS) of Fig. 3.13 (b). The characteristic impedance and admittance for the four types of TLR can be derived as follows, respectively:

$$Y_{C,QS} = \frac{4\omega_0 C_{RP}}{\pi} \quad (3-13)$$

$$Y_{C,HO} = \frac{2\omega_0 C_{RP}}{\pi} \quad (3-14)$$

$$Z_{C,HS} = \frac{2\omega_0 L_{RS}}{\pi} \quad (3-15)$$

$$Z_{C,QO} = \frac{4\omega_0 L_{RS}}{\pi} \quad (3-16)$$

An example to show the validity of a prototype RP LE NGD circuit and its equivalent DE circuit were simulated. By using (3.11) and Fig. 3.11, it is calculated that  $R_{RP}=47.5 \Omega$ ,  $C_{RP}=1.0 \text{ pF}$ , and  $L_{RP}=5.535 \text{ nH}$  to obtain  $-9 \text{ ns}$ , and the estimated return loss was  $-31.82 \text{ dB}$  derived from (3-12) at the center frequency of  $2.14 \text{ GHz}$ . The required group delay value of  $-9 \text{ ns}$  is obtained as a rule of thumb after the practical feedforward application which will be explained later. Then, the LE circuit was converted into the TLR using

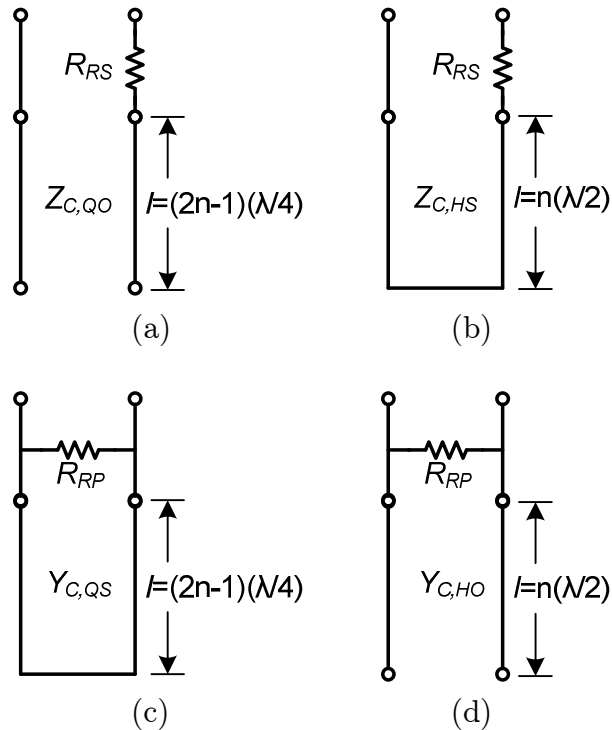


Figure 3.13: Four types of 1-port distributed element NGD circuit: (a) quarter-wavelength open, (b) half-wavelength short, (c) quarter-wavelength short, and (d) half-wavelength open circuit.

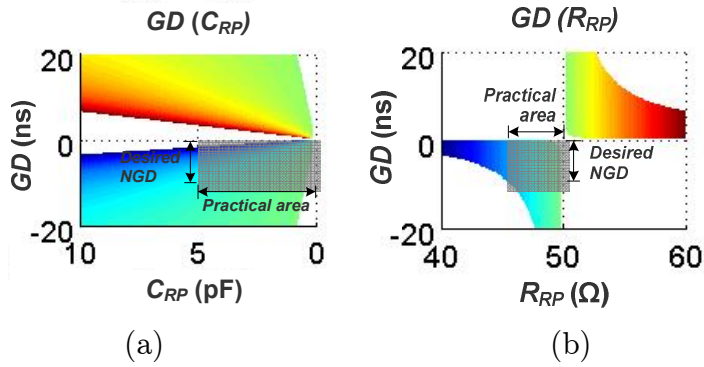


Figure 3.14: Practical range for NGD circuit design according to (a)  $C_{RP}$  and (b)  $R_{RP}$ .

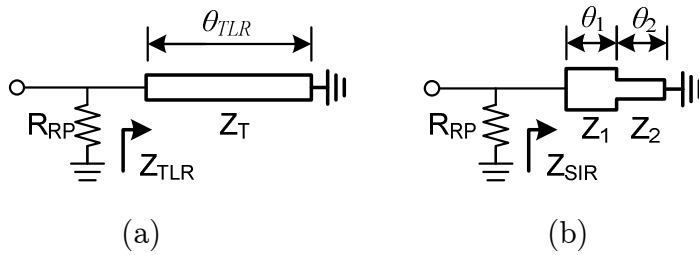


Figure 3.15: Schematic diagram of the reflective parallel 1-port NGD circuit using: (a) transmission line resonator and (b) size reduced stepped impedance resonator. ( $\theta_{TLR}=90^\circ$  and  $\theta_{SIR}=65^\circ$ )

(3-13), and the calculated characteristic impedance for the QS was  $58.4 \Omega$ . As shown in Fig. 3.14, since there is infinite number of combinations for LC resonating pairs,  $C_{RP}$  should be carefully chosen so that the characteristic impedance of TLR should not exceed the practical range. Larger amount of

NGD value beyond 10 ns involves the bandwidth limitation as well as the higher insertion loss.

Based on the above analysis, other types of resonator can be used to generate the NGD. A stepped impedance resonator (SIR) is selected, which has its own advantages as size reduction and controllable harmonic responses.

Fig. 3.15 (a) shows the schematic diagram of the reflective parallel 1-port NGD circuit using the TLR. And its SIR equivalence is shown in Fig. 3.15 (b). TLRs are widely used because of their simple structure and easy-to-design features. In practical design, however, such resonators have a number of intrinsic disadvantages, such as the limited design parameters due to their simple structure and spurious responses at integer multiples of the fundamental frequency [59]. The SIR was proposed to overcome those problems. The typical features of SIR are summarized as follows: (1) a wide degree of freedom, (2) derivation of generalized concept for transmission line resonators, (3) development of an expanded concept for non-uniform impedance resonators, (4) size reduction, and (5) spurious reduction.

The ratio of the impedance step by  $Z_1$  and  $Z_2$  is defined as  $m$ , which can be expressed using the resonance condition as follows [59]:

$$\begin{aligned}
 m &= \frac{Z_2}{Z_1}, \\
 &= \tan \theta_1 \tan \theta_2
 \end{aligned}
 \tag{3-17}$$



where  $\theta_1$  and  $\theta_2$  refers to the electrical length of each stepped impedance section  $Z_1$  and  $Z_2$ . The total electrical length ( $\theta_{SIR}$ ) is equal to the sum of  $\theta_1$  and  $\theta_2$ . The minimum electrical length can be derived as follows:

$$(\theta_{SIR})_{\min} = \tan^{-1}\left(\frac{2\sqrt{m}}{1-m}\right), \quad (3-18)$$

where  $\theta_1=\theta_2=\tan^{-1}(m)$  and  $m$  should be smaller than 1 for the size reduction. The size reduction factor  $S_R$  can be defined as the ratio of the electrical length of the TLR and SIR:

$$S_R = \frac{\theta_{SIR}}{\theta_{TLR}}. \quad (3-19)$$

As a design example, the goal is set to design a 1-port NGD circuit at 2.14 GHz. To reduce the size,  $m=0.4$ ,  $Z_1=100 \Omega$  and  $Z_2=40 \Omega$  were chose for practical fabrication. Calculated  $\theta_{SIR}$  is  $65^\circ$ . In case of the  $\lambda/4$  transmission line resonator, the estimated size reduction ratio when converted to the SIR is 72 % from the original size. Higher  $m$  can result in more size reduction, but the unwanted parasitic effect can also occur at the step junction of transmission line due to the large impedance steps.

To validate the conversion theory, the 1-port NGD circuit shown in Fig. 3.15 was simulated using Agilent's ADS2009. Fig. 3.16 shows the simulated real and imaginary magnitude of the complex reflection coefficients of the 1-port NGD circuit with the TLR and SIR. For the whole frequency band of

interest, the two resonators are similar in real and imaginary reflection coefficients and slope parameters.

Fig. 3.17 and Fig. 3.18 show the simulated group delay response. Fig. 3.17 represents the narrowband NGD characteristic, and the peak NGD values at the center frequency are 9.0 ns and 8.8 ns for the TLR-loaded NGD circuit and SIR-loaded NGD circuit, respectively. From Fig. 3.18 that shows the harmonic response of the NGD, the 1-port NGD circuit with transmission line resonator has its intrinsic spurious response at the 3rd harmonic frequency, 6.42 GHz ( $3f_0$ ) in this case. This spurious response may cause an unwanted operation when the NGD circuit is integrated into a system. However, in case of the 1-port NGD circuit with the SIR, the spurious response is not observed at the 3rd harmonic frequency but it is observed at much higher frequency around 9.7 GHz (about  $4.5f_0$ ). This property is obtained due to the impedance step and the separated electrical length of the SIR.

### 3.2.3 Reflective Circuits for Input/Output Return Loss Improvement

In its current stand alone topologies explained so far, it is not practical to use the practical circuits because the poor return loss would make the circuit behave differently when connected to other circuits. There is one representative technique to improve the input and output return loss

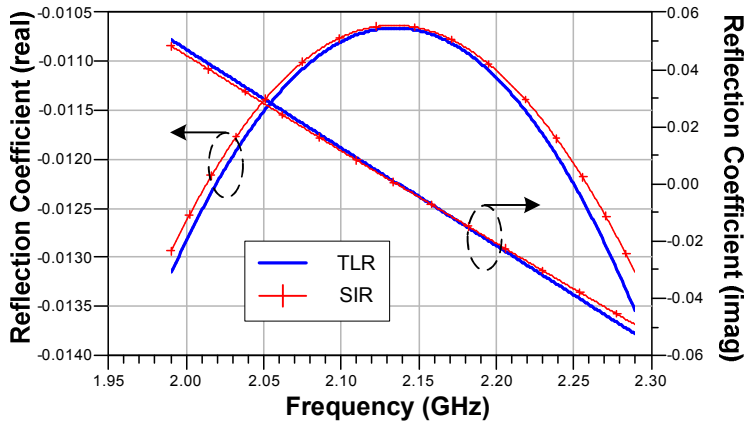


Figure 3.16: Real and imaginary magnitude of reflection coefficient of the 1-port NGD circuit with the transmission line resonator and stepped impedance resonator.

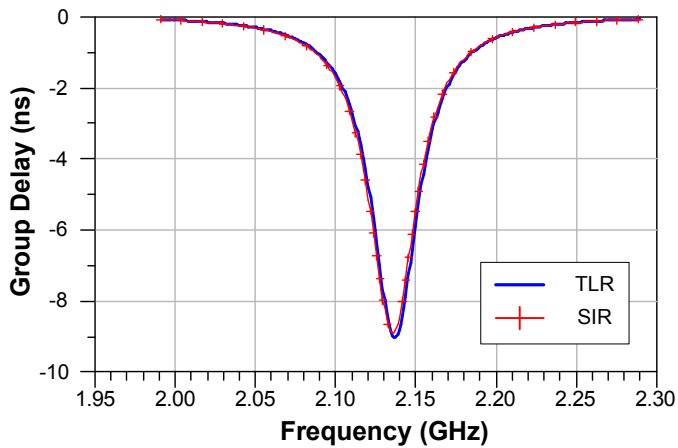


Figure 3.17: Simulated in-band group delay response of the 1-port NGD circuit with the transmission line resonator and stepped impedance resonator.

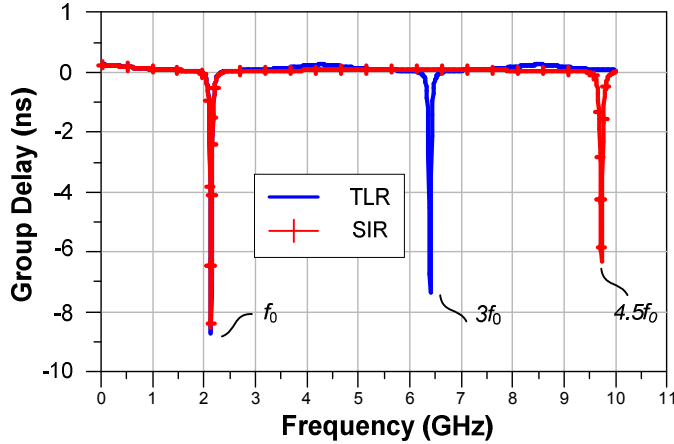


Figure 3.18: Harmonic group delay response of the 1-port NGD circuit with the transmission line resonator and stepped impedance resonator.

employing  $90^\circ$  hybrid couplers in RF frequency.

Fig. 3.19 through Fig. 3.20 show the possible design of the NGD circuits employing  $90^\circ$  hybrid couplers. A reflection topology is very widely used in designing adjustable circuits such as a variable attenuator and phase shifter. The 2-port NGD circuits of reflection topology using LE reflective-series structure, its equivalent distributed circuit with the QO resonator, and equivalent distributed circuit with the HS resonator are shown in Fig. 3.19. Fig. 3.20 show the 2-port NGD circuits of the reflection topology using the LE reflective-parallel structure, their equivalent distributed circuit with the QS resonator, and equivalent distributed circuit with the HO resonator.

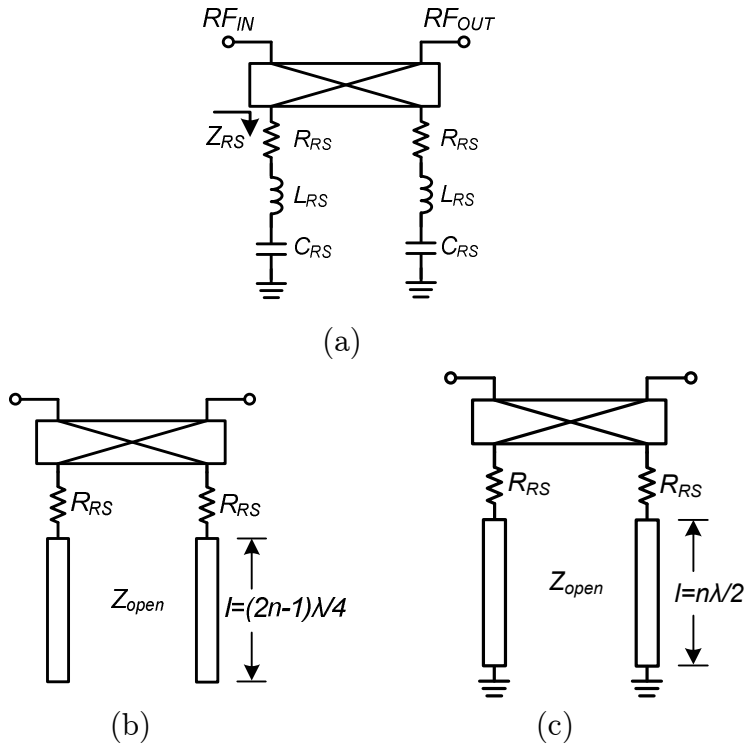


Figure 3.19: 2-port reflection topology NGD circuits: (a) lumped element reflective-series structure, (b) its equivalent distributed circuit with quarter-wave open resonator, and (c) equivalent distributed circuit with half-wave short resonator.

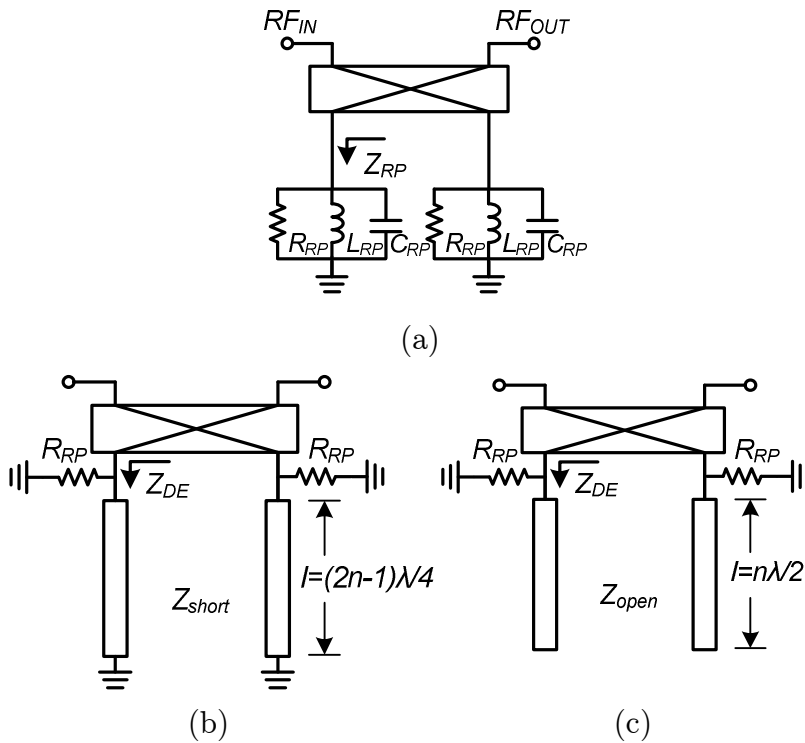


Figure 3.20: 2-port reflection topology NGD circuits: (a) lumped element reflective-parallel structure, (b) its equivalent distributed circuit with quarter-wave short resonator, and (c) equivalent distributed circuit with half-wave open resonator.

### ***3.3 Optimized 2-stage Negative Group Delay Circuit Design for Linearization Techniques***

As a prototype, a microstrip 3dB branch line coupler is designed as a 90° hybrid. To reduce the circuit size, a commercial, low profile, and miniature 3dB hybrid coupler with the surface mount package can be used.

For an experimental verification, the goal is set to design a 2-stage reflective DE NGD circuit with the total group delay of -9 ns, close to 0 dB insertion loss at the center frequency, and 30 MHz bandwidth centered on the WCDMA downlink band (2.125~2.155 GHz). This NGD value is chosen for the compensation of the signal transmission time due to the circuits in the EPA path in the feedforward technique.

The proposed circuit would be constructed of the 90° hybrids and two DE NGD circuit units (#1 and #2) of which the center frequencies were 2.125 GHz and 2.155 GHz, respectively, as shown in Fig. 3.21. By connecting the two units in a cascade, the flat group delay and transmission response can be obtained. The insertion loss of the NGD circuit itself could be compensated by the general purpose small signal amplifier as shown in Fig. 3.21. A compensation capacitor ( $C_{COMP}$ ) would be connected in parallel to the  $R_{RP}$  to compensate for the minute parasitic inductance of a chip resistor so that the  $R_{RP}$  would not have any reactive impedance. Fig. 3.22 shows the photograph

of the fabricated circuit. Total size of the fabricated 2-stage DE NGD circuit is  $180 \times 90 \text{ mm}^2$ .

Next step is to design the  $90^\circ$  hybrid coupled reflective NGD circuit optimized for each upper and lower edge of target frequency band, 2.125 GHz and 2.155 GHz ( $2.14 \pm 15 \text{ MHz}$ ), as shown in Fig. 3.23. Unit cells for each band have group delay of -8 ns and insertion loss of 33dB.

Fig. 3.24 shows the simulation and measurement results of the 2-stage DE NGD circuit. One notable advantage of the proposed topology is that the same magnitude and group delay response can be obtained when the position of the gain amplifier is changed. In other words, the 1<sup>st</sup> gain amplifier ( $G$ ) can be moved to the output of the 2<sup>nd</sup> NGD circuit (Unit #2) according to the input power level. In that way, it is possible to avoid the potential nonlinear distortion generation in the NGD module. The measured results of Fig. 3.24 (a) agree well with the simulation results, where the measured group delay and the insertion loss were  $-9 \pm 0.25 \text{ ns}$  and  $0.21 \pm 0.06 \text{ dB}$  in the operating frequency, respectively. The small amount of group delay and magnitude error is due to the connecting elements and the gain of the small signal amplifier.



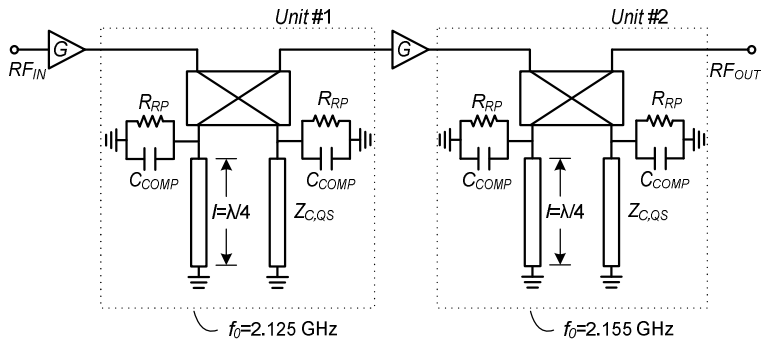


Figure 3.21: Circuit diagram of 2-stage reflection type NGD circuit.

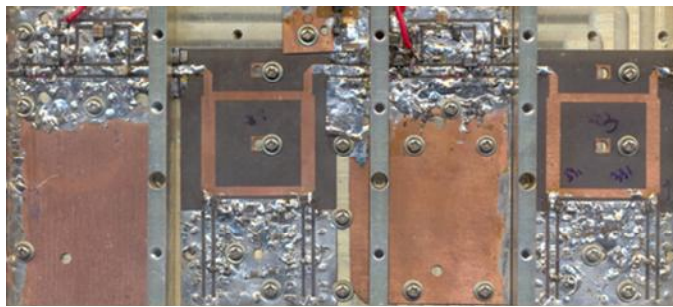


Figure 3.22: Photograph of the fabricated 2-stage reflection type NGD circuit.

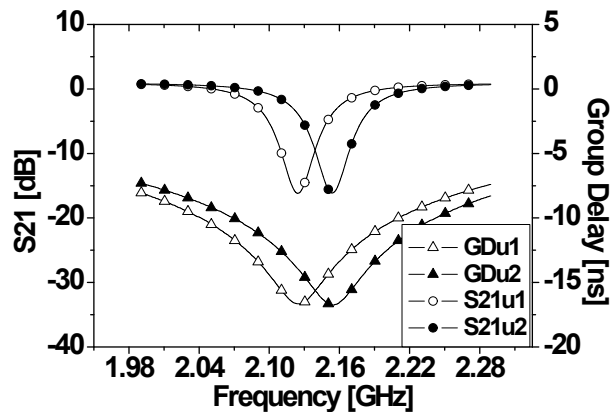
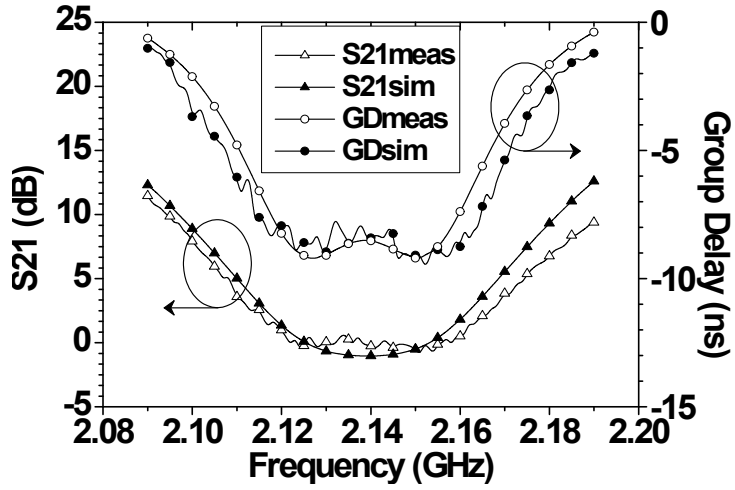


Figure 3.23: Simulated transmission coefficient and group delay of Unit #1 and Unit #2.

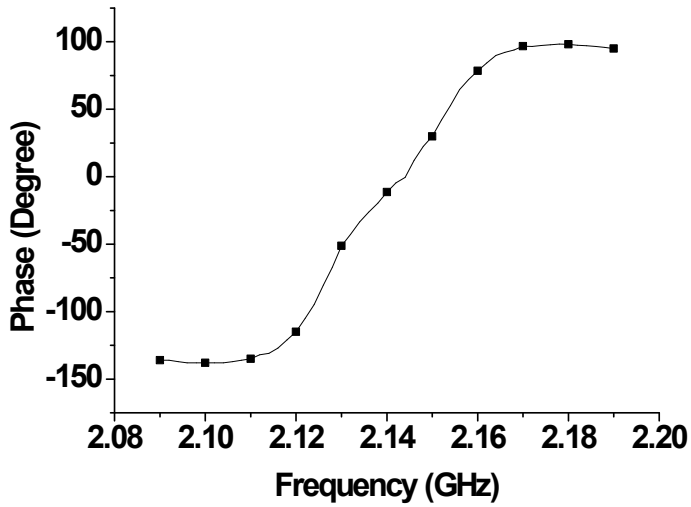
Fig. 3.24 (b) represents the phase jump observed in the NGD region. In the NGD region, the slope of the phase is observed to be positive, implying that the group velocity is negative. The negative group velocity can be translated as the direction of envelope propagation is opposite to the direction of the signal propagation. This inverted phase slope can be used to cancel out or control the negative phase slope (or positive group delay) of the typical circuit, consequently achieving zero phase slope (therefore smaller or even zero group delay). In the case that larger negative group delay would be necessary, a designer should make a trade off between the group delay and the bandwidth. In regards to the additional DC power consumption in the NGD circuit, each small signal amplifier consists of two ERA-5SM of Mini-Circuits and consumes around 1 W. This DC power consumption is a relatively small amount when compared to the RF power level in a typical base-station PA.

### ***3.4 Experimental Verification for the Time Advance Property of Negative Group Delay with Arbitrary Time Domain Waveform***

In the earlier chapters, the NGD is validated by using 1-tone continuous wave (sinusoidal signal in time domain) signal. In a sinusoidal wave case, perfect signal cancellation condition such as the same magnitude and out-of-



(a)



(b)

Figure 3.24: 2-stage reflection type NGD circuit: (a) Simulated and measured group delay and insertion loss, (b) measured phase response.

phase can be met at every  $2\pi$  period even though group delay matching is not secured. Also, mostly Gaussian pulse was used in the previous research results. Therefore it is necessary to validate the existence of the NGD in RF electronic circuits through the loop suppression test by using arbitrary time domain waveform. It is because current communication schemes usually employ broadband CDMA, WCDMA, or OFDM signals which are represented as an arbitrary waveform in time domain.

In this subsection, the arbitrary time domain voltage waveform is obtained from the WCDMA signal to model the modulated waveform. The time delayed output is obtained when the signal is applied to a normal electronic circuit. If the same signal was applied to the NGD circuit, the time advanced waveform could be obtained. Fig. 3.25 illustrates the input (center), the time delayed output (lower), and the time advanced output (upper) with a positive ( $+\tau$ ) and negative ( $-\tau$ ) group delay, respectively. When the input signal is applied to the cancellation loop of Fig. 3.26, the input signal will be cancelled at the output summing node if the amplitude, the out-of-phase, and the group delay balance conditions are matched simultaneously. On the contrary, if the remaining signal of the cancellation loop is sufficiently small at the output node, it can be concluded that time advance surely occurred

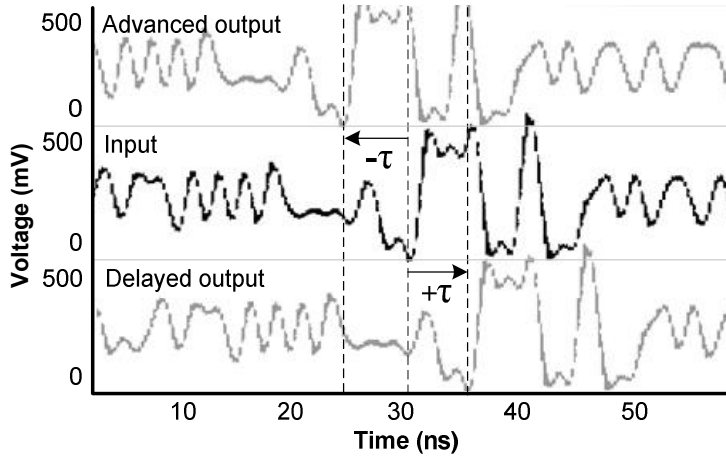


Figure 3.25: The simulation of the time delayed and the advanced output voltages for an arbitrary waveform.

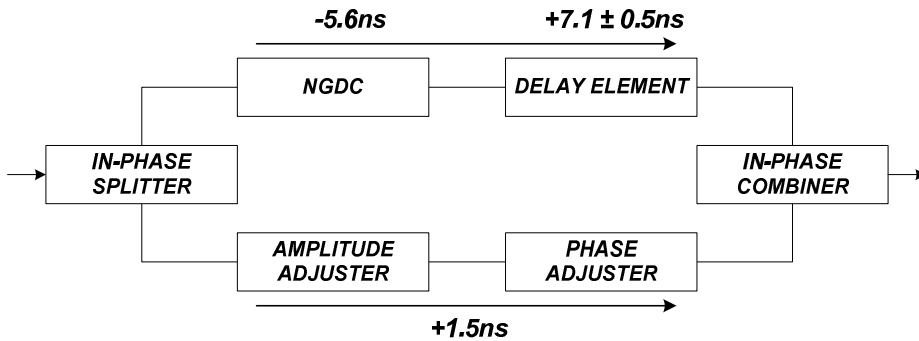


Figure 3.26: The schematic diagram of a simple signal cancellation loop employing an NGD circuit.

and that it is useful for an arbitrary waveform. Fig. 3.27 shows the photograph of the implemented signal suppression loop.

By providing the amplitude, the out-of-phase and the group delay matching conditions between the two paths, a loop suppression of about 30 dB was achieved with the CW signal, as shown in Fig. 3.28. This result can

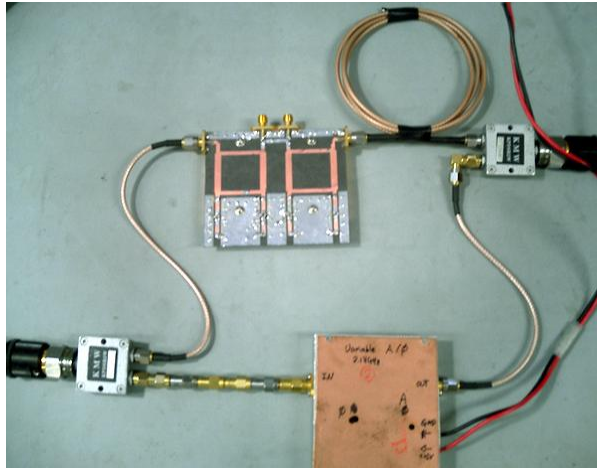


Figure 3.27: Photograph of the implemented signal cancellation loop.

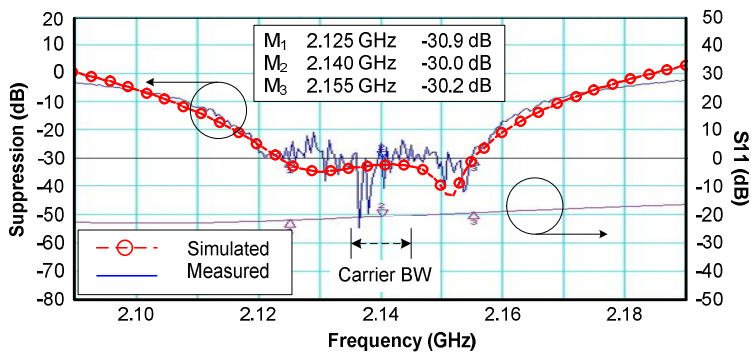


Figure 3.28: Simulated and measured closed loop cancellation results with the swept CW signal.

be interpreted into the out-of-phase mismatch of  $\pm 1.8^\circ$ , the amplitude mismatch of  $\pm 0.28$  dB, and the group delay mismatch of  $\pm 0.16$  ns, when all the other conditions are assumed to be perfectly matched, respectively.

In the case when the WCDMA 4FA signal was applied, around 30 dB suppression was obtained, as shown in Fig. 3.29. This implies that the

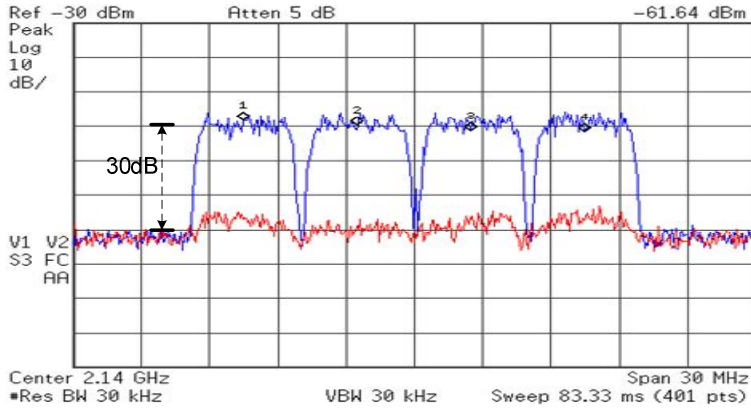


Figure 3.29: The measured output spectrum of the open loop (unsuppressed) and closed loop (suppressed) with 4-carrier WCDMA signal.

proposed NGD circuit can successfully compensate for the positive group delay of a normal electronic circuit when the time-varying arbitrary envelope modulation signal was used. The bandwidth of 20 dB suppression reaches up to 45 MHz. Some degradation was observed near the band edge. It can be optimized by increasing or reducing the frequency offset of the two center frequencies of the two NGD circuit units.

### 3.5 Summary and Discussion

In this chapter, the NGD concept, methods to obtain the NGD, and experimental verification results were discussed. At first, various LE circuit structures were introduced and mathematically analyzed to find the condition to obtain the NGD. Then the LE circuit was converted into the DE circuit based on the traditional filter design theory. To improve the circuit

performance, the NGD circuits with the reflection topology were proposed. To experimentally validate the existence of the NGD in RF electronic circuits, CW and WCDMA signals were used. Based on this interesting NGD concept and the design methodology, I will proceed to apply the time advance concept to the RF PA linearization technique to improve the efficiency and bandwidth performance.



## CHAPTER 4

# LINEARIZATION TECHNIQUES OF RF POWER AMPLIFIERS USING NEGATIVE GROUP DELAY CHARACTERISTICS

### *4.1 Design and Measurement of Power Amplifiers*

In this subsection, the output power, gain, efficiency performances of the PAs utilized in the interlock experiment will be briefly explained.

#### 4.1.1 Medium Power Linear Power Amplifier

Fig. 4.1 shows the photograph of the fabricated 20 W PA to be used as a final stage EPA for the feedforward application. Currently, due to its high breakdown voltage and high power density per area and efficiency, GaN HEMT device is widely used. The utilized RF transistor is GaN HEMT NPTB00025 of Nitronex, which has a peak envelope power of 25 W. Through careful load-pull measurement, the optimum source and load impedance were found as  $Z_S=3.875-j6.547$  and  $Z_L=7.711-j1.774$  when the DC bias condition was  $V_{DS}=28$  V,  $I_{DS}=250$  mA, typical value for Class-AB operation.

Measurement results are summarized and illustrated in Table 4.1 and Fig. 4.2. The maximum output power is 43.13 dBm with the saturated gain of

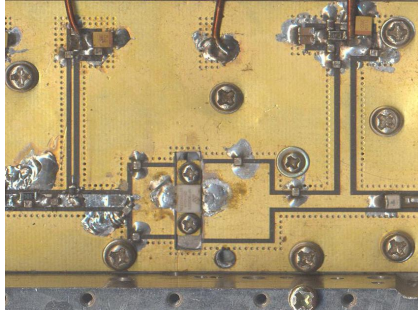


Figure 4.1: Photograph of the fabricated 20 W PA as a final stage EPA for feedforward application.

TABLE 4.1: MEASUREMENT TABLE FOR GAIN AND PAE OVER OUTPUT POWER.

Main (225mA, 60Ohm)							
Pin	Pout	Gain	Ids_min	Ids_max	Vds	PAEmin	PAEmax
14.95	30.00	15.05	250	270	28	12.8	13.8
15.97	31.00	15.03	270	290	28	15.0	16.1
17.01	32.00	14.99	290	310	28	17.7	18.9
18.03	33.00	14.97	330	340	28	20.3	20.9
19.04	34.00	14.96	340	360	28	24.1	25.5
20.07	35.00	14.93	380	400	28	27.3	28.8
21.08	36.00	14.92	440	440	28	31.3	31.3
22.11	37.00	14.89	470	490	28	35.3	36.8
23.15	38.00	14.85	530	550	28	39.6	41.1
24.18	39.00	14.82	580	600	28	45.7	47.3
25.24	40.00	14.76	660	680	28	50.8	52.3
26.33	41.00	14.67	730	750	28	57.9	59.5
27.66	42.00	14.34	830	840	28	64.9	65.7
29.63	43.00	13.37	950	970	28	70.1	71.6
31.03	43.13	12.10	950	970	28	71.0	72.5

12.1 dB. Calculated peak PAE of the PA is between 71 and 72.5 % at the output power of 43.13 dBm. Gain varies from 15.1 dB to 12.1 dB. The quarter-wavelength bias line is used for gate and drain biasing to suppress the 2<sup>nd</sup> harmonic generated at the RF transistor.

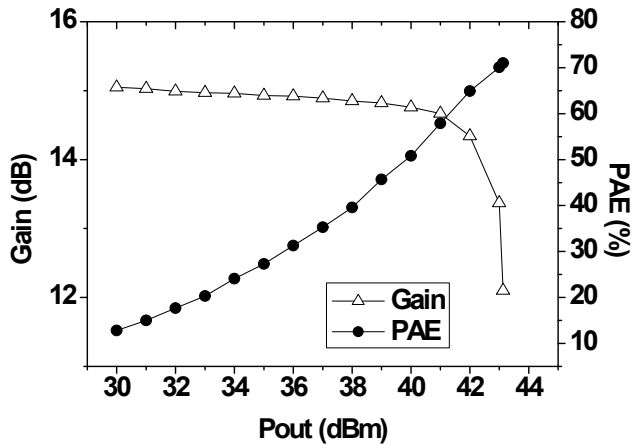


Figure 4.2: Large-signal measurement of gain and PAE over output power.

#### 4.1.2 Characterization of the Main Power Amplifier for Feedforward Application

To show the practical applicability of the proposed NGD with the high power base-station PA, commercially available PA manufactured by Sewon Teletech. Inc. is utilized as the MPA for the feedforward system. Fig. 4.3 shows the module photograph of STA0821-3940MM-MS. It has 120 W peak envelope output power and equipped with the digital predistortion and the automatic power shutdown feature. This MPA could operate up to a 49.18 dBm of the output power (laboratory measurement) with 54.8 dB of gain at 28 V as shown in Table 4.2, Fig. 4.4 and Fig. 4.5. Due to the automatic power shutdown feature to protect the device failure in case of overdrive, the amplifier was turned off when the higher input power was applied. It has 38.3 % of power added efficiency (PAE) at the peak power as shown in Fig.

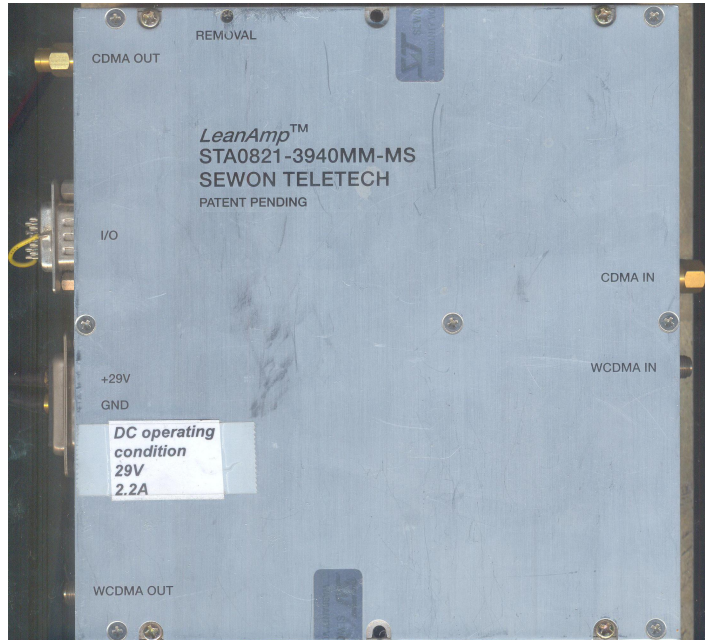


Figure 4.3: Photograph of the commercial base-station PA manufactured by Sewon Teletech, Inc. To use as a nonlinear PA, built-in digital predistortion function is disabled.

4.5. Digital predistortion features were turned off to be operated as a nonlinear high power amplifier (HPA). Adjacent channel leakage ratio (ACLR) characteristics were measured with the 2-carrier WCDMA signal. At the average output power of 45 dBm, ACLR was 33 dBc at the frequency offset of 5 MHz, as shown in Fig. 4.6.

TABLE 4.2: MEASUREMENT TABLE FOR CONTINUOUS WAVE SIGNAL.

STA0821-3940MM-MS							
CW sweep for Gain, PAE							
OBO	Pin	Pout	Gain	Ids	Vds	DE	PAE
19	-25.36	30.00	55.36	2310	29.0	1.5	1.5
18	-24.38	31.00	55.38	2340	29.0	1.9	1.9
17	-23.39	32.00	55.39	2380	29.0	2.3	2.3
16	-22.40	33.00	55.40	2440	29.0	2.8	2.8
15	-21.40	34.00	55.40	2510	29.0	3.5	3.5
14	-20.40	35.00	55.40	2580	29.0	4.2	4.2
13	-19.40	36.00	55.40	2700	29.0	5.1	5.1
12	-18.40	37.00	55.40	2830	29.0	6.1	6.1
11	-17.40	38.00	55.40	2970	29.0	7.3	7.3
10	-16.40	39.00	55.40	3140	29.0	8.7	8.7
9	-15.40	40.00	55.40	3340	29.0	10.3	10.3
8	-14.49	41.00	55.49	3580	29.0	12.1	12.1
7	-13.50	42.00	55.50	3860	29.0	14.2	14.2
6	-12.55	43.00	55.55	4180	29.0	16.5	16.5
5	-11.58	44.00	55.58	4550	29.0	19.0	19.0
4	-10.63	45.00	55.63	4950	29.0	22.0	22.0
3	-9.68	46.00	55.68	5420	29.0	25.3	25.3
2	-8.72	47.00	55.72	5970	29.0	28.9	28.9
1	-7.78	48.00	55.78	6580	29.0	33.1	33.1
0	-6.80	49.00	55.80	7320	29.0	37.4	37.4
0	-5.62	49.18	54.80	7450	29.0	38.3	38.3

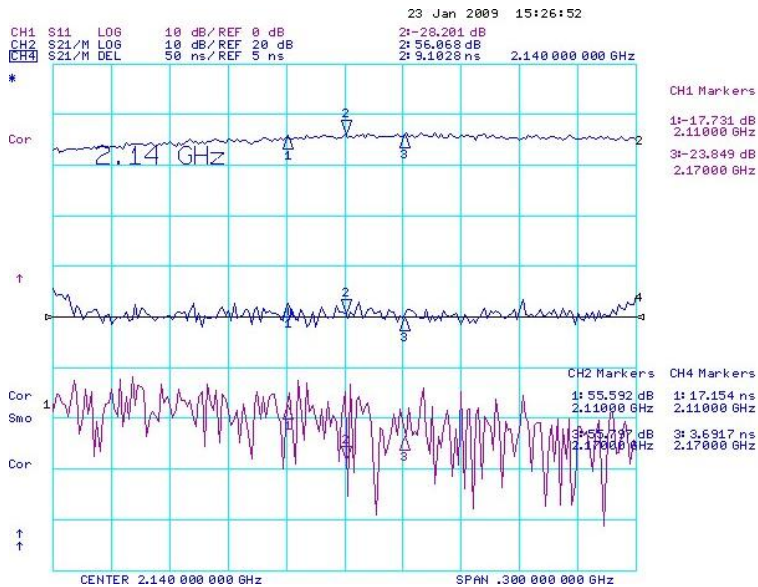


Figure 4.4: Small signal measurement of gain, return loss and group delay.

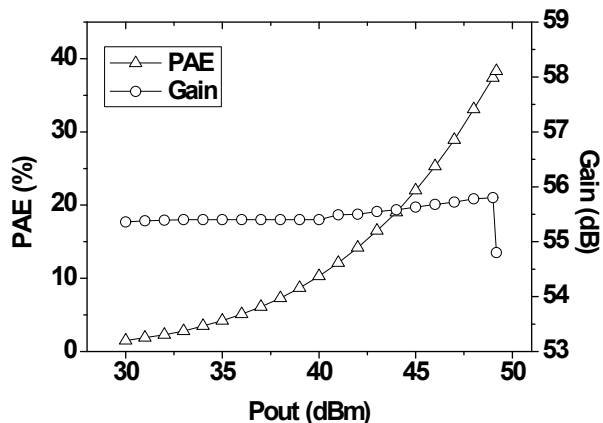


Figure 4.5: Measured gain and PAE versus output power. Abrupt gain drop is due to the automatic power-off feature of the commercial amplifier.

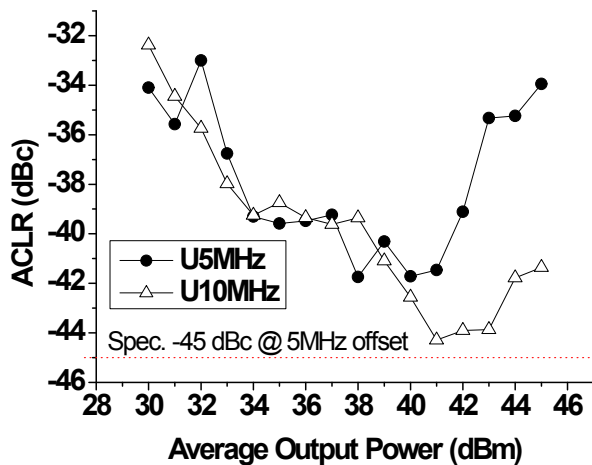


Figure 4.6: Measured ACLRs according to the average output power for 2-carrier WCDMA signal.

### 4.1.3 Design and Measurement of the Main Power Amplifier for Feedback Application

In this subsection, a size reduced quasi Class-E PA with compact defected ground structure (DGS) load-network is proposed and experimentally validated. To reduce the size and complexity of the conventional load-network while obtaining comparable harmonics suppression as well as high efficiency, DGS quarter-wavelength bias line and DGS transmission lines are employed as a load-network for the quasi Class-E operation. Experimental results including gain, output power, and PAE are presented for the optimum bias level and various input frequencies.

Generally, harmonic impedances seen at all the higher order harmonic frequencies should be open terminated at the current generation plane for the Class-E operation. Circuit schematic of Fig. 4.7 (a) shows the conventional transmission line load network for the Class-E PA. Typical transmission line load network consists of several open stubs to suppress higher order harmonics. Moreover,  $\lambda/4$  bias line, which is typically capable of suppressing 2<sup>nd</sup> harmonic, is generally used for most PAs instead of choke inductor due to power handling and memory effect compensating features, etc. If those distributed circuit elements are taken into consideration, integration with other circuit to a smaller size module may be a tough goal to achieve.

DGS is fabricated by etching a few geometrical patterns on the ground plane of the microstrip line. The main advantages of DGS can be summarized as follows: realization of high impedance transmission line typically unachievable due to physical limitation (e.g.,  $200 \Omega$ ), size reduction due to slow-wave effect, and enhancement of PA performance by harmonics suppression.

The proposed load network is presented in Fig. 4.7 (b). As an alternative to the several open stubs in the conventional circuit,  $\lambda/4$  bias line loaded with dumbbell shaped DGS that suppresses 2<sup>nd</sup> and 3<sup>rd</sup> harmonics, and series transmission line (electrical length= $50^\circ$ ) loaded with asymmetrical spiral shaped DGS units which terminates 4<sup>th</sup> and 5<sup>th</sup> harmonics are combined and included as a part of the output matching network. No additional line elements are inserted since DGS units are etched on the ground pattern of previously existing series lines and bias lines. Switching capacitance ( $C_{SW}$ ) is obtained from the load-pull simulation using high power device model since the output capacitance ( $C_{ds}$ ) of the device is not available.

Fig. 4.8 (a) illustrates the design procedure of asymmetric spiral DGS units in a series transmission line element. As for an asymmetric spiral DGS, total perimeter and the number of turn of one symmetric unit cell is inversely



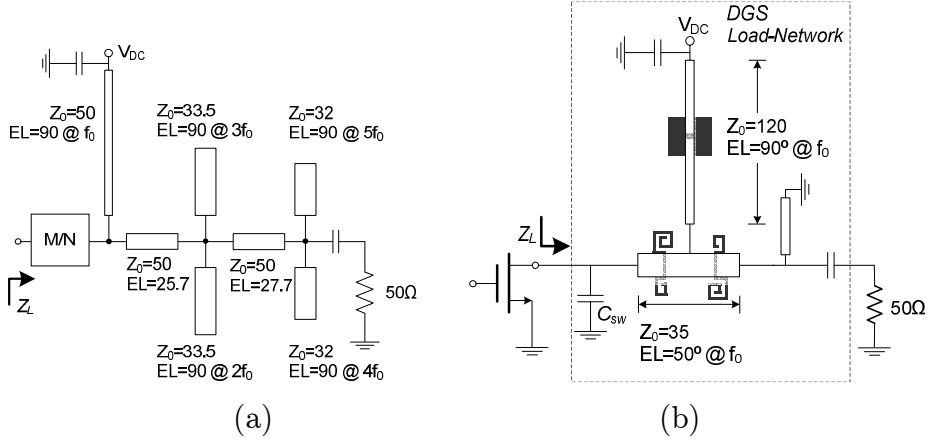


Figure 4.7: (a) Conventional transmission line load-network topology, and (b) the proposed DGS load-network for quasi Class-E PA.

proportional to the resonant frequency. Therefore, the resonance frequency of the smaller unit symmetric spiral DGS is first optimized to be equal to 5<sup>th</sup> harmonic frequency and the larger one to be tuned for 4<sup>th</sup> harmonic. By combining those two units in one cell, it is possible to obtain the desired dual-band suppression characteristic, as depicted in Fig. 4.8 (a). To broaden the cancellation bandwidth at 4<sup>th</sup> and 5<sup>th</sup> harmonic frequency, additional asymmetric unit cell with same perimeter was inserted as in Fig. 4.8 (c), and the desired performance could be obtained. Fig. 4.8 (b) and (c) shows the dimension of dumbbell and spiral shaped DGS optimized by 3D electromagnetic simulation using Ansoft HFSS v11. The surface current distribution at the fundamental and each harmonic frequency are illustrated in Fig. 4.8 (d). All the fundamental signals are transmitted to the output port. No

current exists at the input port for the 2<sup>nd</sup> harmonic, implying that it is open terminated through the combination of  $\lambda/4$  bias line and asymmetric spiral DGS transmission line. The current distribution is strong for the input of the 3<sup>rd</sup>, the 4<sup>th</sup>, and the 5<sup>th</sup> harmonic, implying zero impedance. No harmonic signal is transmitted to the output port at all.

EM simulation and measurement result of the DGS load-network is shown in Fig. 4.9. Up to 5<sup>th</sup> harmonics are considered in the design. RT/Duroid 5880 ( $\epsilon_r=2.2$ ) laminate of Rogers Corp. has been selected for this work.

As shown in Fig. 4.9 (a), noteworthy advantage of the proposed DGS load-network is its extremely low insertion loss, 0.05dB in this case, with comparable harmonic suppression of 37.2 dB, 26.7 dB, 49.5 dB, and 32.4 dB for the 2<sup>nd</sup>, 3<sup>rd</sup>, 4<sup>th</sup>, and 5<sup>th</sup> harmonics, respectively. Low insertion loss enables adoption of the proposed concept to the PA with higher output power. Fig. 4.9 (b) shows the EM simulated and measured impedances of the compact DGS load-network. This is why the proposed load network has been named ‘quasi Class-E’. Unlike infinite harmonic impedances observed from the typical Class-E PAs for proper switching operation ( $|Z_{\text{info}}| \approx \infty$ ,  $n=2\sim 5$ ), the proposed load-network rather provides near-open impedance for 2<sup>nd</sup> harmonic ( $Z_{2f_0} \approx \infty$ ), which is the dominant component, and reactive or near-zero impedance for other higher order minor harmonics for the power device

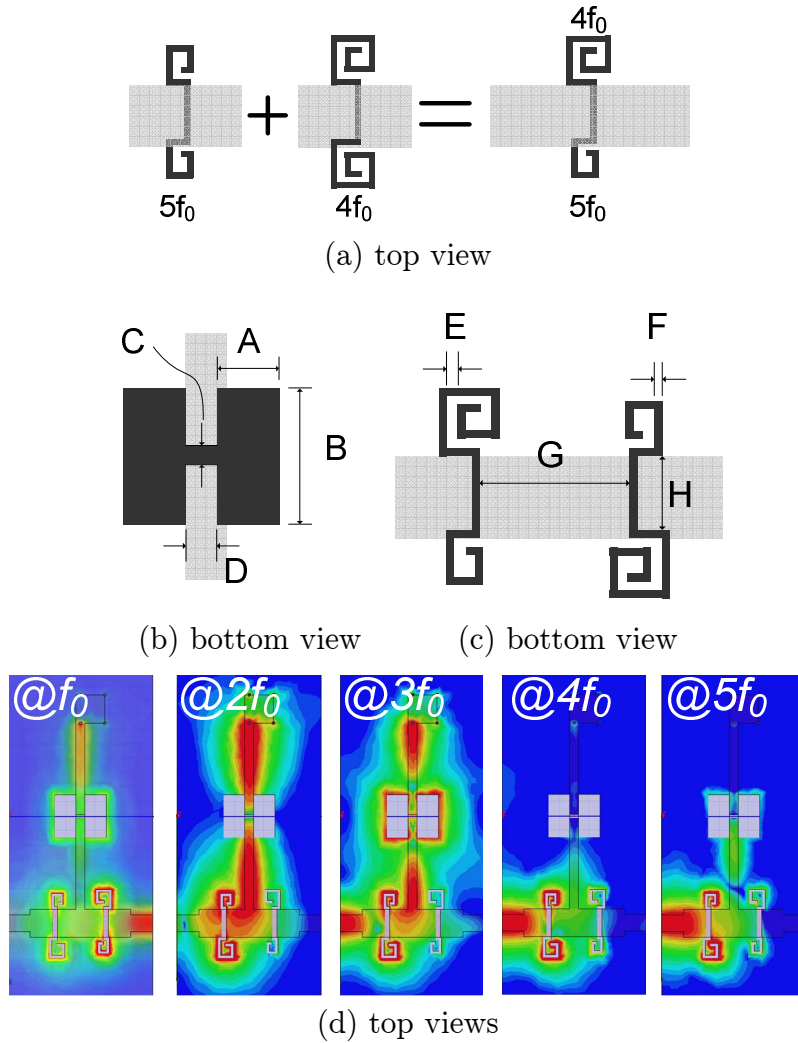


Figure 4.8: (a) Asymmetric spiral DGS design and physical dimension of the DGS units: (b) the dumbbell DGS ( $A=3$ ,  $B=5.9$ ,  $C=0.6$ , and  $D=1.2$  [mm]), (c) the spiral DGS ( $E=0.4$ ,  $F=0.4$ ,  $G=6.4$ , and  $H=4$  [mm]), and (d) the surface current distribution at the fundamental and harmonic frequencies (red: high density, blue: low density in colored version).

( $Z_{\text{info}} \approx 0$ ,  $n=3\sim 5$ ), without experiencing no performance degradation in terms of the efficiency.

A quasi Class-E PA was designed and implemented with GaN HEMT device NPTB00025 of Nitronex, which has a peak envelope power (PEP) of 25 W at the operation frequency of WCDMA base-station band ( $f_0=2.14$  GHz). From the load-pull simulation using the large signal model given by the manufacturer, the maximum achievable PAE was 70.96 % with the proposed DGS load network when the output power is 42.4 dBm. The switching capacitor ( $C_{SW}$ ) was determined as 0.68 pF from the load-pull simulation for the optimum performance.

For comparison, reference Class-AB amplifier was also implemented with the bias condition of  $V_{DS}=28$  V and  $I_{DS}=225$  mA for the same transistor. The optimum load impedance ( $Z_{Lopt}$ ) for Class-AB operation was  $7.65-j0.68 \Omega$ . The saturated output power and peak PAE of Class AB amplifier was 43.9 dBm and 58.5 % with power gain of 12.6 dB. For the proposed Class-E PA, saturated output power was 43.1 dBm with the power gain of 12.7 dB and the linear gain of 16.2 dB, as illustrated in Fig. 4.10. The maximum drain efficiency (DE) and PAE were 74.1 % and 70.2 %, respectively, which showed good agreement with the load-pull simulation.

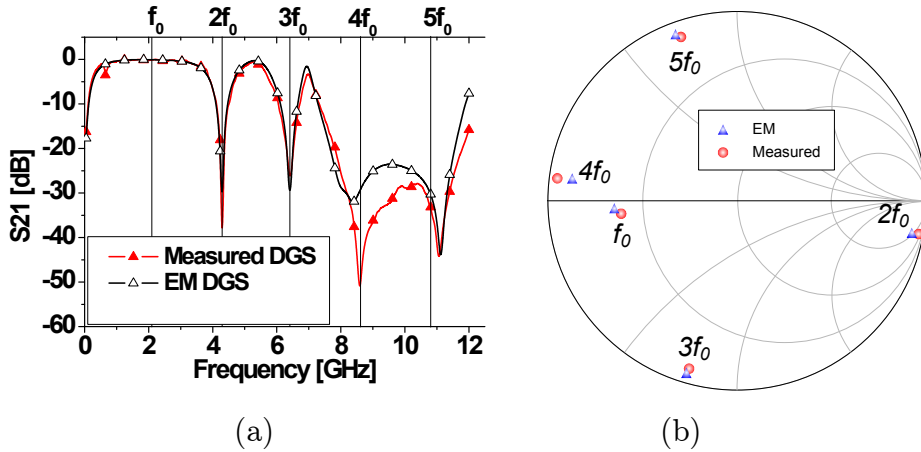


Figure 4.9: EM simulation and measurement result: (a) 2-port transmission characteristics, and (b) 1-port input impedances of the proposed DGS load network.

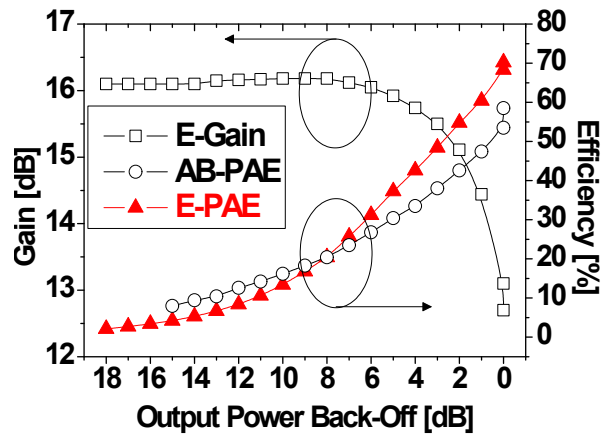


Figure 4.10: Measured gain (E-Gain) and efficiency (E-PAE for quasi Class-E PA, AB-PAE for Class-AB PA) according to output power back-off.

Fig. 4.11 shows the measured output power and PAE according to the drain bias voltages for 30 dBm input power when  $V_{GS}$  was fixed to -1.2 V. For drain bias variation,  $V_{DS}=30\pm 6$  V, PAE is maintained over 63 % and the peak PAE of 70.2 % was obtained when  $V_{DS}=27.5$  V. It is shown in Fig. 4.12 that the measured output power and PAE with respect to various gate bias voltages for 30 dBm input power when  $V_{DS}$  was fixed to 27.5 V. For gate bias variation,  $V_{GS}=-1.2\pm 0.7$  V, PAE was maintained as over 65 % and the peak PAE of 70.2 % was obtained when  $V_{GS}=-1.2$  V. This also implies that the thermal variation does not have a critical effect on the efficiency performance of the proposed PA based on the fact that the increased device temperature may induce degradation.

Fig. 4.13 shows the measured output power and PAE over various input frequencies. For the entire bandwidth of WCDMA base-station (2.11~2.17 GHz), overall PAE was over 60 %, achieving maximum PAE of 70.2 % at the center frequency of 2.14 GHz when the output power was 43.1 dBm.

Measured higher order harmonic power levels are shown in Fig. 4.14. Harmonics are suppressed well below 46dBc for 2<sup>nd</sup> harmonic and 52 dBc for 3<sup>rd</sup>, 4<sup>th</sup>, and 5<sup>th</sup> harmonics through the 8dB output dynamic range. Since the Class-E PA is operated in a heavy saturation mode as 3dB gain saturation, harmonic levels are gradually increasing at higher output power,

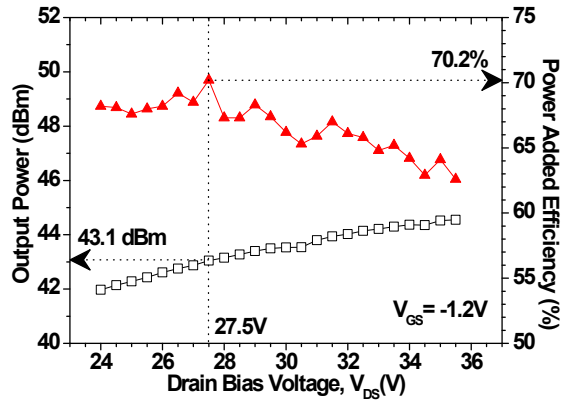


Figure 4.11: Output power and PAE with respect to drain bias voltage.

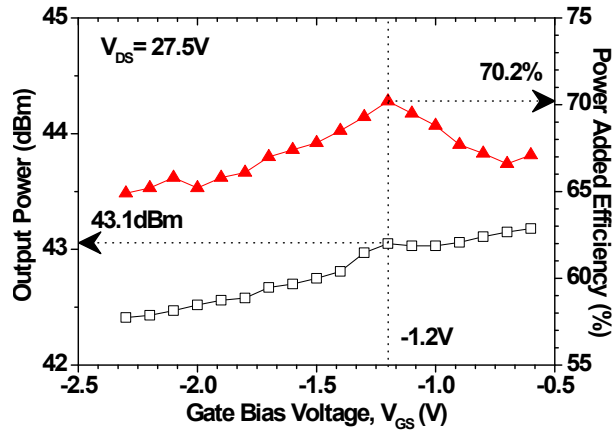


Figure 4.12: Output power and PAE with respect to gate bias voltage.

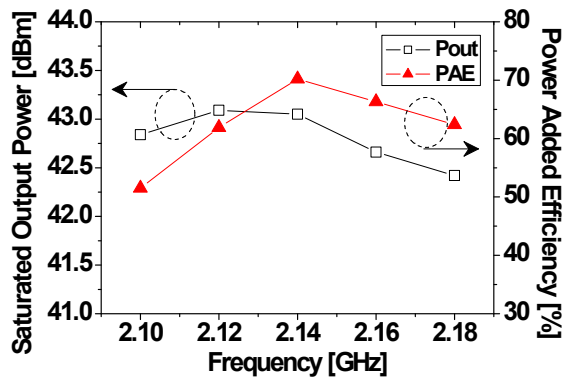


Figure 4.13: Measured output power and PAE for various input CW frequency.

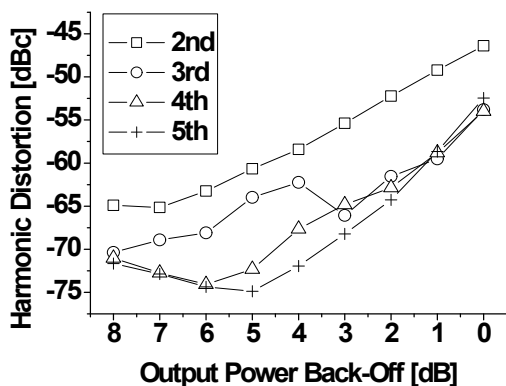


Figure 4.14: Measured higher order harmonics level relative to fundamental output power.

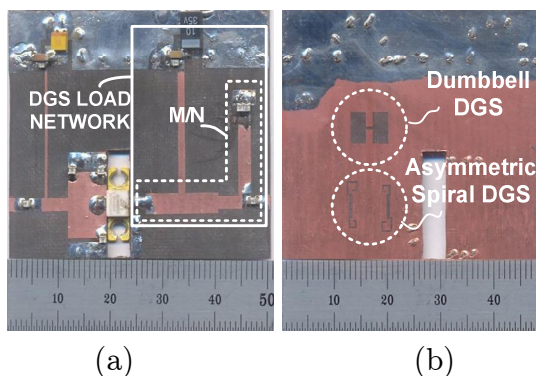


Figure 4.15: Photographs of the fabricated quasi Class-E PA with DGS load network: (a) top and (b) bottom view.

even though the relative level to the fundamental output power is pretty low.

Photographs of the fabricated quasi Class-E PA with compact DGS load-network are presented in Fig. 4.15. Total size of the fabricated PA occupies  $50 \times 50 \text{ mm}^2$ , including the input and output matching networks. If the focus is limited to the output load network, the size reduction would be much more evident.



## ***4.2 Efficiency Enhancement of Feedforward Linear Power Amplifiers by Employing a Negative Group Delay Circuit***

### **4.2.1 Principle of Operation**

Fig. 4.16 illustrates the two types of feedforward amplifiers employing the NGD circuit proposed in this work. The NGD circuit and a band-pass filter (BPF) are added in the conventional feedforward structure. The BPF is used to avoid any unwanted oscillation in forward loops.

In Fig. 4.16 (a), the NGD circuit is placed in the EPA path and counterbalances the group delay time experienced by the EPA path including the vector modulator, the EPA, and other coupling devices. In that way, the delay element (DELAY 2) at the output of the MPA can be eliminated. In this case, the eliminated delay element gives us an efficiency enhancement for the feedforward amplifier without affecting the carrier suppression loop.

In Fig. 4.16 (b), the NGD circuit is inserted into the common path of the two loops. Therefore the delay elements from the carrier suppression loop (DELAY 1) as well as the IMD suppression loop (DELAY 2) can be reduced or eliminated. If the group delays of the MPA and the EPA path are same, the complete elimination of the two delay elements is possible, therefore enhancing the efficiency and minimizing the total size of the feedforward system. Even though the delay element is eliminated, additional power

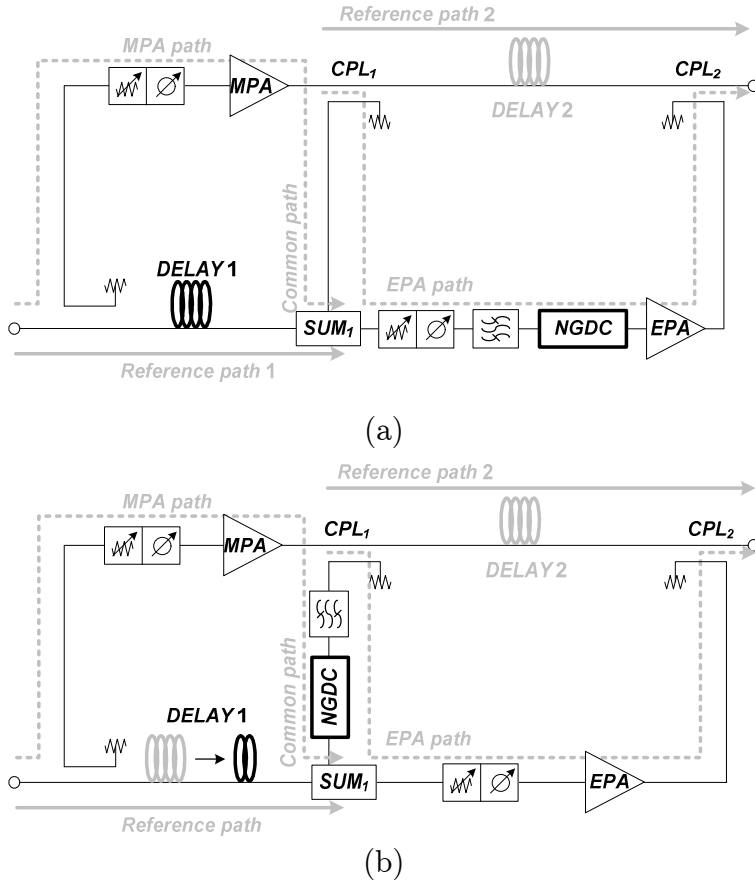


Figure 4.16: Proposed novel feedforward amplifier topologies with NGD circuit employed at: (a) EPA path and (b) common path.

consuming circuits must be added to the NGD circuit. However, an important difference is that the newly adopted NGD circuit consumes a very small DC power as compared to the power lost by the lossy delay elements. Also the NGD circuit is able to be integrated in the EPA module, while the delay elements are typically composed of bulky delay line filters or high power coaxial cables with the inevitable size, weight, and cost penalty. In this work, the topology of Fig. 4.16 (b) is chosen.

## 4.2.2 Feedforward Loop Suppression Analysis

Fig. 4.17 shows a simple signal suppression loop model representing the amplitude, out-of-phase, and group delay mismatches. A portion of the input signal ( $V_{IN}$ ) is coupled into the delay path as a reference signal ( $V_A$ ). The remaining portion of the  $V_{IN}$  is amplified by the PA resulting in the amplified carrier with IMD components. A portion of the output of PA ( $V_B$ ) is then coupled into the subtraction circuit, which is then destructively combined with the  $V_A$ , generating an error signal ( $V_{ERR}$ ) that theoretically does not include any carrier components.

1) Amplitude and out-of-phase mismatch: When the reference signal of a sinusoidal waveform having amplitude ( $V_1$ ) and phase ( $\theta$ ) is combined with the signal that includes the amplitude mismatch factor ( $\Delta V$ ) and the out-of-phase mismatch factor ( $\Delta\theta$ ), the resultant carrier suppressed signal can be represented as a ratio of the average power of  $V_{ERR}$  to  $V_A$ .

$$S \text{ (dB)} = 10 \log \left[ 1 + \left( \frac{V_1 + \Delta V}{V_1} \right)^2 - 2 \left( \frac{V_1 + \Delta V}{V_1} \right) \cdot \cos(\Delta\theta) \right] \quad (4-1)$$

Fig. 4.18 shows the calculated loop suppression performance expressed as a function of an amplitude mismatch of  $\pm 0.2$  dB and an out-of-phase mismatch of  $\pm 1^\circ$ . From the figure, this mismatching range leads to a loop suppression of 30 dB, where the group delay mismatch is assumed to be zero in this analysis.

2) Group delay mismatch: The group delay mismatch ( $\Delta t$ ) between the paths is critical for broadband signal suppression as shown in Fig. 4.19. For our analysis, a unit amplitude ( $V_1=1$ ) and a perfectly matched amplitude and out-of-phase condition ( $\Delta V=\Delta\theta=0$ ) were assumed.  $V_{ERR}$  can be expressed as follows where  $\omega_0$  is an angular frequency:

$$\begin{aligned}
 V_{ERR} &= V_A + V_B \\
 &= \cos(\omega_0 t + \theta) + \cos(\omega_0(t + \Delta t) + \theta + 180^\circ) \\
 &= \cos(\omega_0 t + \theta)(1 - \cos(\omega_0 \Delta t)) + \sin(\omega_0 t + \theta) \sin(\omega_0 \Delta t)
 \end{aligned} \tag{4-2}$$

To calculate the average power over one period,  $|V_{ERR}|^2$  can be obtained by using (4-2).

$$\begin{aligned}
 |V_{ERR}|^2 &= \left| \frac{(1 - \cos \omega_0 \Delta t)^2 + (1 - \cos \omega_0 \Delta t)^2 \cos 2(\omega_0 t + \theta)}{2} \right. \\
 &\quad \left. + \frac{\sin^2(\omega_0 \Delta t) + \sin^2(\omega_0 \Delta t) \sin^2(\omega_0 t + \theta)}{2} \right. \\
 &\quad \left. + \sin 2(\omega_0 t + \theta)(1 - \cos \omega_0 \Delta t)(\sin \omega_0 \Delta t) \right|
 \end{aligned} \tag{4-3}$$

By taking an integral of (4-3) over an arbitrary period  $T_0$ , the average power of  $V_{ERR}$  is given by (4-4).

$$P_{ERR,avg} = 1 - \cos \omega_0 \Delta t \tag{4-4}$$

Since the ratio of (4-4) to the average power of the  $V_A$  ( $P_A=1/2$ ) is defined as the loop suppression, the loop suppression can be expressed in a dB scale for a time mismatching condition as shown in (4-5):

$$S_{\Delta} = 10 \log(1 - (\cos(\omega_0 \Delta t)) \cdot (1 - f / f_0)) + 3 \tag{4-5}$$

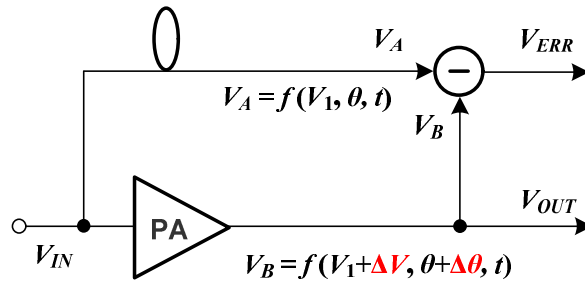


Figure 4.17: Simple signal suppression loop model considering amplitude ( $\Delta V$ ) and phase mismatch ( $\Delta \theta$ ).

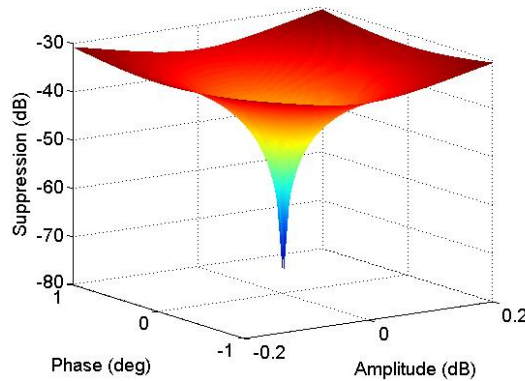


Figure 4.18: Loop suppression expressed as a function of amplitude and phase mismatch.

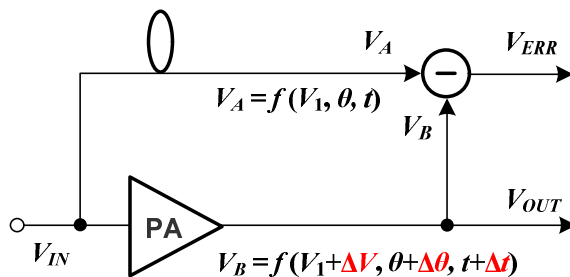


Figure 4.19: Simple signal suppression loop model considering group delay mismatch ( $\Delta t$ ) as well as amplitude ( $\Delta V$ ) and phase mismatch ( $\Delta \theta$ ).

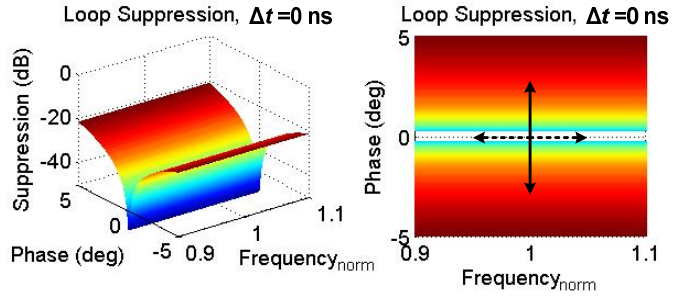
where the term  $1-f/f_0$  is inserted to derive the equation with respect to the normalized frequency while  $f_0$  represents the center frequency.

Finally, from (4-1) and (4-5) the loop suppression equation considering the amplitude, out-of-phase and delay mismatches can be derived as a function of time ( $\Delta t$ ).

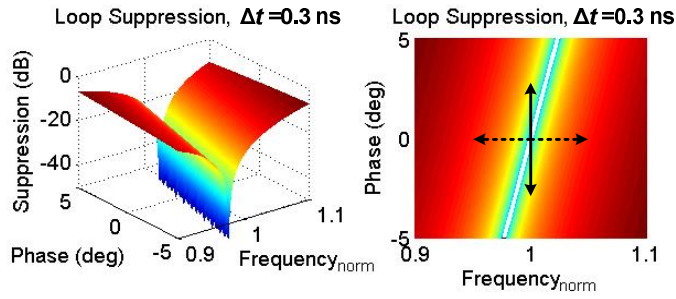
$$S_{total} = 10 \log \left[ 1 + \left( \frac{V_1 + \Delta V}{V_1} \right)^2 - 2 \left( \frac{V_1 + \Delta V}{V_1} \right) \cdot \cos(\omega_0 \Delta t) \left( 1 - \frac{f}{f_0} \right) \right] \quad (4-6)$$

Fig. 4.20 shows the loop suppression performance with and without the presence of a delay mismatch for 0.01 dB of fixed amplitude mismatch. In the case there is no delay mismatch as shown in Fig. 4.20 (a), the loop suppression performance is only limited by the out-of-phase mismatch, not by the frequency, as the dotted arrow direction designates. However, in the presence of 0.3 ns of delay mismatch, the amount of the loop suppression performance is limited both by the phase (solid line) and the normalized frequency (dotted line), as shown in Fig. 4.20 (b).

Fig. 4.21 shows the calculated and the simulated loop suppression performance, with respect to the normalized frequency, for a different delay mismatch when there is 0.01 dB of amplitude mismatch with no phase mismatch. The mathematical estimation closely agrees with the circuit simulation by using ADS2009. In case of 0.3 ns of the group delay mismatch,



(a)



(b)

Figure 4.20: Loop suppression performance expressed as a function of phase and group delay mismatch when: (a)  $\Delta t=0$  ns and (b)  $\Delta t=0.3$  ns (at fixed amplitude mismatch of 0.01 dB).

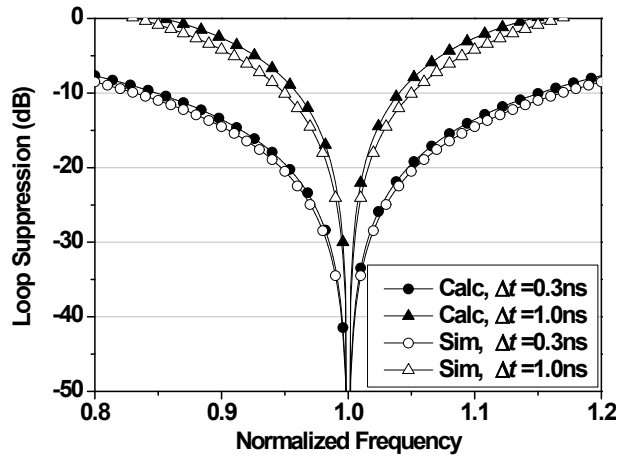


Figure 4.21: Calculated and simulated loop suppression performance expressed as a function of normalized frequency for different time mismatching values.

it is expected that the fractional bandwidth of 20 dB cancellation will be 5.2 %. When the mismatch is 1.0 ns, the bandwidth is considerably decreased to 1.6 %, nearly 30% of the bandwidth for 0.3 ns mismatch.

### 4.2.3 Experimental Setup

The linearity specification for the base-station amplifier is -45 dBc for 5 MHz of frequency offset. The ACLR level of the MPA without the feedforward system was -33 dBc at an average output power of 44 dBm. Then the power level of the nonlinear portion of the output signal is 11 dBm. If 10 dB coupling ratio is selected for an error injection coupler (CPL<sub>2</sub> shown in Fig. 4.16 (b)), the EPA should be linear at an average output power of 21 dBm. From section 4.1.1, the fabricated PA has output power of over 43 dBm. There is a 22 dB back-off margin between the average power and the peak power in the EPA for purely linear operation. But the overall efficiency would be decreased by this over-specification power capability. Before the mass production stage, the power level matching between the MPA and EPA should be performed to optimize the system efficiency. Fig. 4.23 shows the current EPA line up for the feedforward amplifier for prototype lab measurement.



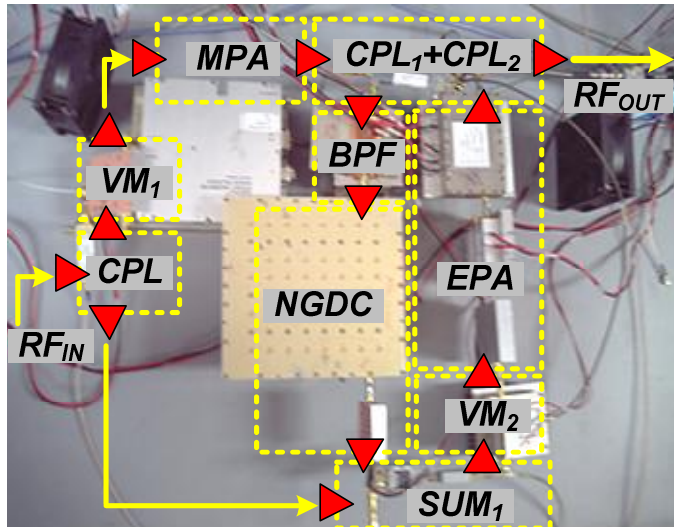


Figure 4.22: Photograph of the proposed feedforward topology ( $VM_1$  and  $VM_2$  refers to the vector modulator).

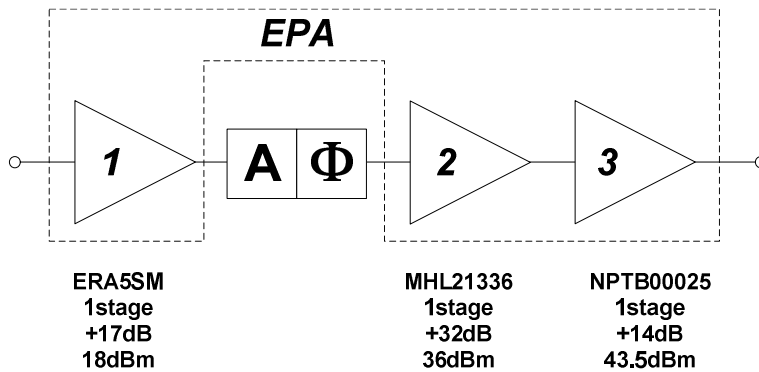


Figure 4.23: EPA line-up for feedforward amplifier as a prototype lab measurement.

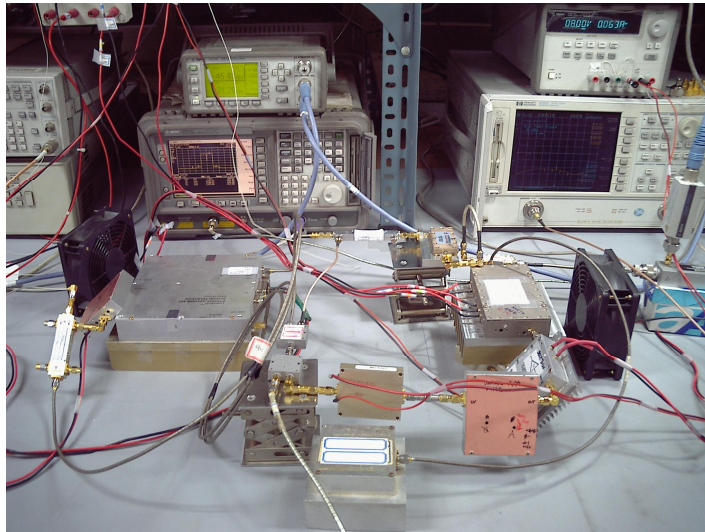


Figure 4.24: Test setup.

Due to the frequency response of the employed NGD circuit, which amplified the unwanted out-of-band noise, the 2-stage quarter-wavelength coupled line BPF was designed with a microstrip line and integrated in front of the NGD circuit to avoid possible instabilities. Addition of narrow band BPF increases the total group delay of the EPA path by 2.5 ns, and this factor has already been considered in the design of the NGD circuit in the previous section. Test setup is illustrated in Fig. 4.24.

#### 4.2.4 Measurement Results

Fig. 4.25 and Fig. 4.26 show the measured level of carrier suppression in the first loop of the proposed feedforward system by using CW and WCDMA

signal. For the carrier bandwidth of the 2-carrier WCDMA signal, at about 10 MHz, at least 32.8 dB of carrier suppression was obtained. Measured intermodulation distortion suppression loop characteristic is shown in Fig. 4.27. Regarding the adjacent channel bandwidth into account for the IMD suppression loop, over 19.2 dB of adjacent channel leakage ratio (ACLR) improvement was expected to be achieved for 30 MHz.

Measured data of DC power consumption, gain, ACLRs before and after the feedforward linearization employing the NGD circuit is shown in Table 4.3 and Table 4.4. Fig. 4.28 shows the measured spectrum of the fabricated feedforward amplifier for a 2-carrier WCDMA signal at an average output power of 43 dBm. The ACLR improvement was almost 20 dB from -36.6 dBc to -56.6 dBc at a 5 MHz offset.

Fig. 4.29 illustrates the measured ACLR before and after linearization for an 8 dB output dynamic range. Optimized for 43 dBm of the output power, the fabricated system achieved at least -53 dBc of the ACLR at a 5 MHz offset for an output power of 37 dBm to 44 dBm.

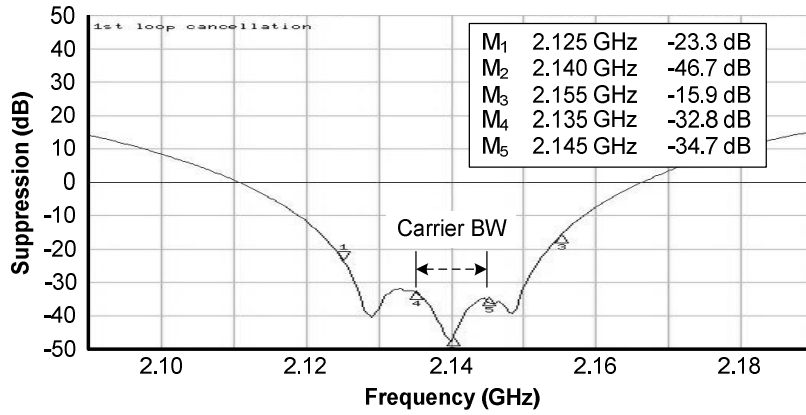


Figure 4.25: Measured carrier suppression loop characteristic.

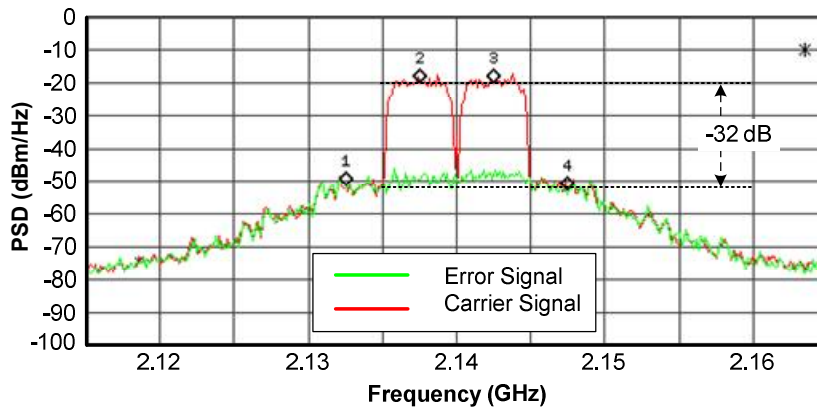


Figure 4.26: Measured 2-carrier WCDMA spectra before (Carrier Signal) and after (Error Signal) carrier suppression.

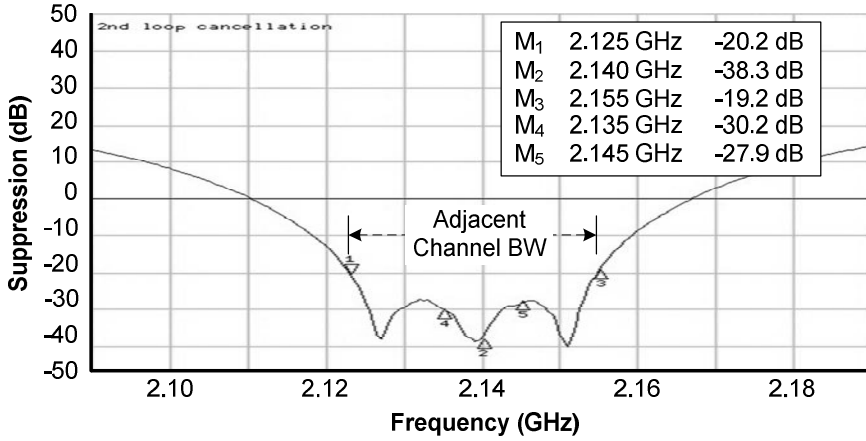


Figure 4.27: Measured intermodulation distortion suppression loop characteristic.

TABLE 4.3: MEASUREMENT TABLE FOR 2-CARRIER WCDMA SIGNAL BEFORE LINEARIZATION.

NGDC FFW ACLR without Loop																	
Backoff from P1dB	Pin_avg [dBm]	Pout_avg [dBm]	2.1425 [dBm]	L10 [dBm]	L5 [dBm]	U5 [dBm]	U10 [dBm]	V1 [V]	I1 [A]	V2 [V]	I2 [A]	V3 [V]	I3 [A]	V4 [V]	I4 [A]	DE [%]	PAE [%]
		44	13.73	-32.80	-22.29	-22.96	-33.20										
		43	11.77	-34.87	-26.24	-26.28	-35.12										
		42	11.32	-38.86	-29.44	-29.28	-38.41										
		41	10.98	-41.14	-32.97	-33.46	-41.20										
		40	9.20	-42.75	-37.74	-38.48	-42.65										
		39	8.87	-45.56	-38.85	-39.42	-45.41										
		38	7.65	-44.87	-42.46	-41.94	-45.10										
		37	6.66	-47.27	-44.57	-44.35	-47.31										

TABLE 4.4: MEASUREMENT TABLE FOR 2-CARRIER WCDMA SIGNAL AFTER LINEARIZATION.

NGDC FFW ACLR with Loop																	
Backoff from P1dB	Pin_avg [dBm]	Pout_avg [dBm]	2.1425 [dBm]	L10 [dBm]	L5 [dBm]	U5 [dBm]	U10 [dBm]	V1 [V]	I1 [mA]	V2 [V]	I2 [mA]	V3 [V]	I3 [mA]	V4 [V]	I4 [mA]	DE [%]	PAE [%]
5	9.45	44	13.41	-44.26	-39.79	-40.90	-45.27	29	3910	25	482	8	195	5	427	19.5	19.4
6	8.57	43	13.32	-45.65	-43.26	-43.53	-46.27	29	3780	25	482	8	195	5	427	15.9	15.9
7	7.65	42	12.32	-46.48	-43.05	-41.59	-46.02	29	3650	25	482	8	195	5	427	13.0	13.0
8	6.64	41	11.40	-47.70	-42.73	-44.09	-47.41	29	3480	25	482	8	195	5	427	10.8	10.8
9	5.72	40	11.01	-46.61	-44.11	-43.68	-45.51	29	3350	25	482	8	195	5	427	8.9	8.9
10	4.79	39	10.09	-47.65	-44.80	-43.87	-46.53	29	3240	25	482	8	195	5	427	7.2	7.2
11	3.89	38	9.30	-46.37	-45.19	-44.43	-46.76	29	3150	25	482	8	195	5	427	5.9	5.9
12	2.93	37	8.35	-46.69	-45.11	-46.36	-45.51	29	3080	25	482	8	195	5	427	4.8	4.8

The measured ACLR and PAE performance with respect to the average output power is presented in Fig. 4.30. At the output power of 43 dBm, the ACLR was -56.6 dBc and PAE was 17 %. At the average output power of 44 dBm, the measured ACLR and PAE (or drain efficiency) were -53.2 dBc and 19.4 % (or 19.5 %), respectively. This included the additional power consumption of the NGD circuit. For the MPA, the ACLR and PAE was -53.2 dBc and 5.1 %, respectively, at an average output power of 36 dBm. For the same ACLR level with and without the proposed feedforward topology, PAE of the system is increased from 5.1 % to 19.4 %. Also, considering -53.2 dBc of ACLR as a reference, the available output power for the MPA is increased from 36 dBm to 44 dBm.

In detail, the group delay difference between the conventional and the proposed structure is summarized in Table 4.5. DELAY1 and DELAY2 denote the delay elements at the reference path 1 (carrier suppression loop) and the reference path 2 (IMD suppression loop) shown in Fig. 4.16, respectively. The total compensating group delay of 8.9 ns required at the output of the MPA is reduced to 1.2 ns, 13.5% of the initial value. This value is the minimum experimentally achievable group delay in the feedforward technique for the laboratory experiment, which is generated by the signal

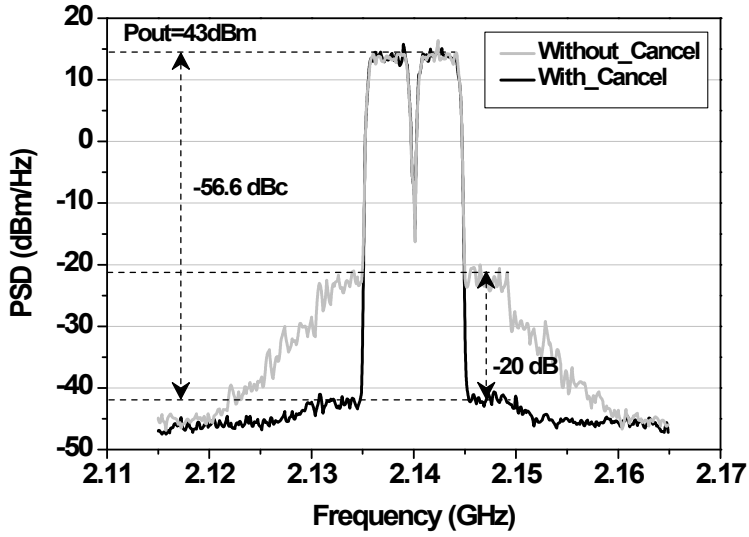


Figure 4.28: Measured 2-carrier WCDMA spectra before and after linearization at an average output power of 43 dBm.

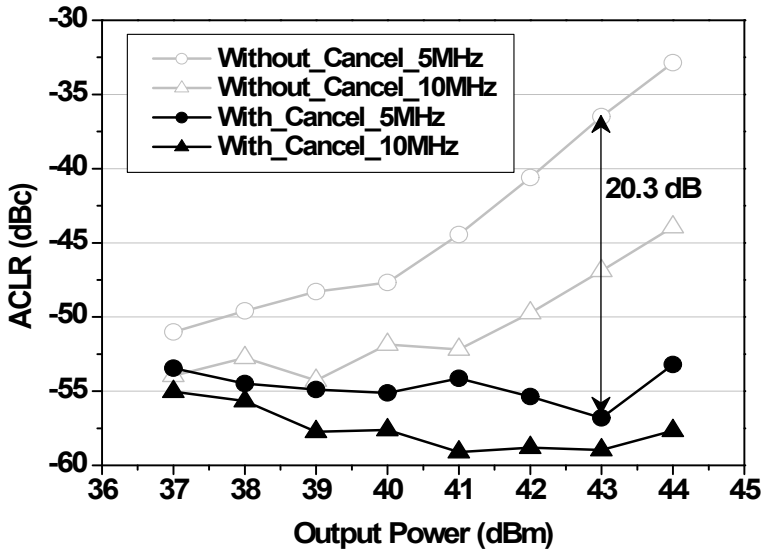


Figure 4.29: Measured ACLR with respect to 2-carrier WCDMA signal at 5MHz and 10MHz offset.

coupling and the error injecting coupler with the minimum connecting element.

Fig. 4.31 shows the output spectra when a 4-carrier WCDMA signal was applied to the proposed system. As observed in Fig. 4.31, in spite of the fact that the employed NGD circuit had 30 MHz of bandwidth, the linearization effect beyond the 30 MHz bandwidth could be achieved. For a 40 MHz bandwidth, the measured ACLR at a 10 MHz offset is nearly -50 dBc.

Also, DELAY1 is reduced from 11.6 ns to 4.1 ns. The measured results and the performance comparisons among feedforward amplifiers are summarized in Table 4.6. Systems using a 2-tone test signal can easily obtain a relatively high efficiency due to the low peak to average power ratio, since the amplifier can be driven into a near-saturation level. However, in the case of transmitting a broadband modulated signal, higher efficiency is a difficult goal to achieve due to the high peak-to-average power ratio (PAPR) of the signal. The 19.5 % of drain efficiency is the best result achieved with the feedforward amplifier at the time of this writing, according to the authors' best knowledge. This noticeable efficiency improvement is achieved by totally eliminating the delay element at the output of the MPA. If the output power of a given MPA is higher than what was used in this study, a few kW for



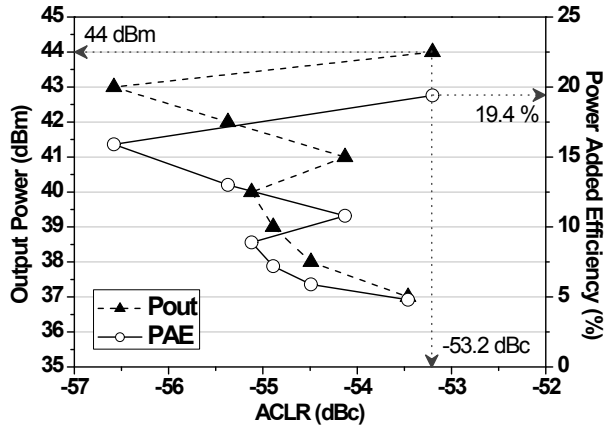


Figure 4.30: Measured ACLR and power added efficiency performance with respect to the average output power.

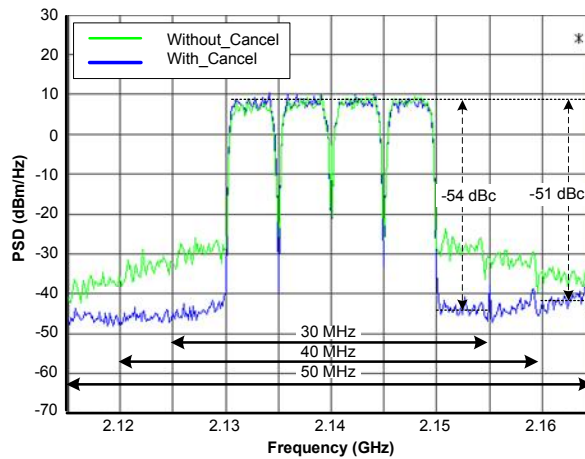


Figure 4.31: Measured 4-carrier WCDMA spectra before and after linearization.

TABLE 4.5: GROUP DELAY COMPARISON

	DELAY1 (ns)	DELAY2 (ns)
Conventional	11.6	8.9
This work	4.1	1.2

TABLE 4.6: MEASUREMENT SUMMARY AND PERFORMANCE COMPARISON  
AMONG FEEDFORWARD AMPLIFIERS

	Frequency (GHz)	Pout (dBm)	Test Signal	Signal BW (MHz)	Linearity (dBc)	Drain Efficiency (%)
[11]	1.97	<u>46.6</u>	CDMA	3.75	<u>-52</u>	7
[50]	0.56	41	2-tone	2	<u>-65</u>	12
[20]	<u>2.14</u>	<u>46.5</u>	<u>WCDMA</u>	<u>10</u>	<u>-55</u>	13.6
[21]	<u>2.14</u>	26	2-tone	-	-	12
[22]	0.22	40	2-tone	0.05	-35	27
[23]	0.22	40	2-tone	0.05	-32	33
[24]	<u>2.12</u>	<u>45.6</u>	<u>WCDMA</u>	-	< -50	10
<b>This work</b>	<b><u>2.14</u></b>	<b><u>44</u></b>	<b><u>WCDMA</u></b>	<b><u>10</u></b>	<b><u>-53</u></b>	<b><u>19.5</u></b>

example, then the efficiency enhancement will be much more evident since the effect of additional DC power consumption due to the small signal amplifier in the NGD circuit will be negligible when compared with the power consumption of delay elements.

#### 4.2.5 Summary and Discussion

An alternative topology was proposed for the feedforward amplifiers that yield substantial efficiency enhancement and size reduction by employing a DE NGD circuit. The design procedure and considerations for the DE NGD circuit were discussed. With the fabricated 2-stage DE NGD circuit with a 30 MHz bandwidth for a WCDMA downlink band, the feedforward amplifier of

the proposed topology experimentally achieved the highest efficiency among those previously reported in the literature, with additional advantages as to size and cost reduction.

Among the various linearization techniques used for a base-station transmitter, although old-fashioned, the feedforward method still has many advantages over DPD techniques, including all RF linearization, and immunity to long-term memory effects. The proposed topology is thought to be especially suitable for a system with a lower frequency of operation, where the physical size of the delay element is relatively large for the system. In addition, when this technique is applied to the high power systems with a few kW, additional efficiency, size, and cost improvements may be fairly realized.

### ***4.3 Bandwidth Enhancement of Feedback Linear Power Amplifiers by Employing a Negative Group Delay Circuit***

#### **4.3.1 Principle of Operation**

Fig. 4.32 illustrates the proposed feedback amplifier employing the NGD circuit, which consists of the  $MPA_{FB}$ , the  $EPA_{FB}$ , the vector modulators, an input coupler, an error injection coupler, the output sampling coupler, the BPF, and the NGD circuit. In the first instance, a portion of the input signal ( $RF_{IN}$ ) is applied to the  $MPA_{FB}$  and experiences the full gain of the amplifier.

Secondly, the remaining input signal is used as a reference ( $A$ ) against which a portion of the amplified output signal ( $B$ ) is compared. Any difference between the reference signal and the output signal, due to noise or distortion, is identified as an error signal ( $C$ ). The error signal is amplified in a separate  $EPA_{FB}$ , and then injected ( $D$ ) into the input port of the  $MPA_{FB}$  in phase in order to generate the error-free  $RF_{OUT}$ . The graphical representation of the test signals and nonlinear distortions shown in Fig. 4.32 are derived from the open loop condition. Due to the feedback path delay, which consists of the sum of the  $MPA_{FB}$ , the output sampling coupler, the BPF, the carrier cancellation circuit, and the vector modulator, plus an additional delay of  $\pi$  radians at the center frequency, the system bandwidth is fairly limited. By introducing the NGD circuit into the feedback loop between the output sampling coupler and the BPF, the feedback path delay can be controlled to increase the cancellation bandwidth. Fig. 4.33 is an alternative circuit schematic of Fig. 4.32. The error signal injection node ( $C$ ) is moved to the front of the reference signal coupler.

Fractional bandwidth variation for loop suppression of 20 dB with respect to the group delay mismatch is illustrated in Fig. 4.34. In case of the 0.3 ns group delay mismatch, it is expected that the fractional bandwidth for a 20 dB cancellation will be 5.2 %. When the mismatch is 1.0 ns, the bandwidth is

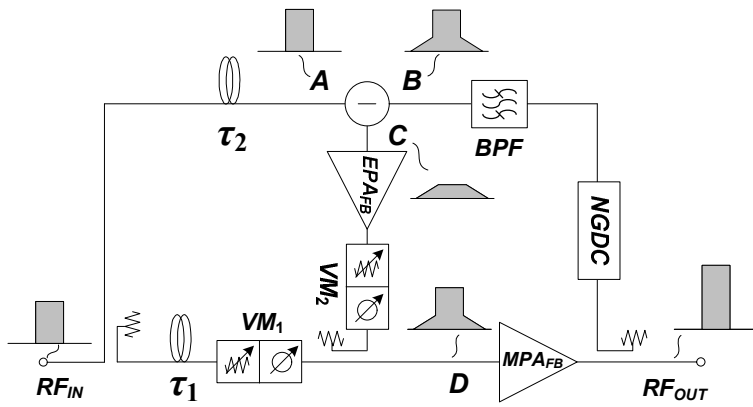


Figure 4.32: The block diagram of the proposed feedback amplifier.

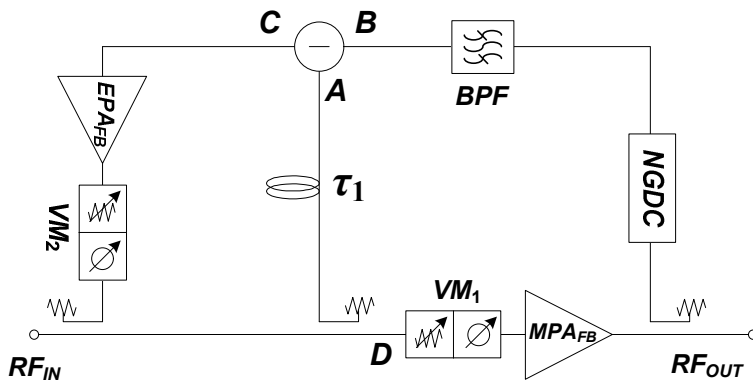


Figure 4.33: Alternative circuit schematic of Figure 4.32. The error signal injection node ( $C$ ) is moved to the front of the reference signal coupler.

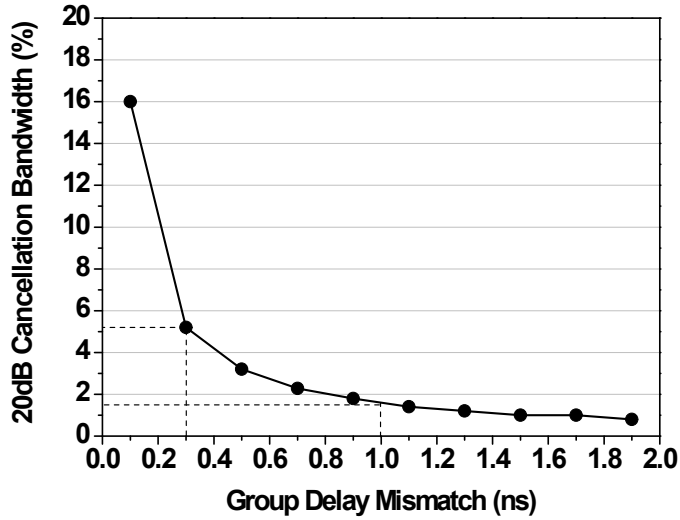


Figure 4.34: Calculated fractional bandwidth for loop suppression of 20 dB according to the group delay mismatch.

considerably reduced to 1.6 %. The cancellation bandwidth is reduced to 30 % of the bandwidth for a 0.3 ns mismatch.

### 4.3.2 Experimental Setup

The MPA of the proposed feedback amplifier was fabricated with a NPTB00025, GaN HEMT device with a peak envelope power of 25 W. The  $MPA_{FB}$  is operated by quasi Class-E with a gate bias voltage of -1.9 V and driven by an MHL21336 made by Freescale. This  $MPA_{FB}$  could operate up to a 43.1 dBm of the output power (laboratory measurement) with a gain of 50 dB at 28 V. It had 70.1 % power added efficiency at the peak output power. Due to the frequency response of the employed NGD circuit, which also

amplified the unwanted out-of-band noise, the 2-stage quarter-wavelength coupled line BPF was designed with a microstrip line and integrated in the feedback loop to avoid possible instabilities. An adoption of the narrow band BPF increased the total group delay of the feedback path by 2.5 ns; this factor was already considered in the previous section in the design of the NGD circuit.

A photograph of the experimental setup for the fabricated feedback amplifier configuration is illustrated in Fig. 4.35. In product form, all the active circuits would be integrated into one module, including the NGD circuit, the vector modulators, the subtractor, the BPF, and the EPA, thereby reducing the size of the whole feedback system. Fig. 4.36 illustrates the amplifier line-up for the MPA of the feedback application. Fig. 4.37 shows the photograph of the test setup.

### **4.3.3 Measurement Results**

Table 4.7 through Table 4.10 is the measurement data. Measured results with 1-carrier WCDMA signal before and after applying feedback loop are listed in Table 4.7 and Table 4.8. Measured results with 2-carrier WCDMA signal before and after applying feedback loop are listed in Table 4.9 and

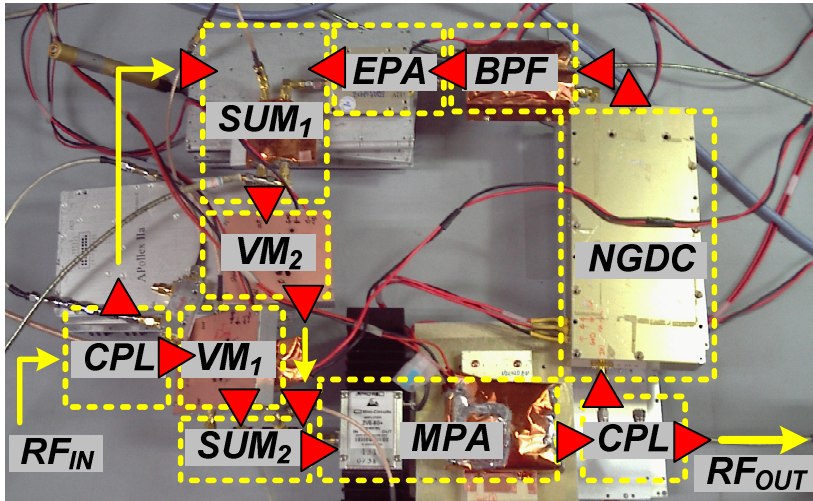


Figure 4.35: Photograph of the proposed analog feedback topology employing an NGD circuit.

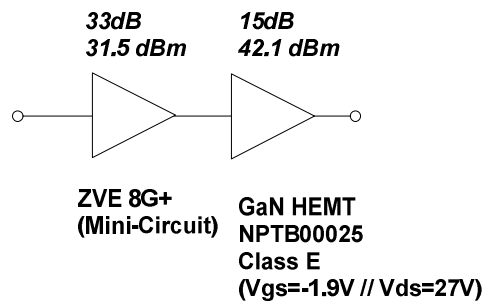


Figure 4.36: MPA line-up of feedback linearization for prototype lab measurement.



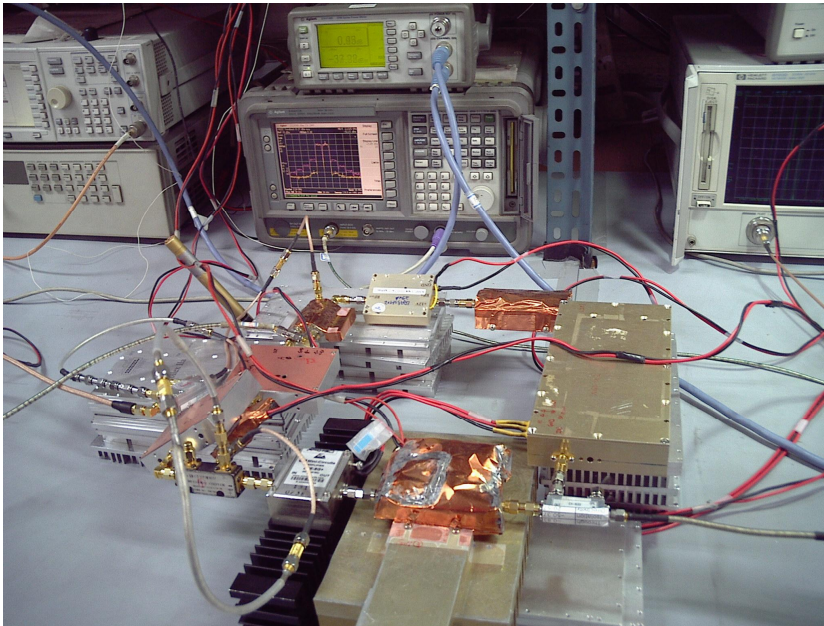


Figure 4.37: Test setup.

Table 4.10. Fig. 4.38 shows the measured spectra of the fabricated feedback amplifier for a 2-tone signal at an output power of 32 dBm/tone. The 2-tone spacing was 5 MHz and the frequency span was 50 MHz so the total IMD signals up to the 9th order could be measured. Due to the gate bias condition around a deep Class B, the output signal of the fabricated feedback amplifier exhibited much nonlinearity when the feedback loop was open. Over the entire bandwidth of interest, intermodulation distortion signals were suppressed by well below 20 dB after closing the feedback loop. This extremely large cancellation bandwidth is nearly 10 times the previous feedback amplifiers.

TABLE 4.7. MEASUREMENT TABLE FOR 1-CARRIER WCDMA SIGNAL BEFORE LINEARIZATION.

NGDC Feedback ACLR without Loop (WCDMA 1FA Test model 1 64 DPCH// Class E PA// Vgs=-1.9V )																	
Backoff from P1dB	Pin_avg [dBm]	Pout_avg [dBm]	2.14 [dBm]	L10 [dBm]	L5 [dBm]	U5 [dBm]	U10 [dBm]	V1 [V]	I1 [mA]	V2 [V]	I2 [mA]	V3 [V]	I3 [mA]	V4 [V]	I4 [mA]	DE [%]	PAE [%]
7		35	12.36	-37.14	-20.04	-22.89	-37.14	27	340	12	920						15.6
8		34	9.03	-38.81	-22.43	-22.49	-38.81	27	310	12	920						12.9
9		33	8.74	-38.99	-24.06	-25.12	-38.99	27	280	12	920						10.7
10		32	8.87	-41.78	-24.83	-25.83	-41.78	27	250	12	920						8.9
11		31	7.14	-45.44	-29.19	-29.82	-45.44	27	210	12	920						7.5
12		30	5.92	-46.29	-30.12	-31.44	-46.29	27	200	12	920						6.1
13		29	6.61	-47.97	-31.06	-33.30	-47.97	27	180	12	920						5.0
14		28	5.26	-49.43	-29.72	-32.49	-49.43	27	160	12	920						4.1

TABLE 4.8. MEASUREMENT TABLE FOR 1-CARRIER WCDMA SIGNAL AFTER LINEARIZATION.

NGDC Feedback ACLR with Loop (WCDMA 1FA Test model 1 64 DPCH// Class E PA// Vgs=-1.9V )																	
Backoff from P1dB	Pin_avg [dBm]	Pout_avg [dBm]	2.14 [dBm]	L10 [dBm]	L5 [dBm]	U5 [dBm]	U10 [dBm]	V1 [V]	I1 [A]	V2 [V]	I2 [A]	V3 [V]	I3 [A]	V4 [V]	I4 [A]	DE [%]	PAE [%]
7		35	11.18	-47.25	-34.92	-35.11	-47.25	27	340	12	920	8	195	5	410	13.3	
8		34	11.50	-49.17	-38.78	-38.94	-49.17	27	310	12	920	8	195	5	410	10.9	
9		33	10.48	-48.04	-40.29	-40.09	-48.04	27	280	12	920	8	195	5	410	9.0	
10		32	10.59	-50.12	-41.35	-41.68	-50.12	27	250	12	920	8	195	5	410	7.4	
11		31	8.36	-51.49	-47.29	-44.67	-51.49	27	210	12	920	8	195	5	410	6.2	
12		30	7.86	-50.39	-47.21	-44.89	-50.39	27	200	12	920	8	195	5	410	5.0	
13		29	7.31	-52.38	-49.89	-46.44	-52.38	27	180	12	920	8	195	5	410	4.1	
14		28	5.49	-52.22	-49.36	-47.48	-52.22	27	160	12	920	8	195	5	410	3.3	

TABLE 4.9. MEASUREMENT TABLE FOR 2-CARRIER WCDMA SIGNAL BEFORE LINEARIZATION.

NGDC Feedback ACLR without Loop (WCDMA 2FA// (PCCPCH+SCH) // Class E PA// Vgs=-1.9V )																	
Backoff from P1dB	Pin_avg [dBm]	Pout_avg [dBm]	2.1425 [dBm]	L10 [dBm]	L5 [dBm]	U5 [dBm]	U10 [dBm]	V1 [V]	I1 [mA]	V2 [V]	I2 [mA]	V3 [V]	I3 [mA]	V4 [V]	I4 [mA]	DE [%]	PAE [%]
8		34	6.572	-26.64	-17.94	-19.82	-26.64	27	270	12	920						13.7
9		33	4.958	-31.37	-19.18	-23.37	-31.37	27	250	12	920						11.2
10		32	5.476	-32.49	-21.09	-23.05	-32.49	27	230	12	920						9.2
11		31	4.105	-33.3	-21.6	-23.97	-33.3	27	210	12	920						7.5
12		30	2.676	-34.74	-23.61	-25.15	-34.74	27	190	12	920						6.2
13		29	1.689	-25.51	-25.31	-26.56	-35.51	27	170	12	920						5.1
14		28	1.74	-36.53	-26.47	-26.47	-36.53	27	160	12	920						4.1
15		27	0.88	-40.22	-27.83	-27.83	-40.22	27	140	12	920						3.4
16		26	-0.05	-40.46	-27.09	-29.10	-40.46	27	120	12	920						2.8
17		25	0.79	-40.08	-28.58	-28.64	-40.08	27	100	12	920						2.3
18		24	-1.87	-42.69	-29.34	-30.87	-42.69	27	100	12	920						1.8

TABLE 4.10. MEASUREMENT TABLE FOR 2-CARRIER WCDMA SIGNAL AFTER LINEARIZATION.

NGDC Feedback ACLR with Loop (WCDMA 2FA 64 DPCH// Class E PA// Vgs=-1.9V )																
Backoff from P1dB	Pin_avg [dBm]	Pout_avg [dBm]	2.1425 [dBm]	L5 [dBm]	U5 [dBm]	U10 [dBm]	V1 [V]	I1 [A]	V2 [V]	I2 [A]	V3 [V]	I3 [A]	V4 [V]	I4 [A]	DE [%]	PAE [%]
8		34	6.475	-41.63	-38.12	-37.99	-41.63	27	270	12	920	8	195	5	410	11.4
9		33	5.392	-45.19	-42.54	-42.04	-45.19	27	260	12	920	8	195	5	410	9.3
10		32	5.476	-47.6	-43.56	-42.43	-47.6	27	230	12	920	8	195	5	410	7.6
11		31	4.862	-46.71	-44.01	-43.52	-46.71	27	210	12	920	8	195	5	410	6.2
12		30	4.719	-51.06	-47.55	-47.68	-51.06	27	190	12	920	8	195	5	410	5.1
13		29	1.829	-52.4	-49.08	-50.16	-52.4	27	170	12	920	8	195	5	410	4.1
14		28	2.12	-58.28	-51.90	-50.41	-58.28	27	160	12	920	8	195	5	410	3.3
15		27	1.09	-27.01	-52.15	-53.34	-57.01	27	140	12	920	8	195	5	410	2.7
16		26	0.36	-56.32	-51.47	-51.31	-56.32	27	120	12	920	8	195	5	410	2.2
17		25	-0.04	-59.33	-54.24	-54.35	-59.33	27	100	12	920	8	195	5	410	1.8
18		24	-0.39	-59.70	-55.08	-54.48	-59.70	27	100	12	920	8	195	5	410	1.4

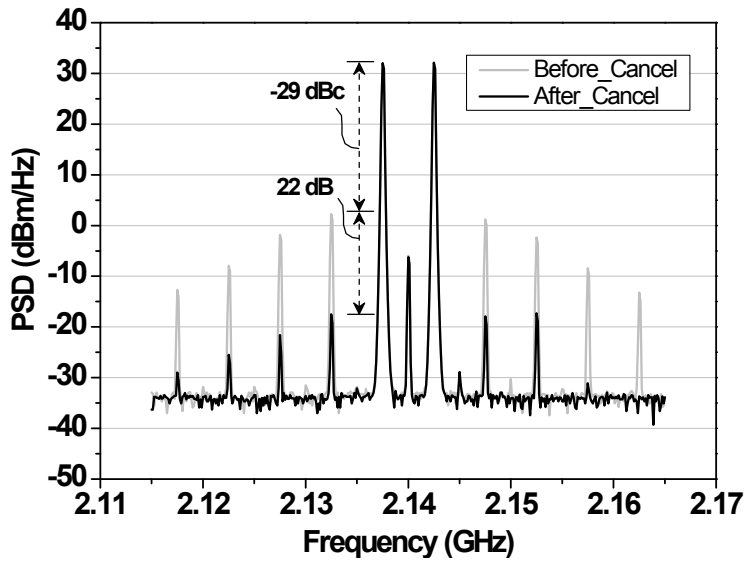
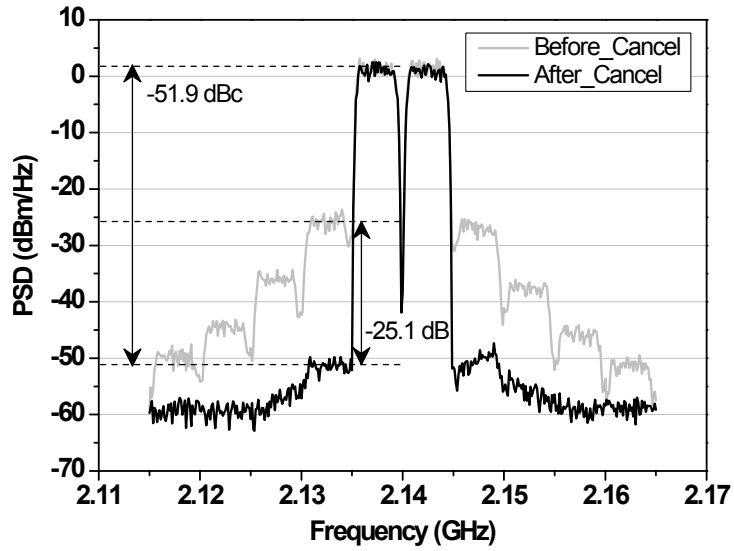


Figure 4.38: The measured 2-tone spectra before and after linearization at an output power of 32 dBm/tone.

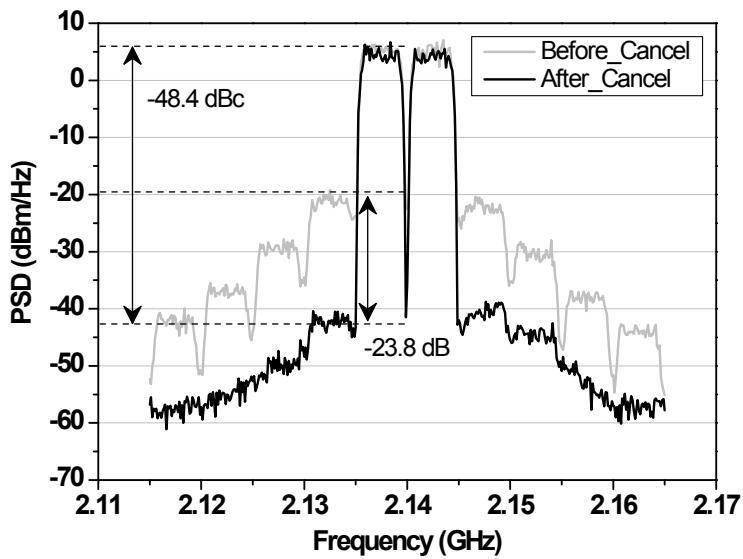
Fig. 4.39 shows the measured spectra of the feedback amplifier for the 2-carrier WCDMA signal at an average output power of 28 dBm and 33 dBm. The peak to average power ratio of the signal was 10.5 dB at 0.01 %. When the average output power was 28 dBm, the adjacent channel leakage ratio

improvement was almost 25.1 dB from -26.8 dBc to -51.9 dBc at a 5 MHz offset, as shown in Fig. 4.39 (a). When the average output power was 33 dBm, the ACLR improvement was almost 23.8 dB from -24.6 dBc to -48.4 dBc at a 5 MHz offset, as shown in Fig. 4.39 (b). In the case of an output power higher than 34 dBm, the measured ACLR does not meet the linearity specification, which is -45 dBc for a base-station PA.

Fig. 4.40 illustrates the measured ACLR before and after linearization for a 10 dB output dynamic range using the 2-carrier WCDMA signal. Optimized for 28 dBm of the output power in terms of the linearity, the fabricated system achieved at least -45 dBc (red dotted line) of the ACLR at a 5 MHz offset for an output power between 24 dBm to 34 dBm. The maximum ACLR improvement of 25.1 dB was achieved when the output power was 28 dBm, which is a superior linearity improvement with an increased bandwidth for the feedback amplifier. It was observed that the linearity of the closed loop operation is degraded when the output power was higher than 34 dBm. The reason is because the small signal gain amplifier used in the NGD circuit is thought to begin to saturate at an output power level higher than 35 dBm. Since the focus of this work is the bandwidth enhancement of the cancellation bandwidth, not the efficiency, the efficiency issues will not be seriously discussed.



(a)



(b)

Figure 4.39: The measured 2-carrier WCDMA spectra (PAPR: 10.5 dB at 0.01 %) before and after linearization at an average output power of: (a) 28 dBm, and (b) 33 dBm.

The measured ACLR and PAE performance with respect to the average output power using the 1-carrier WCDMA signal is presented in Fig. 4.41. The proposed feedback technique achieved ACLR and PAE of -46.1 dBc and 13.3 %, respectively, at an average output power of 35 dBm by using 1-carrier WCDMA signal. For the MPA without the feedback loop, the ACLR and PAE were -46.4 dBc and 2.7 %, respectively, at an average output power of 26 dBm. For the same ACLR level with and without the proposed feedback topology, PAE of the system is increased from 2.7 % to 13.3 %. Also, considering -46.1 dBc of ACLR as a reference, the available output power for the MPA is increased from 26 dBm to 35 dBm. This efficiency included the additional power consumption of the NGD circuit and the other accessory feedback circuits.

The measured results and the performance comparisons among the feedback amplifiers are summarized in Table 4.11. Due to its extremely limited bandwidth performance, the analog feedback amplifier has not been actively studied. The 50 MHz cancellation bandwidth achieved in this work is about 10 times the previous results. This is the best result ever achieved with the analog RF feedback amplifier architecture at the time of this writing, according to the authors' best knowledge.

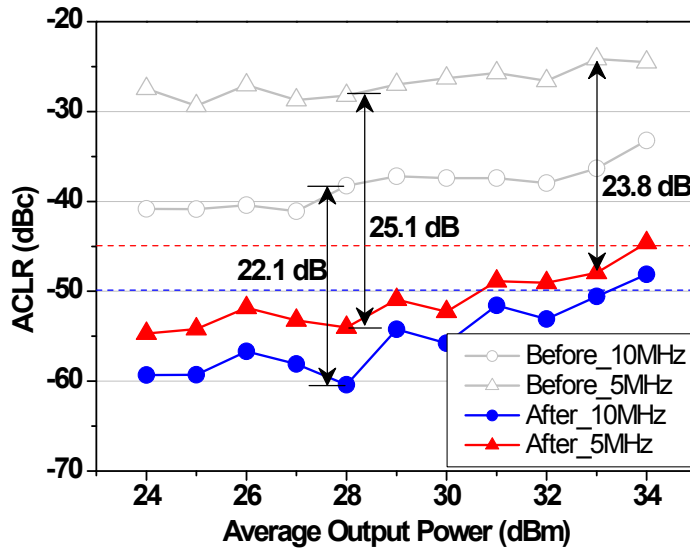


Figure 4.40: The measured ACLR with 2-carrier WCDMA signal at 5MHz and 10MHz offset for 10 dB output dynamic ranges before and after linearization.

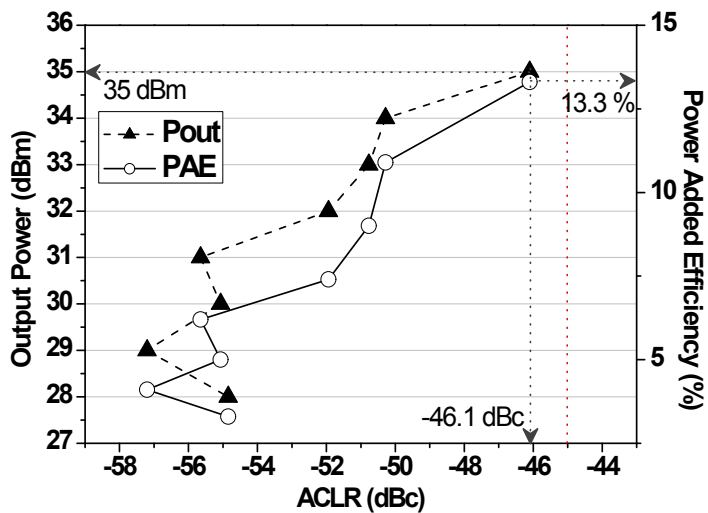


Figure 4.41: The measured ACLR and power added efficiency performance with respect to the average output power for 1-carrier WCDMA signal.

TABLE 4.11: MEASUREMENT SUMMARY AND PERFORMANCE COMPARISON  
AMONG THE ANALOG RF FEEDBACK ARCHITECTURES

	Frequency (GHz)	$P_{1dB}$ (dBm)	Test Signal	Cancellation BW (MHz)	Linearity (dBc)	Improvement (dB)	Remarks
[27]	0.35	23	2-tone	6	-40	8	IMS '94
[28]	1.85	27	2-tone	0.5	-42	20	IMS '98
[29]	0.88	33	2-tone	6	-46	12	MWJ '05
[30]	4.00	25	2-tone	1	-40	8	TMTT'90
[31]	0.89	46	2-tone	1	-40	16	EL'95
<b>This work</b>	<b>2.14</b>	<b>43</b>	<b>2-tone</b>	<b>&gt; 50</b>	<b>-51</b>	<b>22</b>	
	<b>2.14</b>	<b>43</b>	<b>WCDMA</b>	<b>&gt; 50</b>	<b>-52</b>	<b>25</b>	

\*IMS: International Microwave Symposium

\*MWJ: Microwave Journal

\*TMTT: Transactions on Microwave Theory and Techniques

\*EL: Electronics Letters

#### 4.3.4 Summary and Discussion

The novel topology was proposed for analog feedback amplifiers that yield a substantial cancellation bandwidth enhancement by employing a DE NGD circuit. The design procedure and considerations were discussed for the DE NGD circuit. With the fabricated 2-stage DE NGD circuit for the WCDMA downlink band, the analog feedback amplifier using the proposed topology experimentally achieved the highest bandwidth among those previously reported in the literature.



# CHAPTER 5

## CONCLUSION

### *5.1 Conclusion*

The first key point of this thesis is the understanding of the RF PA linearization techniques and their practical limitation in terms of efficiency and linearization bandwidth.

Due to the nonlinear transfer function of the RF transistor, the linearization technique is necessary to reduce the nonlinear distortion components. Key RF PA linearization techniques including predistortion, feedforward, and feedback topologies involves signal suppression loop to generate the error signal by cancelling out the carrier component. Among them, feedforward technique provides wide cancellation bandwidth with excellent linearization performance in expanse of complexity and efficiency degradation. Especially, insertion loss from the main path delay element takes great part in the overall efficiency degradation. Distortion feedback topology is also a good candidate for linearizing nonlinear PA in a transmitter if the time delay matching issue regarding the feedback loop can be solved. Unfortunately, those two issues have been left unsolved for a long

time, up to date. It is because every electronic circuit involves its own propagation delay for a signal to be transmitted.

Second key point of this thesis is the understanding of the NGD concept and the derivation of the general design methodology. In this thesis, the NGD concept, methods to obtain NGD, and experimental verification results were discussed. Various LE circuit structures were introduced and mathematically analyzed to find the condition to obtain the NGD. Then the LE circuit was converted into the DE based on the traditional filter design theory. To improve the circuit performance, the NGD circuit of the reflection topologies were proposed. To experimentally validate the existence of the NGD in RF electronic circuits, CW and WCDMA signals were used as the periodic and arbitrary time domain waveform signals. Based on this interesting NGD concept and the design methodology, the time advance concept was applied to the RF PA linearization technique for efficiency and bandwidth enhancement.

Third part of this thesis is composed of practical application of the NGD circuit to the feedforward linear PA. An alternative topology was proposed for the feedforward amplifiers that yield substantial efficiency enhancement and size reduction by employing a DE NGD circuit. With the fabricated 2-stage DE NGD circuit with 30 MHz bandwidth at WCDMA downlink band,

the feedforward amplifier of the proposed topology experimentally achieved the highest efficiency among those previously reported in the literature while meeting the output power and linearity specification of the commercial base-station PA, with additional advantages as to size and cost reduction. The proposed topology is thought to be especially suitable for a system with a lower frequency of operation, where the physical size of the delay element is relatively large for the system. In addition, when this technique is applied to the high power systems with a few kW, additional efficiency, size, and cost improvements may be fairly realized.

Fourth part of this thesis is devoted to the bandwidth enhancement of the feedback technique. The novel topology is proposed for the analog distortion feedback amplifier that involves a substantial cancellation bandwidth enhancement by employing an NGD circuit. The analog feedback amplifier using the proposed topology experimentally achieved the highest and commercially applicable cancellation bandwidth of over 50 MHz, which is the best performance among those previously reported in the literature.

## ***5.2 Future Research Direction***

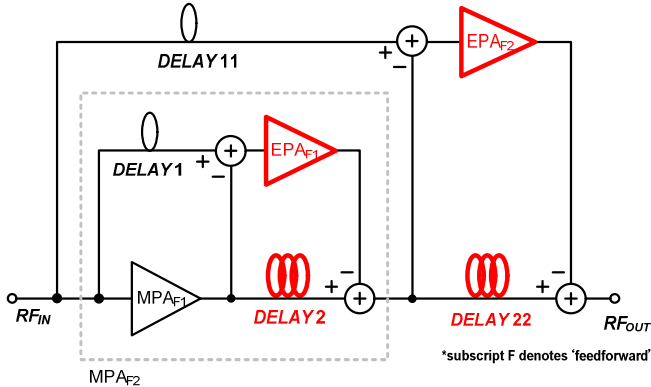
Feedforward is a technique used to linearize a nonlinear MPA. The feedforward amplifier can be used as the MPA in a second feedforward

amplifier and such system is called dual-loop feedforward, as shown in Fig. 5.1 (a). Dual-loop feedforward is usually chosen as the linearization technique for applications requiring very low levels of distortion (e.g. less than -70 dBc) over a wide bandwidth and wide dynamic range. In the dual-loop feedforward, there are two main path delay elements (DELAY2 and DELAY22) at the output of the MPA. The insertion losses of these two elements add up to seriously degrade the efficiency performance. Based on the proposed feedforward employing the NGD circuit, the reference path delay elements (DELAY1 and DELAY11) as well as the main path delay elements can be eliminated at the same time, as shown in Fig. 5.1 (b). Fig. 5.1 is just a simple example, and various topology variations are possible. Unvisited linearization topologies such as analog and digital predistortion (Fig. 5.2) and the cross cancellation technique (Fig. 5.3) need to get a full consideration as soon as possible.

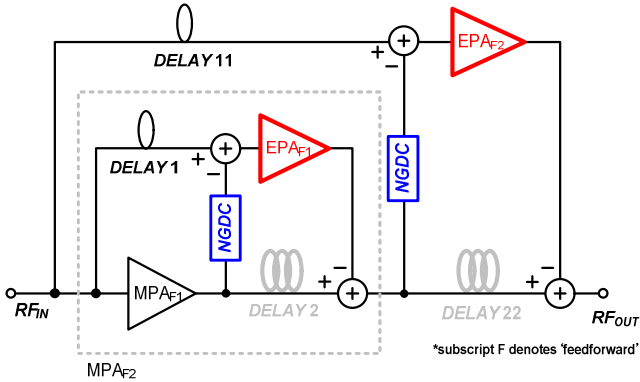
Also, the current design schematic of the NGD circuit involves bulky hybrid coupler and microstrip transmission line elements as well as lumped elements. Based on the experimental results described in this thesis, it is also possible to apply the NGD concept to the commercial mobile- and base-station PA. To achieve that goal, size reduction is essential. So the proposed NGD circuit including the gain compensation amplifier and BPF can be

considered to be integrated into a small area by using RF CMOS integrated circuit design process or LTCC design technique.

The chances on the application of the proposed NGD circuit to various RF PA linearization techniques are still widely open since the research is in the beginning stage.



(a)



(b)

Figure 5.1: Dual-loop feedforward system: (a) conventional structure with large delay element with high loss and (b) its solution to remove lossy delay element.

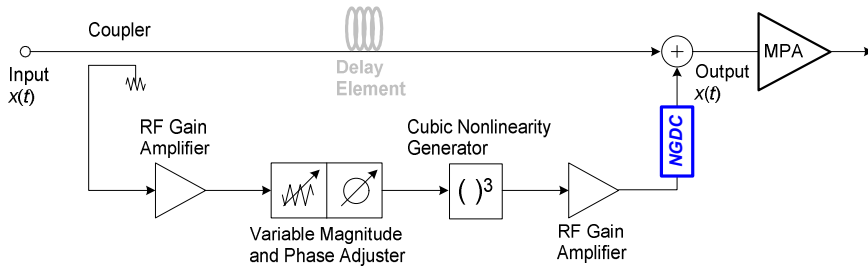


Figure 5.2: Analog predistortion linearizer employing an NGD circuit. Reference path delay element can be eliminated.

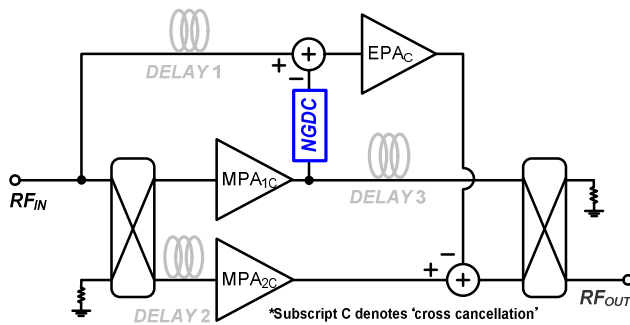


Figure 5.3: Cross cancellation technique employing an NGD circuit. Lossy delay element (DELAY 3) and other delay elements can be removed.

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# CURRICULUM VITAE AND FIELDS OF STUDY

## Heungjae Choi

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#7304, Department of Electronics and Information Engineering, Chonbuk National University, Deokjin-dong, Jeonju-si, Chollabuk-do, 561-756, Republic of Korea

Mobile Phone : +82-17-654-8583

E-mail : [streetpoet@jbnu.ac.kr](mailto:streetpoet@jbnu.ac.kr), [11010J@gmail.com](mailto:11010J@gmail.com)

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### **RESEARCH INTERESTS**

I have worked on **the linear and high efficiency RF transmitter architecture for base-station application, mostly based on Si LDMOS and GaN HEMT devices**. I have a rich experience in circuit and system design through simulation, implementation and measurement. And now I would like to broaden my knowledge to the transmitter and receiver front-end integrated circuit design including CMOS RF IC and MEMS, especially to the development of next generation transistor device.

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### **EDUCATION**

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Ph.D., Electrical and Electronic Engineering, <i>Chonbuk National University</i>	2006-present
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Academic Advisor : Professor Yongchae Jeong

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M.S., Information and Communication Engineering, <i>Chonbuk National University</i>	2004-2005
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Academic Advisor : Professor Yongchae Jeong

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B.S., Electrical and Electronic Engineering, <i>Chonbuk National University</i>	2000-2003
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## **AWARDS AND HONORS**

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16 <sup>th</sup> Human Tech Thesis Prize Awards (sponsored by Samsung Electronics): Consolation-prize with "Efficiency Enhancement of Feedforward Amplifiers by Employing a Negative Group Delay Circuit"	2010
8 <sup>th</sup> Electromagnetic Wave and Broadcasting Paper Contest (sponsored by the Korean Institute of Electromagnetic Engineering Science): Silver-prize with "Efficiency Enhancement of Feed-forward Amplifiers by Employing a Negative Group Delay Circuit"	2009
Research achievement contest in 2008 Chonbuk IT-Open Fair (sponsored by Advanced Graduate Education Center of Chonbuk for Electronics and Information Technology-BK21): Creative research award with "Digital Controlled Co-channel Feedback Interference Cancellation System with Broadband Cancellation"	2008
Student High-Efficiency Power Amplifier Design Competition (sponsored by IEEE MTT-S High Power Amplifier Components Committee): Outstanding Achievement Award with "class-AB power amplifier with 68% PAE at 2.14 GHz"	2008
5 <sup>th</sup> Electromagnetic Wave and Broadcasting Paper Contest (sponsored by the Korean Institute of Electromagnetic Engineering Science): Bronze-prize with "Dual-band Feedforward Linear Power Amplifier Using Equal Group Delay Signal Canceller"	2006

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## **REFERENCES**

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### **Yongchae Jeong, Ph.D**

Professor, Academic Advisor (*Senior Member, IEEE*)  
#7304, Department of Electronics and Information Engineering,  
Chonbuk National University, 664-14,  
Deokjin-dong, Jeonju-si, Chollabuk-do, 561-756, Republic of Korea  
Phone : +82-63-270-2458  
Fax : +82-63-270-2394  
E-mail : [ycjeong@jbnu.ac.kr](mailto:ycjeong@jbnu.ac.kr)

---

### **James Stevenson Kenney, Ph.D**

Associate Professor (*Fellow, IEEE*)  
School of Electrical and Computer Engineering, Georgia Institute of  
Technology, Atlanta, GA 30332  
Phone : +1-404-894-5170  
Fax : +1-404-894-4641  
E-mail : [jkenney@ece.gatech.edu](mailto:jkenney@ece.gatech.edu)

---

### **Chul Dong Kim, Ph.D**

Chief Executive Officer, Sewon Teletech, Inc. (*Member, IEEE*)  
*Member, the Korean Academy of Science and Technology*  
881, Kwanyang-dong, Dongahn-gu, Anyang-si, Geonggi-do, 431-804,  
Republic of Korea  
Phone : +82-31-422-0031  
Fax : +82-31-425-9931  
E-mail : [chuldkim@sewon-teletech.co.kr](mailto:chuldkim@sewon-teletech.co.kr)

---

### **Jongsik Lim, Ph.D**

Associate Professor, (*Senior Member, IEEE*)  
Department of Electrical and Communication Engineering,  
Soonchunhyang University, Eupnae-ri,  
Shinchang-myeon, Asan-si, Choongnam, 336-745, Republic of Korea  
Phone : +82-41-530-1332  
Fax : +82-41-530-1548  
E-mail : [jslim@sch.ac.kr](mailto:jslim@sch.ac.kr)

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# PUBLICATION

## INTERNATIONAL PEER-REVIEWED JOURNALS

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- [1] **Heung-Jae Choi**, J.-S. Lim, and Y.-C. Jeong, "A new design of Doherty amplifiers using defected ground structure," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 12, pp. 687-689, Dec. 2006.
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#### **INTERNATIONAL CONFERENCE PRESENTATIONS**

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- [1] H.-Y. Jeong, **Heung-Jae Choi**, Y. -C. Jeong, Y. Kim, C.-D. Kim, “The design of predistortion linearizer using zero-if mixing operation,” in *Asia-Pacific Microw. Conf. Dig.*, 2004, pp.765-768.
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