Ph.D Dissertation

Highly Linear/Efficient CMOS Power Amplifier Design for 802.11g WLAN Application

802.11g 무선 랜용 고선형/고효율 CMOS 전력 증폭기 설계

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To my beloved family

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ABSTRACT

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The demand for higher integration of wireless transceivers has been growing rapidly to reduce the cost and size in a modern wireless communication system. According to these demands, many RF chip designers have sought to enhance the degree of transceiver integration by using low-cost CMOS technology. However, in these efforts to implement highly integrated SoC, RF power amplifiers (PAs) have become a major roadblock due to a low breakdown voltage of the transistor and lossy substrate associated with CMOS technology. In particular, the PAs for wireless communication systems with high data rate have been required high efficiency and good linearity at the backed-off power levels to efficiently amplify a multiplexing signal with a high peak-to-average power ratio. Although many CMOS PA techniques for efficiency and linearity enhancements have been introduced, PAs based on the scaled-down CMOS technology still face many obstacles for reliable operation, such as hot carrier injection and time-dependent dielectric breakdown problems. Despite these problems, many studies for PAs using the standard deep-submicron CMOS process have been performed, since it is beneficial that the CMOS PAs can be readily integrated with various other control circuits in a transmitter [1]-[78].

The objective of this dissertation is the CMOS power amplifier design techniques for efficiency and linearity enhancements. In a power amplifier design, two main concerns as

1) to maximize the efficiency at backed-off power region, while the linearity is satisfying within system requirement, and 2) to minimize active area so that it can be integrated with RF transceiver for WLAN application, have been addressed. Thus, I have proposed a novel CMOS Doherty amplifier with variable balun transformer to enhance efficiency at backed-off power region. In addition, CMOS PA scheme using dual gate bias is proposed so that it can be implemented in small size while achieving high efficiency and linearity. Both the proposed two amplifiers are tested and verified with 64-QAM OFDM signal with 20 MHz channel bandwidth, and demonstrated that those amplifiers are compliant with linearity specification for 802.11g WLAN application.

Keywords: CMOS power amplifier, CMOS Doherty amplifier, Dual gate bias, Variable balun transformer, WLAN.

ABSTRACT IN KOREAN

요약

현대 무선 통신 시스템에서 무선 송수신기의 보다 높은 집적화를 위한 요구가 가격과 크기를 줄이기 위해서 급격히 증대되고 있다. 이러한 요구에 따라서, 많은 고주파 칩 설계자들은 저가의 CMOS 공정을 이용하여 집적도를 높이기 위해서 많은 노력을 해 왔다. 그러나 고집적화된 시스템 온 칩을 구현하기 위한 이러한 노력에 있어서, 초고주파 전력 증폭기들은 CMOS 공정의 낮은 항복 전압과 손실이 큰 기판 특성 때문에 주요 장애물이 되었다. 특히, 고속 데이터 통신을 위한 무선 통신 시스템용 전력증폭기는 높은 최대 전력 대비 평균 전력 비율이 높은 다중화 신호를 효율적으로 증폭시키기 위해서 최대 전력보다 크게 낮춰진 평균 전력 세기에서 높은 효율과 선형성이 요구된다. 비록 선형성과 효율 증대를 위한 많은 CMOS 공정 기반의 전력 증폭기 기술들이 소개되고 있지만, 소형화된 CMOS 기술을 기반한 전력 증폭기는 안정적 동작에 있어서 여전히 많은 장애 요소에 직면하고 있다. 그럼에도 불구하고, 송신부의 다양한 다른 제어 회로와 집적될 수 있다는 굉장히 큰 장점 때문에 소형화된 CMOS 공정을 이용한 전력 증폭기에 대한 많은 연구가 진행되고 있다.

이 논문은 효율과 선형성의 향상을 위한 전력 증폭기 설계 기법을 다루고 있다. 전력 증폭기 설계에 있어서 두 가지의 주요 쟁점들이, 1) 낮춰진 전력 세기에서 선형성을 만족하면서 효율 개선 2) 무선랜용

RF 송수신기에 집적화 되기 위한 면적 최소화에 맞추어졌다. 그리하여, 낮춰진 전력 세기에서 효율 증대를 위해 가변 발룬 변환기를 이용한 CMOS 도허티 전력 증폭기가 제안되었다. 게다가, 전력 증폭기가 고선형성과 효율을 달성하면서 작은 면적에 구현될 수 있도록 하기 위해 이중 게이트 바이어스를 이용한 전력 증폭기 구조가 제안되었다. 이러한 제안된 두 가지 증폭기는 64 QAM 변조방식의 직교 주파수 다중화 (OFDM) 신호를 이용하여 측정되고 검증되었으며, 그 측정된 증폭기의 성능이 무선랜 선형성 규격에 부합함을 보였다.

키워드 : CMOS 전력 증폭기, CMOS 도허티 증폭기, 이중 게이트 바이어스, 가변 발룬 트랜스포머, 무선 랜.

ABBREVIATIONS

ACLR	adjacent channel leakage ratio
AM-AM	amplitude to amplitude distortion
AM-PM	amplitude to phase distortion
BALUN	balanced to unbalanced
BT	bluetooth
CDMA	code division multiple access
CG	common gate
CMOS	complementary metal oxide silicon
CS	common source
CW	continuous wave
DA	drive amplifier
DAT	distributed active transformer
DE	drain efficiency
DPD	digital pre-distortion
ET	envelope tracking
EVM	error vector magnitude
FcCSP	flip chip-chip scale package
GaAs	gallium arsenide
GSM	global system for mobile
HBT	hetero-junction bipolar transistor
HFSS	high frequency structure simulator

HPA	high power amplifier
HPM	high power mode
IC	integrated chip
IMD	inter modulation distortion
LTE	long term evolution
LPM	low power mode
MOSFET	metal oxide silicon field effect transistor
OFDM	orthogonal frequency division modulation
P1dB	1dB compression point
PA	power amplifier
PAE	power added efficiency
PAPR	peak to average power ratio
PCB	printed circuit board
PGA	programmable gain amplifier
PHEMT	pseudomorphic high electron mobility transistor
PVT	process, voltage, temperature
QAM	quadrature amplitude modulation
RF	radio frequency
RX	receiver
SMPA	switching mode power amplifier
SoC	system on chip
TSMC	Taiwan semiconductor manufacturing company
TX	transmitter

VBT	variable balun transformer
WLAN	wireless local area network
WCDMA	wideband code division multiple access
WiMAX	world-wide interoperability for microwave access

CHAPTER 1

1.0 Introduction

The wireless communication market has experienced a remarkable development and growth since the introduction of the first modern mobile phone system, with a steady increase in the number of subscribers, new application areas, and higher data rates. This growth of wireless communication industry has led to several tremendous advancements in semiconductor technology. Among them, the most significant progress is in CMOS technology. The remarkable advanced characteristic of transistors is that their speed increases, while they consume less power per function in digital circuits, and cost decreases as their size is reduced. As a result, these CMOS technology advancements have enormously contributed to performance and function enhancement of modern mobile devices.

As technologies advancement, the demand for higher integration of wireless transceivers has been growing rapidly to reduce the cost and size, in a recent wireless communication system. Accordingly, the inevitable task and ultimate goal of the modern wireless communication industry is the full integration of digital, analog, and even radio frequency (RF) functions. To meet these demands, many researchers who study chip sets have tried to enhance the degree of transceiver integration by using CMOS technology, owing to its cost effective material and great versatility. As a result, CMOS system-on-chip (SoC) has been widely implemented in wireless applications such as wireless local area network (WLAN)

and Bluetooth (BT).

However, recent SoC designers are trying constantly to integrate up to a PA module. In these efforts to implement a fully integrated SoC, RF power amplifiers (PAs) capable of high power levels have become a major roadblock owing to the lossy substrate and the low breakdown voltages associated with CMOS technology [1]-[2]. Thus, the implementation of CMOS RF front-end module (FEM), such as an RF switch [3] or a RF PA [4], remains a challenging task. Accordingly, most commercial products are based on gallium arsenide (GaAs) technologies, as shown in Fig. 1.1.

Today, the various demands from consumers have stoked the development of multiple standards. For example, global system for mobile communications (GSM), code division multiple access (CDMA), and wideband CDMA (WCDMA) are now used for voice and relatively low data rate communications while WLAN and long term evolution (LTE) mainly target high data rate communications with varying mobility. The typical output power levels of PAs for some wireless applications are

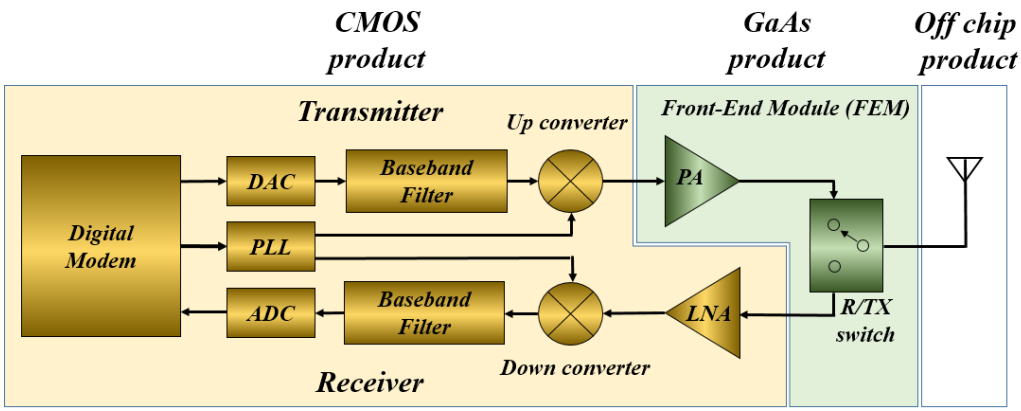


Fig. 1.1. A block diagram of a direct-conversion transceiver and its fabrication processes.

shown in Fig. 2, along with their data rates. While many standards require different average output powers due to peak-to-average power ratio (PAPR), the general peak output power requirement for wireless communications is usually 30 dBm to 35 dBm as indicated in Fig. 1.2. Due to the poor linearity performance of CMOS devices, satisfying the key specifications of commercial RF PA products (high output power and high linearity) with CMOS devices poses a great challenge and even a greater one for emerging wireless communications [4],[5] in which good linearity is a default requirement.

Besides output power and linearity problems, there is more critical issue associated with CMOS design. It is well known that a PA can only achieve maximum efficiency at peak output power. As output power decreases, efficiency drops rapidly. Unfortunately, the PA for high data rate wireless communication

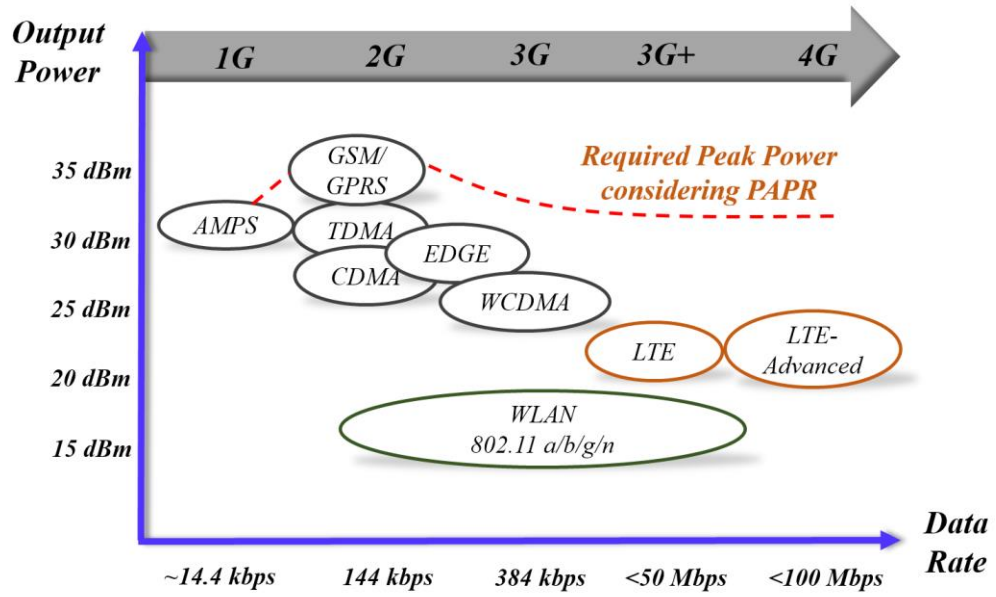


Fig. 1.2. Output power requirements of various standards.

system is operated at backed-off power level as much as PAPR from the peak power. It means that the PA has low efficiency in the wireless system with high PAPR. As shown in Fig. 1.3, since a DC power consumption of PA has occupied large portion of total power consumption in modern wireless system, many studies for the PA technique for enhancement efficiency at backed-off power level are being continued in order to expand battery life time of portable device.

1.1 Motivation

The difficulties of CMOS RF PAs have already been described in the previous section. In terms of performance, CMOS technologies are not a good solution. Nevertheless, CMOS RF PA has a large benefit in terms of cost since CMOS technology would be the cheapest among other candidates such as hetero-junction bipolar transistor (HBT), PHEMT, GaAs technologies, as shown in Fig. 1.4. In addition, CMOS RF PA can be implemented in small area by being integrated with

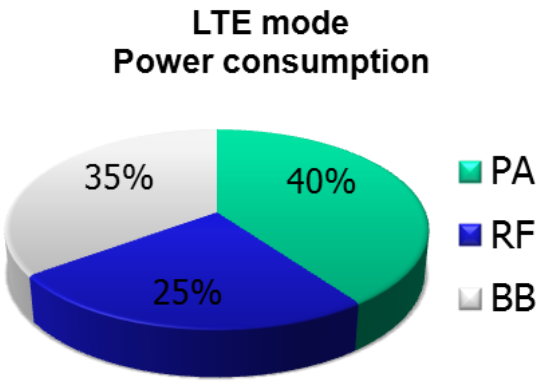


Fig. 1.3. Internal power consumption distribution of LTE mobile device

other control circuits. Consequently, it is the best solution to put the PA, transceiver IC, digital baseband and power management module on a single piece of silicon.

Currently, the atmosphere is ideal for an RF CMOS PA in the wireless market. One caveat, however, is how to achieve comparable performance using CMOS in implementing a PA. From various study for the enhancement of the PA performance, a novel CMOS PA techniques such as distributed active transformer (DAT) [4] and stacked PA have been introduced [7]-[13]. As a result, the SoC chipset products which integrates up to CMOS PA were released for WLAN and BT applications in which consume small power relatively. However, some performance or reliability issues still remain in those techniques. Therefore, in serious consideration of the implementation of CMOS RF PAs, this research will introduce and discuss various efforts at determining good PA solutions for their

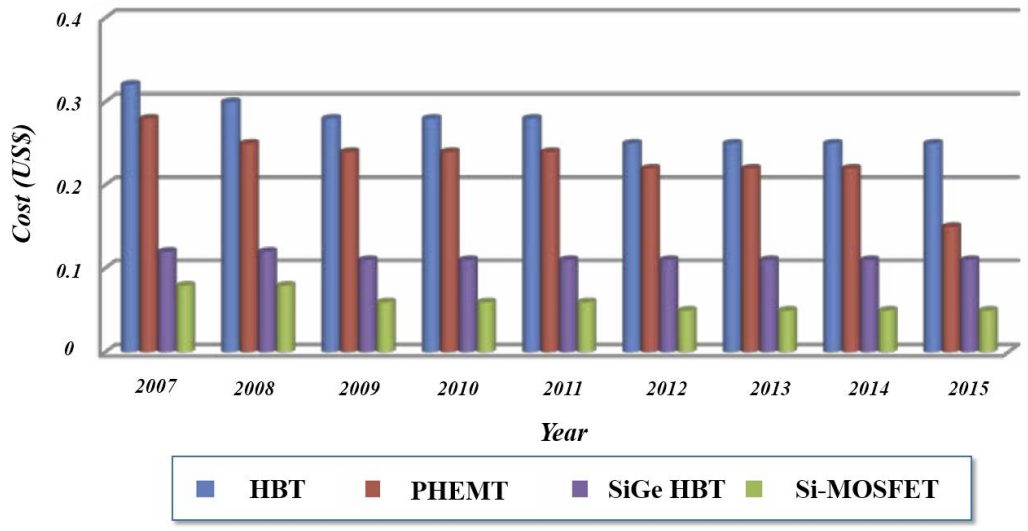


Fig. 1.4. Cost advantages of CMOS technologies over other semiconductor technologies for PA solutions in US$/mm^2

commercial applications in wireless communications.

1.2 Literature Review

Extensive researches on CMOS PA for the enhancements of high linearity, output power, and efficiency have been presented [1]-[25]. The first CMOS RF PA that could deliver hundreds mW power was reported in 1997, implemented in a single-ended configuration with a 0.8 um CMOS technology [14]. The PA could provide 1 W of output power at 804 ~ 849 MHz with 62% drain efficiency using 2.5 V supply. The impedance transformation network was built with off-chip passive components. Single-ended configuration was the designers' first choice when PAs were implemented with discrete transistors. From the integration perspective, it is ill-suited for full integration since it increases the possibility of coupling with other on-chip components. The first CMOS RF differential PA that could deliver over 1W at GHz range was reported in 1998, implemented with a 0.35 μm CMOS technology [15]. It leveraged high-Q bond-wires as inductors for the matching network, and micro strip balun for differential-to-single-ended conversion at the output. Using injection locking technique to reduce the input drive requirements, the PA could transmit 1 W power at 2 GHz with 41% combined power added efficiency using 2 V supply. Since then, there have been quite a few publications on CMOS RF PAs [16]-[20]. They all rely on off-chip components such as bond-wires, off-chip inductors, off-chip capacitors to implement low-loss impedance transformation network, and thick-gate-oxide transistors to avoid overstressing devices. Since the most important factors for 2G

system were output power capability and efficiency of PA, the majority of published CMOS PAs were nonlinear.

Without using power combining techniques, reported fully integrated CMOS PA with 55% drain efficiency could only achieve 85 mW power at 900 MHz [21], or could transmitter 150 mW at 1 dB compression point (P_{1dB}) at 5 GHz but only with 13% power added efficiency [22]. If we could combine power from several efficient small PAs, medium-to-high output power could be achieved with good power efficiency.

Various methods have been used to split and combine RF signals. Among them, transformers have been widely used as means for combining RF power. However one serious problem associated with conventional on-chip transformers in CMOS technologies is high insertion loss which directly translates into loss in the power efficiency. Therefore, this approach has only been adopted to implement inter-stage matching [23]. Circular geometry distributive active transformer, known as DAT, was proposed to overcome high insertion loss problem in on-chip transformers [4]. It functions as an eight-way power combiner with good efficiency at the peak output power, implemented with 0.35 μm CMOS transistors. Despite many advantages of this approach, the circuit geometry DAT still has some problems inherently from its structure [24], [26].

Besides integration, there is another serious issue associated with conventional CMOS PA. It is well known that a PA can only achieve maximum efficiency at the peak power. However, in modern wireless communication with high PAPR, the

efficiency is very critical issue at backed off power level from the peak power, as mentioned in previous section.

Even if high-performance CMOS-based GSM/GPRS [29], GSM/EDGE [30], and WCDMA PAs [31], as well as fully-integrated WLAN CMOS transceivers with integrated front-ends [26]-[28] have been reported, further research is needed in the field of CMOS PAs. Challenges are the limitations on the supply voltage, posing challenges to meet the requirements on linearity, output power, bandwidth, and efficiency.

1.3 Dissertation Objectives and Organization

The main objective of this dissertation is for linearization and efficiency enhancement techniques for CMOS PA. The rest of this dissertation is organized as follows. Chapter 2 describes the fundamental principle of CMOS RF PA efficiency enhancement techniques, briefly. Main techniques to be discussed are the out-phasing/LINC PA, the envelope tracking (ET) PA, and Doherty PA. The advantages and practical limitation of each approach will be discussed, especially regarding the efficiency issues and bandwidth issues.

Chapter 3 describes concept of differently biased amplifier using current combining method and mathematical analysis as well as the practical applicability. Based on the research literatures, causality issues related to the voltage combining are discussed. And then, the efficiency and linearity characteristics based on combination of differently biased amplifier are compared with those characteristics of other amplifiers with the fixed single bias. The proposed amplifier is fabricated

by using TSMC 0.13 um CMOS process and is experimentally validated by using 802.11g 64-QAM OFDM signal which has high PAPR.

Chapter 4 introduces a novel CMOS Doherty amplifier with small occupied size. The Doherty PA is one of the most popular schemes with which to obtain high efficiency at backed-off power levels [25]. However, the conventional Doherty scheme has critical limitation to integrated implementation of CMOS process. Thus, the discussion begins with the principle of Doherty operation to solve the size limitation. And as an impedance inverter which is the key factor of load modulation, a novel variable balun transformer structure is proposed in order to facilitate high integration. In addition, the adaptive bias technique is adopted to auxiliary amplifier of Doherty amplifier to maximize efficiency at backed off power level. The technique contributes so that the real CMOS Doherty amplifier operates nearly same as ideal Doherty operation. This CMOS Doherty amplifier is also fabricated and validated by using TSMC 0.13 um CMOS process.

Chapter 5 describes CMOS PA using dual bias and un-even size for common source stage amplifier. The technique is proposed to reduce the active area of CMOS PA since it is targeted to commercial product. Without additional area consumption, the proposed amplifier for enhancements of linearity and efficiency is demonstrated through the simulation and measurement. In addition, to support various functions similar to other commercial products, RF variable gain amplifier and high power by-pass switch design issues for reliable operation are introduced together. The amplifier is fabricated with fully integrated SoC by using 40 nm standard CMOS process and demonstrated experimentally by WLAN 802.11g

signal. Finally, Chapter 6 summarizes the contributions of the dissertation and provides ideas for future research in this area.

CHAPTER 2

OVERVIEW OF KEY RF POWER AMPLIFIER EFFICIENCY ENHANCEMENT TECHNIQUES

In this chapter, the fundamental principle and the problems related to the representative efficiency enhancement techniques of RF PA such as out-phasing (LINC) PA, the envelope tracking (ET) PA, and Doherty PA will be briefly discussed.

2.1 Outphasing PA

The basic principle of the outphasing concept shown in Fig. 2.1, is that an amplitude and phase-modulated signal, $s(t)$ in (2.1), is decomposed into two constant amplitude signals, $s_1(t)$ and $s_2(t)$ as in (2.2) [32], [33] containing the original signal and the quadrature signal, $e(t)$ (2.3).

$$s(t) = r(t)e^{j\theta(t)} = r_{\max}\cos(\varphi(t))e^{j\theta(t)}; 0 \le r(t) \le r_{\max} \tag{2.1}$$

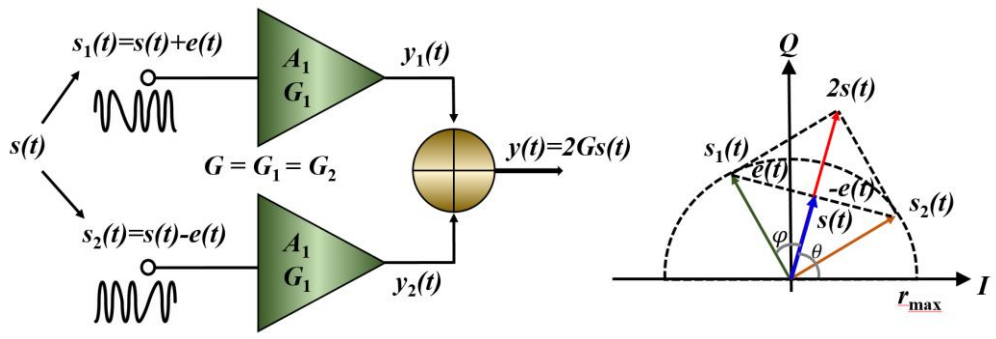
$$\begin{aligned} s_1(t) &= s(t) + e(t) = r_{\max}e^{j\theta(t)}e^{j\varphi(t)} \\ s_2(t) &= s(t) - e(t) = r_{\max}e^{j\theta(t)}e^{-j\varphi(t)} \end{aligned} \tag{2.2}$$

$$e(t) = js(t)\sqrt{\frac{r_{\max}^2}{r^2(t)} - 1} \tag{2.3}$$

Each of these two signals is fed to its own nonlinear RF PA cell, which is usually a switching mode PA (SMPA) cell that could be driven by the constant envelope outphased signals to achieved high efficiency. The SMPA amplifies each separated

signal by an identical amount. After the individual amplification, the separated signals are fed to the combiner for recombination. The resulting output signal after combination is an amplified version of the input signal without any added distortion in the ideal case. In other words, the outphasing PA combiner restores the RF signal into amplitude modulated one with the two constant envelope inputs, in which the distortions on each SMPA cell can be canceled due to outphasing. The combiner design is also one of the most critical parts of the outphasing transmitter to maintain high efficiency and linearity.

The theoretical efficiency of the outphasing transmitter is 100% because the PAs used are highly efficient nonlinear amplifiers as well as the constant envelope nature of the phase-modulated signals. From the linearity point of view, the linearity performance of outphasing transmitter is dominated by the RF gain and phase match between the two amplified signals [34]. The generation of two signals and the power combining after the amplification are also key issues in these types of PA.



(a) (b)

Fig. 2.1 (a) A block diagram of outphasing PA and (b) outphasing decomposition concept.

The advantages of outphasing PA are obvious. Due to using nonlinear high efficiency RF PAs, theoretically high transmitter efficiency can be realized with this technique. However, the drawbacks stem from the matching between two-branches and ultra wide phase signal bandwidth. The performance of the system depends on the effects of the necessary reactive compensation, which may have bandwidth restrictions. The design of the outphasing modulator is critical because the linearity of the whole system depends on it. Sufficient gain and phase matching are therefore difficult to realize [35]-[44].

Although this technology had demonstrated elegant efficiency with acceptable linearity for handset or terminal application scenarios, it is still challenging to apply it to CMOS RF PA design because of size issue, large passive loss, the performance sensitivity.

2.2 Envelope Tracking

The block diagram of a classical envelope tracking (ET) PA is shown in Fig. 2.2. The ET, which utilizes liner PAs whose low efficiency weakness during relatively low power levels can be mitigated by adjusting the supply voltage accordingly [45]-[53].

Typically, the ET PA comprises a linear RF PA and a supply modulator for providing a modulated supply voltage as a dynamic supply to the PA. The basic idea of the ET technique is to drive the linear RF PA in its high efficiency region regardless of the magnitude of the input signal. This is accomplished by detecting the envelope of the input signal and using it to modulate the supply voltage of the

linear PA. In general, when using a linear PA, good enhancements in efficiency can be achieved with ET technique. However, the efficiency of the supply modulator should be sufficiently high to achieve high overall efficiency of the ET system. High efficiency can be achieved by involving a switch mode power supply design, although there may be some severe bandwidth limitations for the supply modulator. There are usually DSP blocks that compare the timing error measurements of envelope and RF branches to perform delay alignment, crest factor reduction,

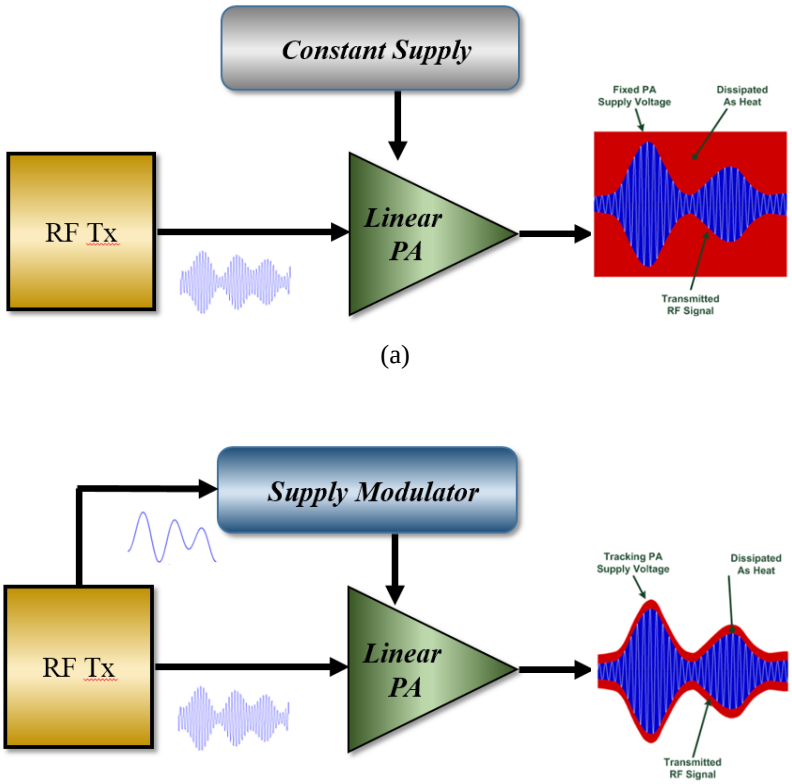


Fig. 2.2 Block diagrams of (a) conventional fixed supply bias and (b) a classical ET PA.

envelope shaping functions, and finally pre distortion to the ET PA. ET PAs are relatively easy to shift to other carrier frequencies, since it is only necessary to adjust the matching network of the RF PA in a relatively simple way without any adjustments to the supply modulator. For the scenario of increased bandwidth, the ET PA has a significant challenge associated with maintaining high efficiency and accuracy of the supply modulator, which generates the time varying power supply.

Based on these reasons, ET becomes more and more attractive for high efficiency, broadband, and linear transmitters for modern communications such as the 4G system and beyond. However, there are also three major disadvantages of ET.

A. The ET technique requires the use of a high-efficiency supply modulator to increase the efficiency of the RF PA.
B. The efficiency of ET is smaller at low input levels than at high input levels because both envelope and RF paths exhibit the same amplitude modulation shape.
C. The distortion caused in the supply modulator can be introduced to RF PA in different forms and, therefore, it requires extra powerful linearization methods to correct them. Linearity requirements force the use of new but more complex pre distortion algorithms and a wide bandwidth requires a higher degree of timing alignment precision.

Finally, although linearity and efficiency are mutually exclusive properties in the traditional fixed DC supplied RF PAs, ET PAs can linearly amplify amplitude and

phase modulated signals with much higher efficiency. Both linear PAs and high efficiency SMPAs can benefit from ET with modern pre-distortion algorithm.

2.3 Doherty

The basic principle of Doherty PA operation is based on a load modulation, with which the load impedance varies according to the power level. The Doherty architecture has been reborn recently and chosen as the mainstream high efficiency RF PA for wireless infrastructure since W. H. Doherty developed it in 1936 [32]. It was called “new after 70years” with several variants developed to meet ever–growing efficiency requirements for high PAPR signal amplifications.

Even or symmetrical Doherty is the classic topology, as shown in Fig. 2.3. In Doherty RF PA, the carrier to peak cell size ration is 1:1. Therefore, the RF input signal is split by a 3 dB splitter or hybrid coupler into two paths with 90° phase difference. With a low power input level, the peak amplifier cell does not operate, which results in a load impedance of $2 \cdot Z_0$ for the carrier amplifier cell. While increasing the input power level, both carrier and peak amplifier cells are turned on and the matching network and micro strip offset lines modulate the carrier cell load impedance from $2 \cdot Z_0$ to Z_0 according to the output power levels. The load impedance modulation is performed by a quarter wave length transmission line at output stage of carrier amplifier. In addition by adjusting both carrier and peak cell bias feeding line, the intention to compensate the package internal parasitic effects such as bonding wire inductance can be implemented to further improve the Doherty performance.

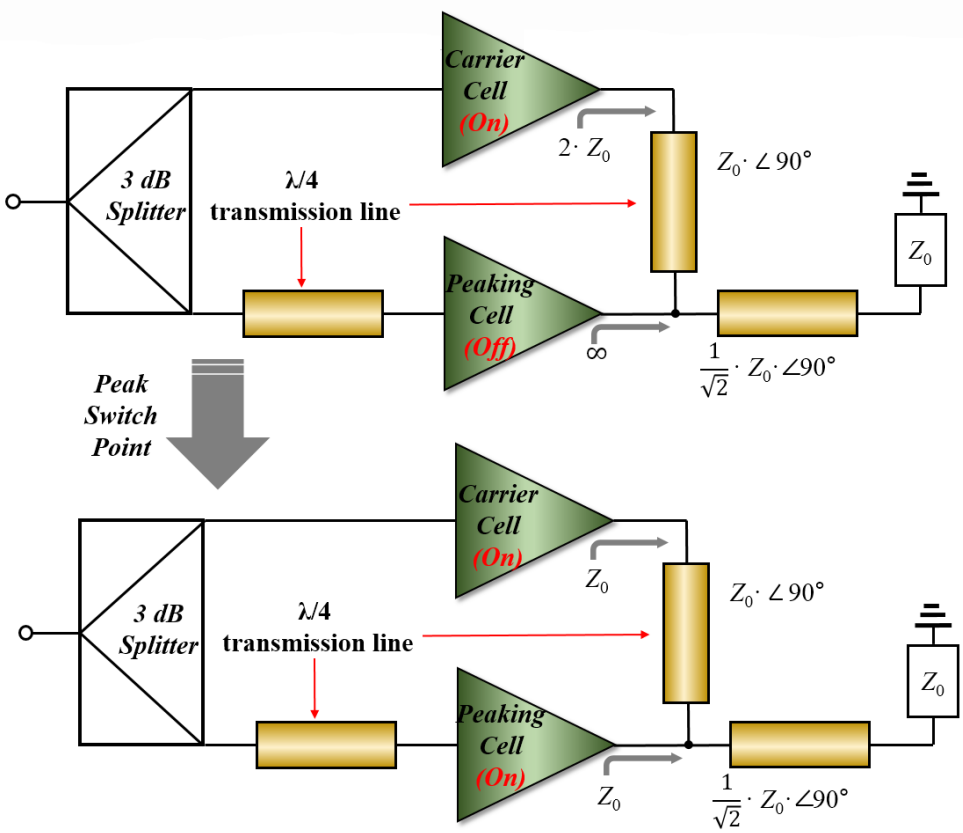


Fig. 2.3 The principle and schematic diagram of the traditional Doherty RF PA.

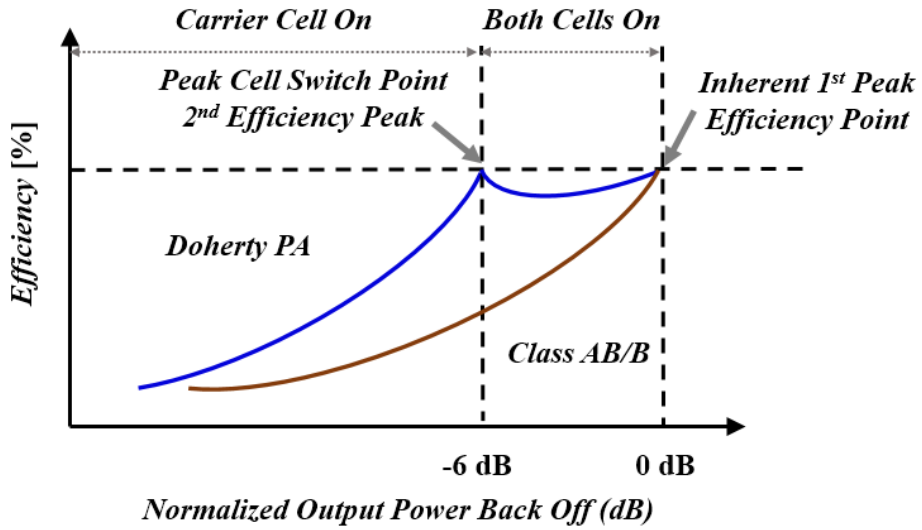


Fig. 2.4 The efficiency trace comparison between Doherty and class AB/B RF PAs.

As illustrated in Fig. 2.4, besides the inherent first peak efficiency point of the peak cell, the efficiency curve will keep increasing during low power mode with the peaking cell shut down. Therefore, the carrier cell can generate the second peak efficiency point at 6 dB or four times lower from maximum output power. As shown in Fig. 2.4, the low power efficiency of Doherty PA can be enhanced. However, since the each output signals of Doherty PA should be combined by in-phase, operating bandwidth has a limitation. In addition, quarter wavelength transformers which have frequency dependency are necessary for the accurate load modulation, there are some difficulties to implement in CMOS process, such as size and output loss.

2.4 Summary and Discussion

Due to poor efficiency characteristics of CMOS process, efficiency enhancement technique is necessary to reduce the power consumption for wireless communication system. RF PA efficiency enhancement techniques including outphasing, ET, and Doherty topologies have been discussed. Among them, the outphasing topology can achieve the best efficiency performance, but it has significant limitation in the views of the output power dynamic range and operating bandwidth. And the ET can be useful for efficiency enhancement, but the topology has also significant drawbacks of complexity and linearity degradation. The Doherty PA is one of the most popular schemes with which to obtain high efficiency at backed-off power levels [32]. However, the large circuit size of the transmission line transformers limits implementation of a fully integrated CMOS

Doherty PA. To solve these issues of CMOS Doherty PA implementation, a variable balun transformer is introduced. Detail explanation of CMOS Doherty will be discussed in the chapter 4.

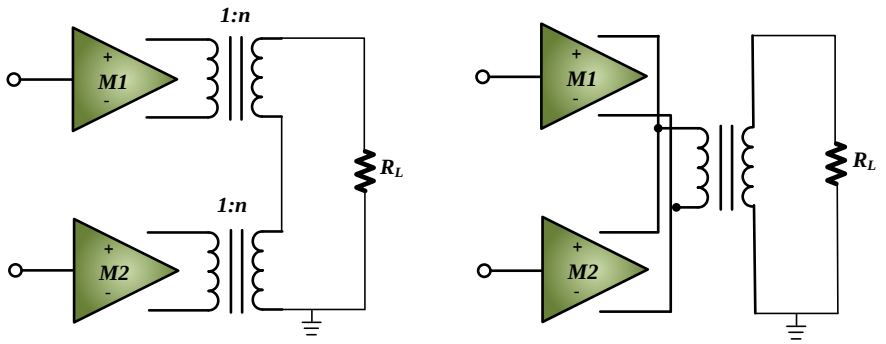
CHAPTER 3

HIGHLY EFFICIENT AND LINEAR CMOS POWER AMPLIFIER USING DUAL GATE BIAS FOR WLAN APPLICATION

Some previous studies for integrated CMOS PAs have been implemented using a voltage-mode transformer based on a power combiner, which is a series combining transformers, as shown in Fig. 3.1(a) [54]-[56]. However, the series voltage combining method is very difficult to implement symmetrically and requires two or more transformers. For these reasons, the insertion loss of the voltage-mode transformer is increased and causes a degradation of the overall efficiency and performance of a CMOS PA.

In this chapter, a CMOS PA using a current-mode transformer-based power combiner is proposed, as shown in Fig. 3.1(b). The proposed structure can reduce the size and output power loss, owing to the use of only one transformer. In addition, amplifier using dual bias such as those found in a Doherty scheme are used to enhance the efficiency at the backed-off power level and improve the nonlinear characteristics. A complete block diagram of the proposed PA is shown in Fig. 3.2. The PA consists of drive and power stages to obtain the high gain and high linear output power. The characteristics of the proposed amplifier will be compared with conventional Class AB amplifier and validated experimentally.

3.1 Power Combining Methods of Power Amplifier



(a) (b)

Fig. 3.1. The amplifier structures with (a) the voltage mode transformer based power combiner and (b) the current mode transformer based power combiner.

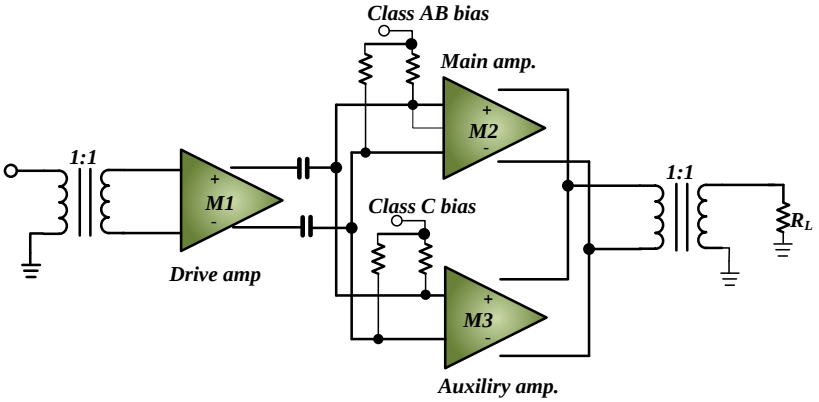


Fig. 3.2. Total block diagram of proposed power amplifier.

3.1.1 Impedance Transformation

Normally, the PA must have a low load impedance to increase the maximum output power at the limited voltage amplitude, as shown through (3.1):

$$P_{out,\max} = \frac{V_{\max}^2}{2R_L} \tag{3.1}$$

Therefore, to deliver the maximum output power to the transmitting antenna, the low load impedance must be transformed into 50 Ω. In a typical GaAs HBT PA, the impedance transformation is implemented using an inductance-capacitance

(*LC*) resonant matching network, as shown in Fig. 3-3(a). However, in CMOS technology, the loss of the *LC* resonant matching network cannot be ignored, owing to the low *Q* factor of the passive components and the sensitivity to the impedance error from a layout parasitic effect [57]. The magnetic coupled transformer can be used to implement the matching network as the solution of a conventional *LC* matching network, as shown in Fig. 3.3(b). The advantage of a magnetic coupled transformer is that it can be used to implement a high-efficiency matching network, regardless of the impedance transformation ratio. Additionally, in the case of a CMOS PA that adopts a differential structure, the amplifier must use a balanced-to-unbalanced (balun) component to transform the differential inputs into a single output. Since the magnetic coupled transformer can perform an impedance transformation and balun operation simultaneously, it is useful for a

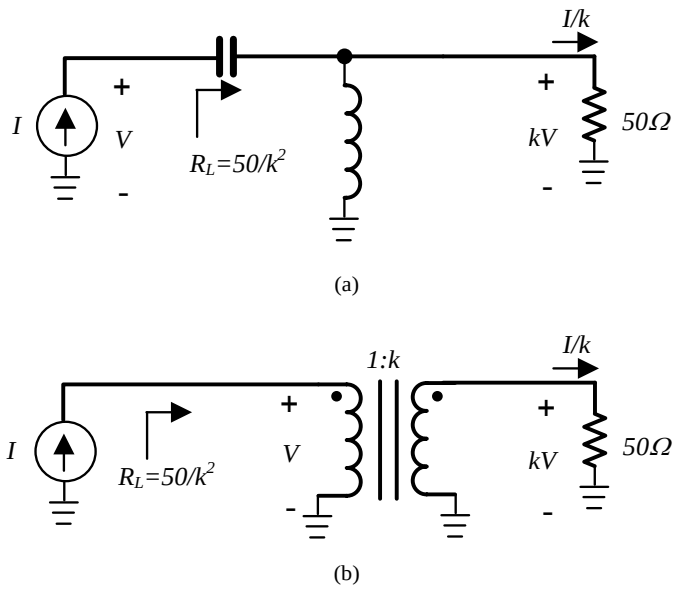


Fig. 3.3. (a) Impedance transformer using *LC* matching network and (b) magnetic coupled transformer.

CMOS PA design [4].

3.1.2 Power Combining Method

In a CMOS PA, a single amplifier is not sufficient to satisfy the output power requirements for certain applications, owing to a low breakdown voltage characteristic. Thus, most PAs have adopted several methods for combining the output power of multiple PAs. One power combining method is the voltage-mode transformer-based power combiner. In the voltage-mode transformer-based power combiner, the secondary coils of the transformer are connected in series and their primary coils are driven by separate amplifiers, as shown in Fig. 3.4. The AC voltages are added to the secondary side to obtain a higher output power. The advantage of a voltage-mode transformer-based power combiner is that the impedance of each PA is up scaled *n* times, which relaxes the design of the PA and

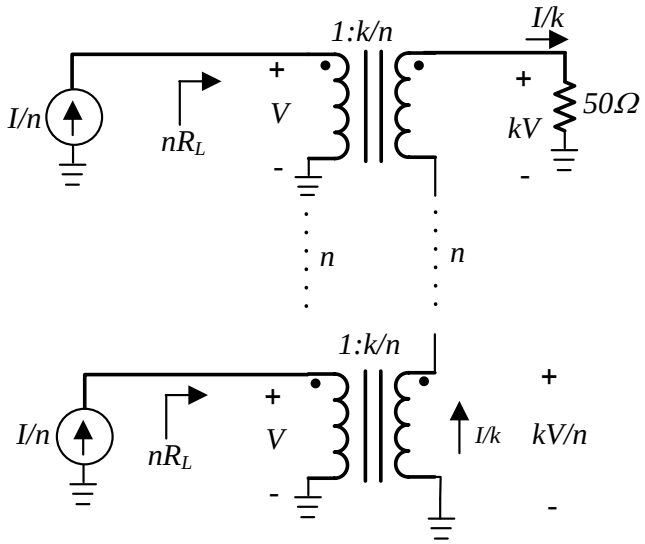


Fig. 3.4. Voltage-mode transformer-based power combiner.

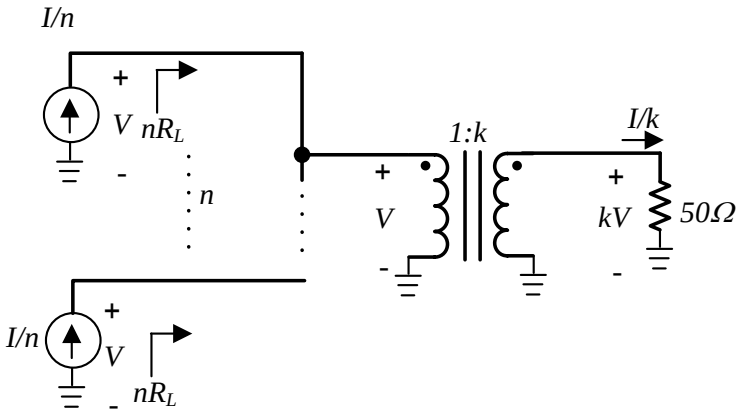


Fig. 3.5. Current-mode transformer-based power combiner.

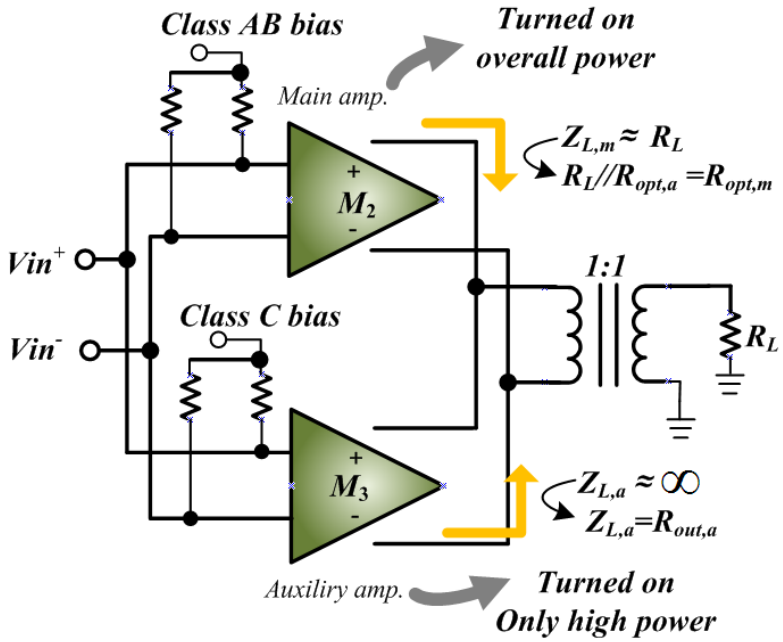


Fig. 3.6. Block diagram of proposed power stage.

reduces the sensitivity to the layout parasitic effect.

A conventional CMOS Doherty PA usually uses this voltage-mode

transformer-based power combining method. However, not all of the primary ports of the voltage-mode transformer may be symmetric with respect to the secondary ports, which can cause amplitude and phase mismatches. Such these mismatches can reduce the maximum output power and overall efficiency of the PA. The losses of separate transformers will also be added at the output port. Thus, an overall transformer losses is so large that the losses cannot be ignored.

To avoid these problems, another solution for the power combining methods is the current-mode transformer-based combiner shown in Fig. 3.5. All the power stages can easily be made symmetric. The advantage of this topology is a smaller loss in the secondary coil. If the resistance of a secondary coil is *r*, the total resistive power loss is as follows:

$$P_{loss,r}(\text{current\_mode}) = \frac{I^2 \cdot r}{k^2} \tag{3.2}$$

where *I/k* is an output current. Since the resistance values of secondary coils (*r*) are connected serially in case of the voltage-mode transformer-based combiner, the total resistive power loss in a secondary coil is

$$P_{loss,r}(\text{voltage\_mode}) = \frac{I^2 \cdot n \cdot r}{k^2} \tag{3.3}$$

where *n* is the number of stages. Thus, the total secondary loss of the current-mode transformer-based combiner is *n* times smaller than that of the voltage-mode. In this paper, the CMOS Doherty PA is designed with the current-mode transformer-based power combiner to reduce the transformer loss and size.

3.2 Proposed CMOS Power Amplifier Operation

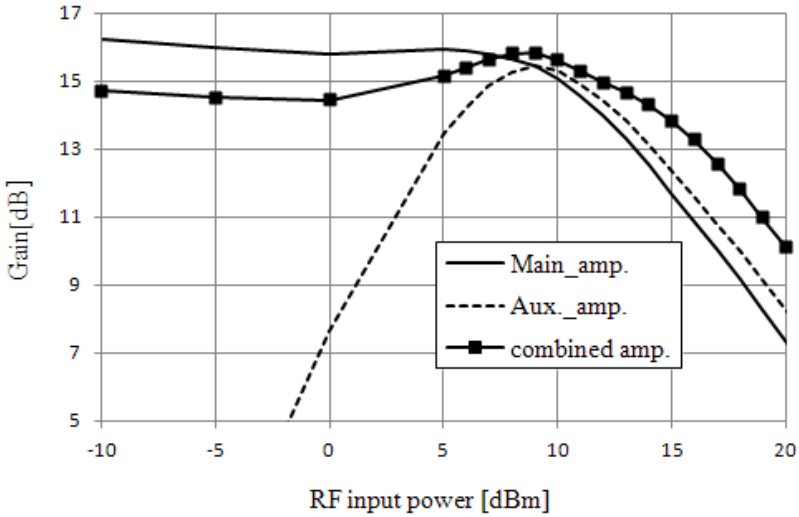


Fig. 3.7. Proposed power stage simulation results for RF input power vs. gain of individual amplifier and combined amplifier.

The proposed PA consists of the drive stage of a drive amplifier (M_1) and the power stages of the class AB main amplifier (M_2) and the class C auxiliary amplifier (M_3), as shown Fig. 3.6. The class AB biased M_2 provides linear amplification for all power ranges while the class C biased M_3 only contributes the increase of the output linear power [58]. Therefore, the power stage amplifiers operate differently according to the input power level. At a lower power level, M_3 does not operate owing to a low bias condition (V_g, M_3<V_{th}) and its consequential output impedance should be infinite to minimize the power loss. Additionally, M_3 starts to operate at the power level at which M_2 is saturated. In this operation, the output impedance of M_3 is changed from infinite to the optimum output impedance of $R_{out,a}$ and the load impedance of M_2 is decreased from R_L to $R_L//R_{out,a}$(=$R_{opt,m}$), which is the optimum load impedance of M_2. As a result, the maximum output power of M_2 is enhanced owing to a decrease of the load impedance, and the total

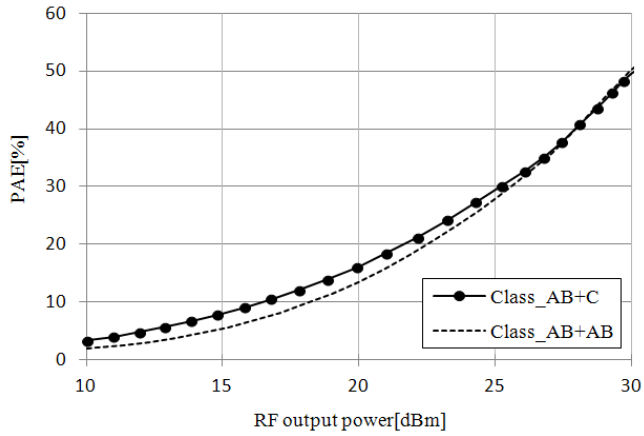


Fig. 3.8. PAE simulation results for even (class AB and class AB) and uneven biased (class AB and C) amplifiers.

maximum output power of the power stage is increased by combining the enhanced linear power of M_2 and the output power of M_3. Figure 3.7 shows the simulation results for the gain and output power characteristics of individual amplifiers and the combined amplifier, according to the RF input power. As shown in Fig. 3.7, the maximum output power of a combined amplifier is 4.5 dB higher than that of a class AB main amplifier alone, including a power combiner loss of 1 dB.

Although the maximum output power of the proposed amplifier has a small improvement of 1.5 dB compared to that of the even biased two-class AB amplifiers, the proposed amplifier can reduce the quiescent bias current and enhance the efficiency at the lower power level. The power added efficiency (PAE) traces for the output power of even biased (class AB) amplifiers and uneven biased (class C and class AB) amplifiers are shown in Fig. 3.8. Additionally, the proposed uneven biased amplifier has a good linearity performance since the higher drive power to the auxiliary amplifier causes a proper third order intermodulation

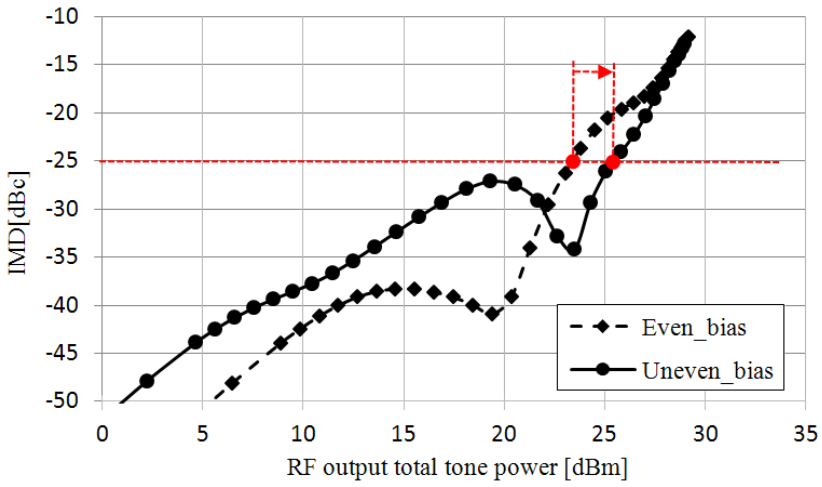


Fig. 3.9. IMD3 simulation results for even and uneven biased amplifiers.

distortion (IMD3) cancelation.

Fig. 3.9 shows the simulation results of IMD3 according to the output power for even and uneven biased amplifiers. The simulation is performed using two-tone signals with 5 MHz tone spacing. As shown in Fig. 3.9, the proposed amplifier improves IMD3 at the higher power levels at where the auxiliary amplifier is operated. In the simulation, the two-tone total output power with IMD3 under 25 dBc is 2 dB higher than that with the even biased amplifier.

3.3 Implementation of Proposed CMOS PA

The design of the proposed PA is implemented using the commercial Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 μm technology. A simplified schematic of the designed PA is shown in Fig. 3.10. Differential cascode structures are used as the drive and power stages to prevent gain reductions that are

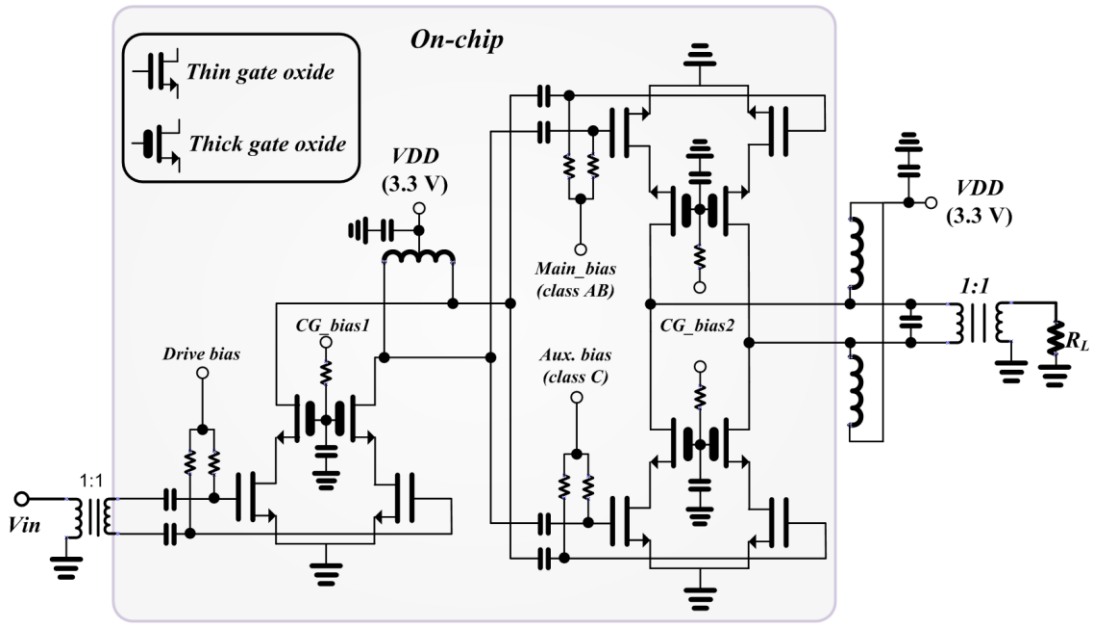


Fig. 3.10. Simplified schematic of designed PA.

induced by the bonding wires. The common gate transistors of the power stage are implemented using a high breakdown voltage device (L_{min}=0.35 μm) to increase the output voltage swing. In addition, common source transistors are implemented using an RF transistor with a minimum gate length of 0.18 μm to achieve a desirable RF performance. In addition, all transistors in the drive amplifier are implemented with an RF transistor with a minimum gate length of 0.18 μm since it can endure the output voltage swing of the drive stage.

The common source gate bias of an auxiliary amplifier for the class C operation is applied at 0.38 V, which is below the threshold voltage of 0.5 V, whereas that of the main and drive amplifiers is selected to be 0.6 V for the class AB operation and the linearity specification. Additionally, the gate bias of common gate transistors for all amplifiers is selected to be 2.2 V to reduce the voltage stress on the common

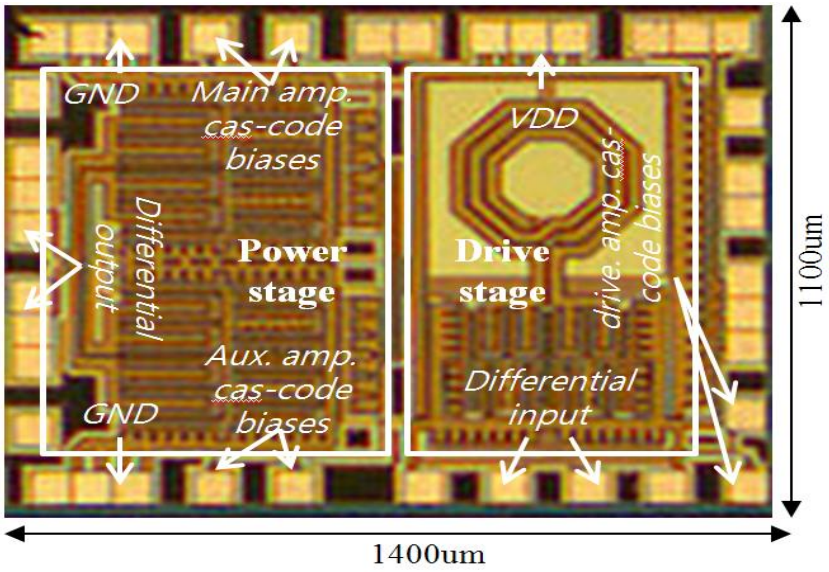


Fig. 3.11. Chip photograph of implemented PA.

source transistors, and the transistor sizes are chosen to obtain the optimum output impedance and target power. The output signals of the main and auxiliary amplifiers are combined with a current-mode transformer. The input and output transformers are implemented with off-chip components to obtain a stable operation and reduce the chip size. A photograph of the chip layout of the proposed amplifier is shown in Fig. 3.11. The chip can be implemented at a compact size of 1,400 μm × 1,100 μm, including the pads.

3.4 Measurement Results

3.4.1 Continuous Wave (CW) Signal Measurement

Figure 3.12 shows the measured gain and PAE characteristics of the proposed amplifier for the CW signal at 2.4 GHz. The measured linear gain, 1 dB compression point (P1dB), saturation power (Psat), PAE at P1dB, and peak PAE

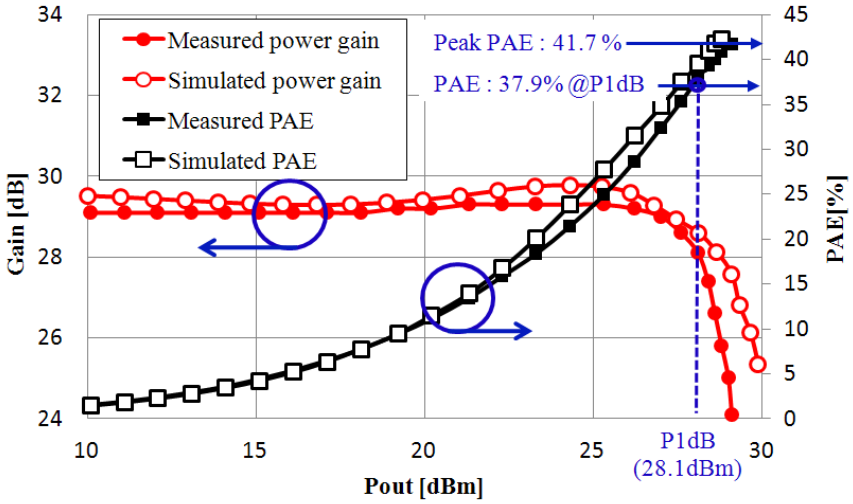


Fig. 3.12. Simulated and measured results for power gain and PAE according to output power level at 2.4 GHz.

are 29 dB, 28.1 dBm, 29.5 dBm, 37.9%, and 41.7%, respectively. The amplifier had a quiescent current of 162 mA for the overall amplifier. A close agreement between the simulation and measurement results is observed.

The two-tone test was performed at 2.4 GHz with 5 MHz tone spacing. The simulated and measured IMD3 characteristics according to the output power are shown in Fig. 3.13. For a linear operation of 25 dBc in the case of the two-tone signal, the PA must be operated under an output power of 25.8 dBm. Additionally, as shown in Fig. 3.13, the IMD3 of the fabricated amplifier is achieved under –25 dBc in all power ranges by adjusting the bias point of the main amplifier and the position of the sweet spot.

3.4.2 Modulation Signal Measurement

Finally, to verify whether the linearity of the fabricated amplifier is suitable for 802.11g WLAN system application, a high-level modulation signal was applied.

The used modulation signal source was an OFDM signal with a data rate of 54 Mb/s using 64 QAM. The measured error vector magnitude (EVM) at 2.4 GHz is shown in Fig. 3.14. As shown in the figure, the measured average output power that satisfies the EVM requirement of 25 dB is around 22 dBm. This measured EVM compliant output power is 2 dB higher than the maximum output power requirement of 802.11g application, owing to RX/TX switching loss and line loss. Additionally, the PAE performance is 21.5% at the EVM compliant output power. Figure 3.15 shows the output spectrum mask of the fabricated amplifier at a channel average power of 21.9 dBm with an adjacent channel leakage ratio of 25 dBc. As shown in Fig. 3.15, a spectrum mask requirement can be satisfied at an average output power of 21.9 dBm. In addition, the constellation error of the amplifier at an average output power of 21.9 dBm is shown in Fig. 3.16.

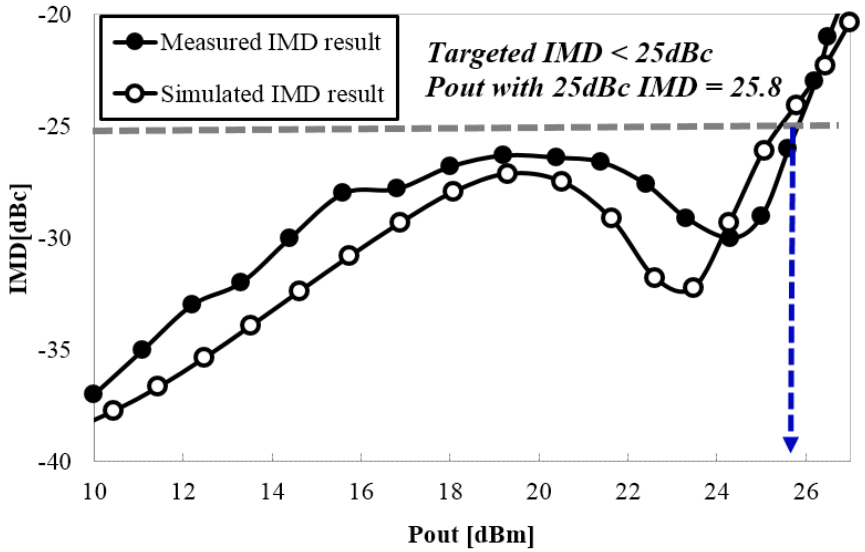


Fig. 3.13. Simulated and measured IMD performances for 2-tone signals with 5 MHz tone spacing at 2.4 GHz.

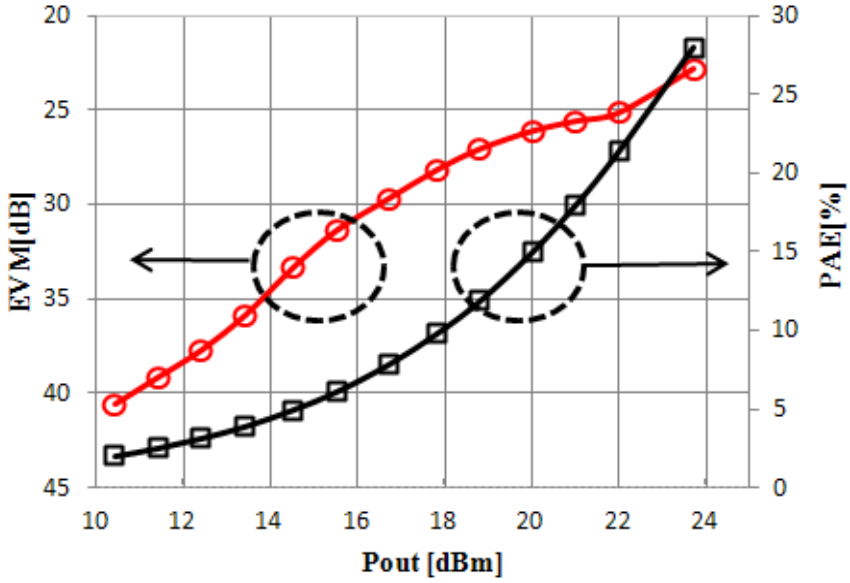


Fig. 3.14. Measured EVM and PAE performance of amplifier with 64-QAM OFDM at 2.4 GHz.

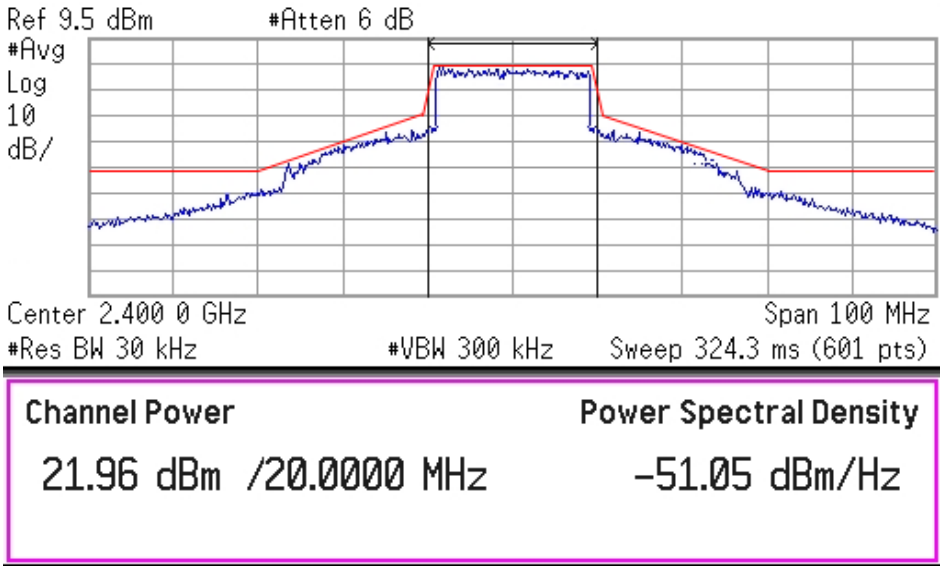


Fig. 3.15. Measured output spectrum mask of amplifier.

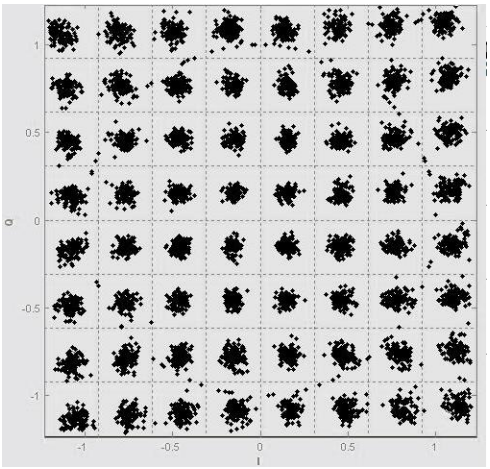


Fig. 3.16. Constellation error of amplifier with 64-QAM-OFDM signal.

3.5 Summary and Discussion

In this chapter, a current-mode combined transformer-based dual biased PA was demonstrated. The performances of the PA are summarized in Table 3.1, together with other state-of-the-art WLAN PAs. The proposed PA proved to be superior in terms of the peak PAE. Additionally, its efficiency with a 54 Mbps WLAN signal achieved 22% at the maximum linear output power, which satisfies the WLAN (802.11g) requirements. Its high efficiency results from the uneven bias and high linear characteristics of the proposed amplifier architecture. The PA showed a desirable PAE at a 25 dB EVM and spectral mask characteristics at the maximum average output power of 22 dBm. In addition, the amplifier was implemented at the small size of 1.4 mm × 1.1 mm, using the current-mode power combining method.

TABLE 3.1. 1st comparison of CMOS PAs for WLAN application.

	CMOS Process	Supply [V]	P_{sat} [dBm]	Peak PAE [%]	P_{out} / PAE @ 25 dB EVM	Size [mm^2]	Linearization technique
ISSCC 2010 [59]	65 nm	3.3	31.5	25	22.7 dBm/16%	N/A	g_m (class AB ~ B)
CICC 2010 [57]	65 nm	3.3	33.5	37.6	26 dBm/20%	6	g_m (class AB ~ B)
ESSCIRC 2010 [60]	0.25 μm	3.3	20.5	26.7	13 dBm/19%	1.92	series combining Doherty
JSSC 2009 [61]	90 nm	3.3	30	33	22.7 dBm/12%	4.2	switching Doherty
This work	**0.18 μm**	**3.3**	**29.5**	**41.7**	**22 dBm/22%**	**1.51**	g_m (class AB ~ C)
801.11g specification	Minimum EVM with 64-QAM-OFDM signal (54 Mbps): 25 dB. Maximum transmitted output power: 100 mW (20 dBm).						

CHAPTER 4

CMOS DOHERTY AMPLIFIER WITH VARIABLE BALUN TRANSFORMER AND ADAPTIVE BIAS CONTROL FOR WIRELESS LAN APPLICATION

As mentioned in Chapter 2, the Doherty scheme is very popular scheme for efficiency enhancement. Up to date, CMOS implementation of Doherty PA has been challenge due to output loss and bulky size. In order to overcome these problem, a novel CMOS Doherty topology using a variable balun transformer and adaptive bias control is proposed.

In this chapter, detail operation principle, analysis, and implementation of the proposed CMOS Doherty PA will be explained and briefly discussed.

4.1 Doherty Amplifier Operation

4.1.1 Load Modulation

The Doherty amplifier was first proposed in 1936 [32] and focused on efficiency enhancements or power conservation primarily. The original Doherty amplifier consisted of two tube amplifiers and an impedance inverter, as shown in Fig. 4.1. This impedance (Z)-inverter is configured using a $\lambda/4$ transmission line, and it modulates the load impedance (Z_m) of the main amplifier according to the operation of the auxiliary amplifier. This modulation ensures superior efficiency performance of the Doherty amplifier in the low-power region [62]-[70].

Fig. 4.2 shows a simplified schematic diagram which explains the load modulation process. It is assumed that both amplifiers have high output impedance and that both can be replaced with current sources. Load modulation is conducted according to the fundamental current ratios of both amplifiers. In the Doherty PA, the main amplifier is normally biased with the class AB or B mode, while the auxiliary amplifier is biased with the class C mode. Therefore, only the main amplifier is operated until its maximum output voltage is reached. Thus, the first efficiency peak is achieved. When the input voltage is increased further, the auxiliary amplifier is turned on, while the load impedance of the main amplifier is decreased. Although the output voltage of the main amplifier remains constant, the

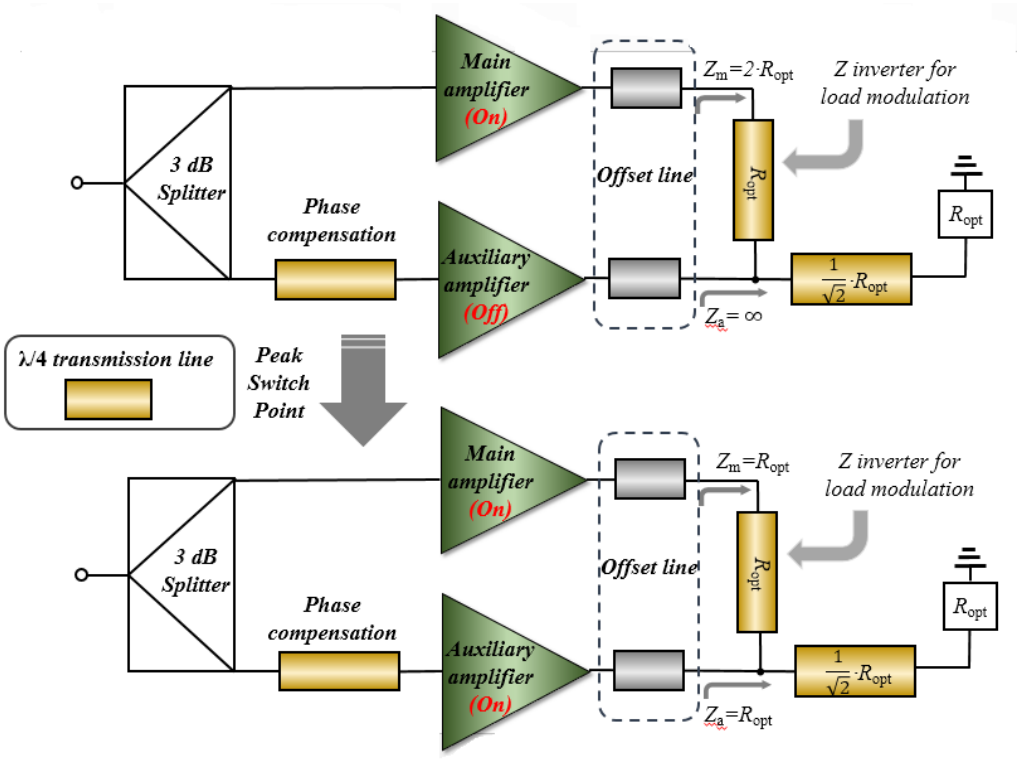


Fig. 4.1. Conventional Doherty amplifier structure and operation principle.

total output voltage of the Doherty PA is increased by the operation of the auxiliary amplifier. As a result, the second efficiency peak can be achieved at the maximum voltage of the auxiliary amplifier, as shown Fig. 4.3. These two peak efficiency points help to enhance the efficiency at backed-off output power levels. The key factor to this operation is the load modulation of the amplifiers by the impedance inverter. The load impedance of each amplifier can be derived by the active load–pull principle [66]. This is expressed in (4.1) and (4.2):

$$Z_m = 2 \cdot R_{opt}, \quad Z_a = \infty, \qquad @\, 0 < \frac{V_{in}}{V_{in,\max}} \le \frac{1}{2} \tag{4.1}$$

$$Z_m = \frac{2 \cdot R_{opt}}{1 + \dfrac{I_a}{I_m}}, \quad Z_a = \left(1 + \frac{I_m}{I_a}\right) \cdot \frac{R_{opt}}{2}, \quad @\, \frac{1}{2} < \frac{V_{in}}{V_{in,\max}} \le 1 \tag{4.2}$$

where V_{in}, $V_{in,max}$, Z_m, and Z_a are the input voltage, the maximum input voltage, and the load impedances of the main and auxiliary amplifiers, respectively. I_m and I_a correspondingly represent the total drain current of the main and auxiliary amplifiers, and R_{opt} is the optimum load impedance required to obtain the maximum output power.

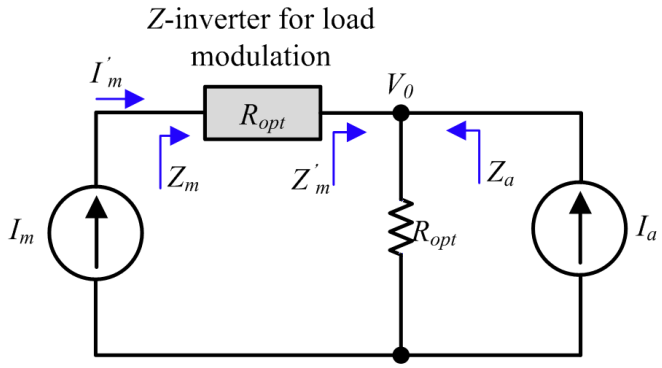
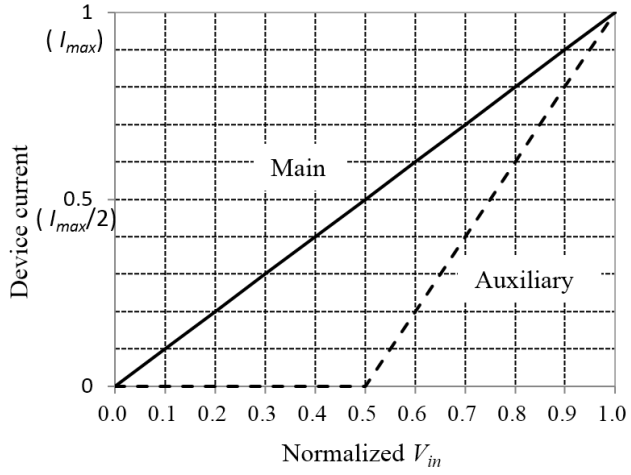
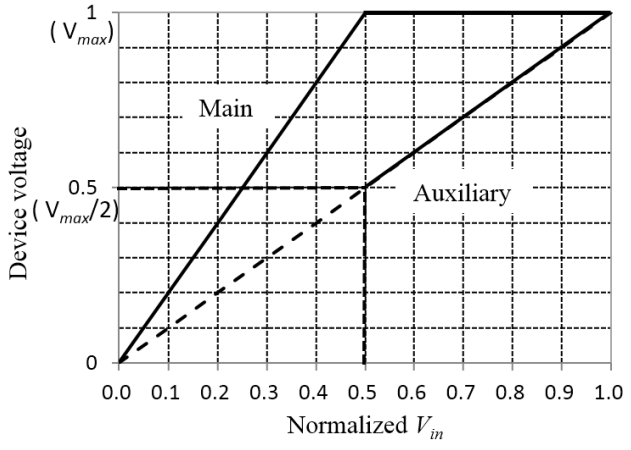


Fig. 4.2. Simplified schematic diagram for load modulation.



(a)



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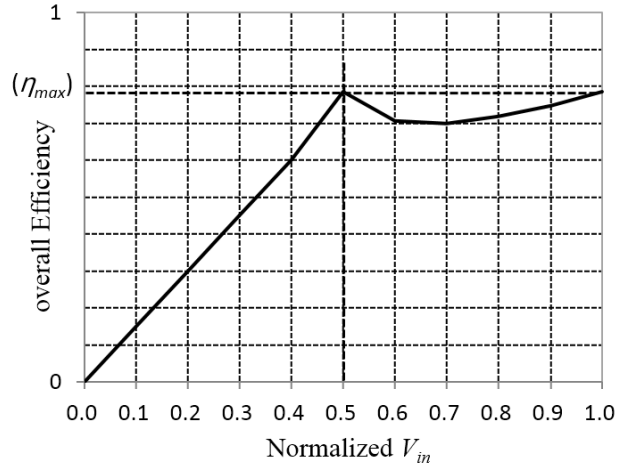


(c)

Fig. 4.3. Ideal (a) output current, (b) voltage, and (c) efficiency of the main and auxiliary amplifiers.

As shown in (4.1) and (4.2), the main PA maintains a load impedance of $2 \cdot R_{opt}$ while the auxiliary PA is turned off. Thus, the first maximum efficiency of the Doherty PA is generated by operation of the main PA at half of $V_{in,max,}$ as shown in Fig. 4.3(a). In addition, when the normalized input voltage (V_{in}) increases from half of $V_{in,\,max}$ to $V_{in,max}$, I_a and I_m are reached at the same maximum output current, as shown in Fig. 4.3(b) while Z_m is changed to R_{opt}, Z_a is also changed to R_{opt}. As a result, the Doherty PA scheme leads to an overall output power increase of 6 dB with achieving the second peak efficiency at the maximum output power of the amplifier, as shown in Fig. 4.3(c).

Consequently, the Doherty PA has superior efficiency compared to the class B PA throughout the output power range. Accordingly, the Doherty PA is a useful PA scheme in modern wireless systems for high-PAPR applications.

4.1.2 Linearity Characteristic

The Doherty PA has a linear gain for all output power ranges through load modulation. At a low power level, only the main amplifier is turned on. Therefore, the load impedance of the main amplifier is twice that at the high power level, and the gain is doubled. However, the input power of the main amplifier becomes half of the total input power due to the use of an input power splitter. When the auxiliary amplifier is turned on at high power level, the gain of the main amplifier is reduced due to the reduced load impedance, whereas the total gain is compensated by the auxiliary amplifier operation. Ultimately, the gain of the Doherty PA is constant throughout the input power

range. Thus, the Doherty PA can achieve a linear AM-AM response as a function of the input power.

The main and auxiliary amplifiers have a nonlinearity like other class AB, B, or C amplifiers. However, the nonlinearity of each amplifier can be cancelled out by the destructive combination of differently biased amplifiers. The transfer functions of the main and auxiliary amplifiers can be modeled using a Taylor series expansion equation, as follows:

$$\begin{aligned} I_{out}(v_{in}(t)) &= \frac{dI_{DS}}{dV_{GS}} \cdot v_{in}(t) + \frac{1}{2!}\frac{d^2 I_{DS}}{dV^2{}_{GS}} \cdot v_{in}^2(t) + \frac{1}{3!}\frac{d^3 I_{DS}}{dV^3{}_{GS}} \cdot v_{in}^3(t) + \cdots \\ &= g_{m1} \cdot v_{in}(t) + g_{m2} \cdot v_{in}^2(t) + g_{m3} \cdot v_{in}^3(t) + \cdots \end{aligned} \tag{4.3}$$

where v_{in}, g_{mn}, and I_{out} are the input voltage, the n-th order coefficients of the nonlinear transconductance, and the output current, respectively.

Fig. 4.4(a) shows the third-order trans conductance coefficient (g_{m3}) trace of a standard MOSFET as function of the gate bias voltage. This parameter is related to the third-order harmonic and the generation of intermodulation distortion (IMD) signals. As shown in Fig. 4.4(a), its polarity changes according to the gate bias. With the proper combination of the main and auxiliary amplifiers, IMD3 signals can be cancelled, as like Fig. 4.4(b). To understand the cancellation operation of the third-order IMD in the spectrum domain, the input two-tone signals are expressed as:

$$v_{in}(t) = A\{\cos(\omega_1 t) + \cos(\omega_2 t)\}. \tag{4.4}$$

When two-tone signals are injected into the main and auxiliary amplifiers, the third order IMD3 signals generated by the main and auxiliary amplifiers can be calculated. To clarify this, it is assumed that this is an ideal memoryless amplifiers. In this case, the upper and lower IMD3 signals will be the same. Therefore the upper third-order IMD3 signals of the main and auxiliary amplifier at $2(\omega_2 - \omega_1)$ in terms of $I_{out}(v_{in})$ are given as follows,

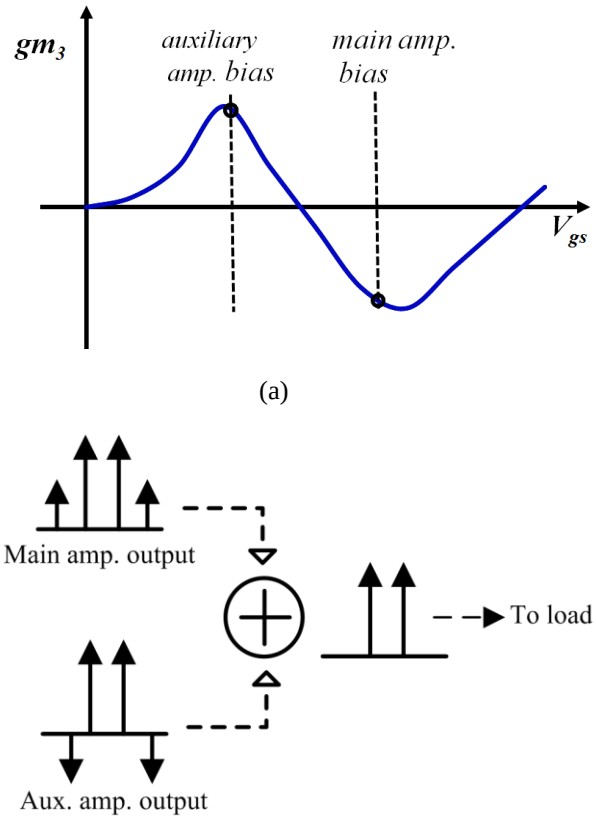


Fig. 4.4. (a) Third-order transconductance coefficient trace of a general MOSFET according to the bias point and (b) output fundamental and IMD3 signals of main and auxiliary amplifiers with the phase in the spectrum domain.

$$I_{out\_main}(2\omega_2-\omega_1)=\frac{3}{4}g_{m3\_main}\cdot A^3\cdot e^{j\theta_{main}}$$
$$I_{out\_aux.}(2\omega_2-\omega_1)=\frac{3}{4}g_{m3\_aux.}\cdot A^3\cdot e^{j\theta_{aux.}} \quad (4.5)$$

where θ_{main} and $\theta_{aux.}$ are the phases of the IMD3 signals, which depend on the g_{m3_main} and $g_{m3\_aux.}$ values of the main and auxiliary amplifiers, respectively. As shown in Fig. 4.4(a), the g_{m3} of a class C biased auxiliary amplifier has an opposite polarity relative to that of the class AB biased main amplifier. As a result, the third-order IMD3 signals are cancelled out by the combination of the opposite phase signals. Fig. 4.4(b) shows the output fundamental signals and the IMD3 signals at the output port of each amplifier with a phase in the spectrum domain. Although this g_{m3} cancellation scheme cannot be perfect due to memory effect and PVT variation in a real case, the linearity improvement effect was proved in many previous studies [55]-[62].

4.2 CMOS Doherty Amplifier Design

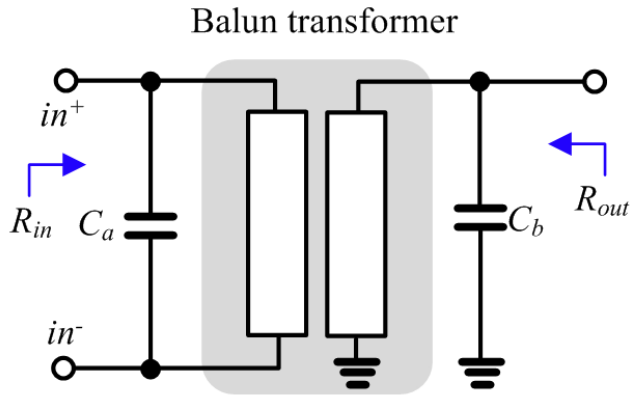
4.2.1 Load Modulation with Variable Balun Transformer

In the CMOS amplifier design, a single amplifier is not sufficient for the high output power requirement due to its low breakdown voltage. In addition, since there is no back-via, which is used for a ground connection in the HBT and GaAs process, the gain reductions caused by the ground wire bonding degeneration effect cannot be ignored. Thus, the CMOS amplifier relies on differential or cascode structure to prevent wire bonding degeneration loss and avoid the breakdown issue.

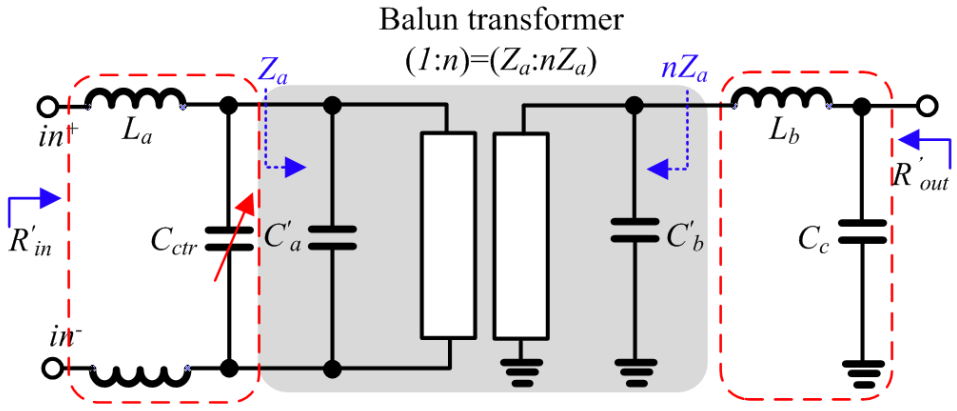
Additionally, the antenna and filter connected to the output port of the PA are usually single-ended circuits. As a result, a balun transformer is necessary to connect the differential amplifier to the single-ended circuits and to convert the optimum load impedance of the PA to 50 Ω.

Recent CMOS PAs use a coupled transformer to achieve output impedance matching instead of on-chip passive components with a low Q-factor. Fig. 4.5(a) shows the conventional balun transformer used for the output matching of the amplifier. In order to implement an impedance inverter for load modulation without a λ/4 transmission line, the input resistance of the transformer (R_{in}) has to be changed from $2 \cdot R_{opt}$ to R_{opt} while the output resistance of the transformer (R_{out}) has to be changed from R_{out} to $2 \cdot R_{out}$. Fig. 4.5(b) shows the proposed variable balun transformer (VBT) for the active load modulation. In the proposed VBT, downward and upward *LC* transformers have been added at the input and output ports of the conventional balun, respectively. In addition, the VBT has bigger capacitors (C'_a and C'_b) compared to those (C_a and C_b) of the conventional transformer to achieve matching using the additional inductor (L_a, L_b). A simplified equivalent circuit of the proposed VBT can be represented as shown in Fig. 4.5(c). To simplify the analysis, an equivalent input impedance is considered in Fig. 4.5(c). The input impedance of VBT, Z'_{in_s}, is given as follows:

$$
\begin{aligned}
Z'_{in\_s} &= \left(Z_a \,//\, -j\frac{1}{\omega C_{ctr}} \right) + j\omega L_a \\
&= \frac{g_a}{g_a^2 + \omega^2 (b_a + C_{ctr})^2} - j\omega \cdot \frac{b_a + C_{ctr}}{g_a^2 + \omega^2 (b_a + C_{ctr})^2} + j\omega L_a
\end{aligned}
\qquad (4.6)
$$



(a)



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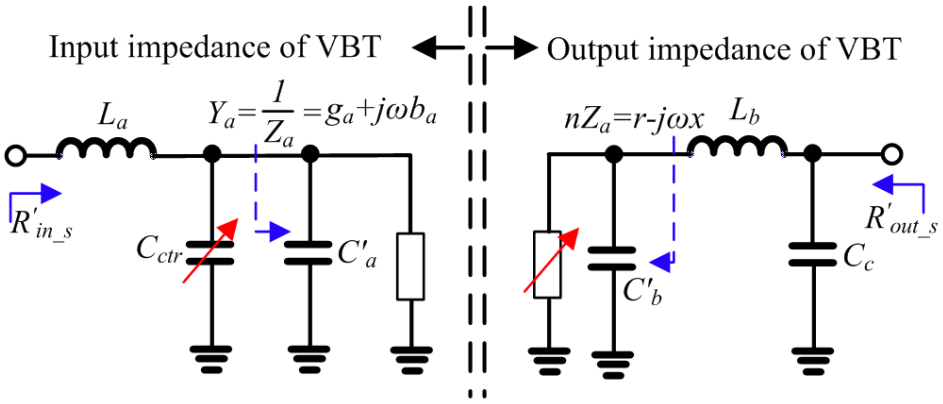


(c)

Fig. 4.5. (a) Conventional balun transformer for output matching, (b) architecture of the proposed VBT, and (c) simplified equivalent circuit of the VBT.

where

$$Y_a = \frac{1}{Z_a} = g_a + j\omega b_a \tag{4.7}$$

Z_a , Y_a, and C_{ctr} are the input impedance and admittance of the 1:n coupled transformer, and variable capacitance to achieve variable impedance transformation, respectively. In addition, g_a and ωb_a are the conductance and susceptance of the Y_a, respectively. If the C_{ctr} is increased from 0 pF, an imaginary part of Z'_{in_s} at C_{ctr} of 0 pF should be removed by the serial inductance (L_a). As a result, the L_a can be selected as follows:

$$L_a = \frac{b_a}{g_a^2 + \omega^2 (b_a)^2} \tag{4.8}$$

Hence, the imaginary part of Z'_{in_s} is rewritten as follows:

$$-j\omega \cdot \left(\frac{b_a + C_{ctr}}{g_a^2 + \omega^2 (b_a + C_{ctr})^2} - \frac{b_a}{g_a^2 + \omega^2 (b_a)^2} \right) \tag{4.9}$$

In addition, the input resistance (R'_{in_s}) is written as follows:

$$\begin{aligned} R'_{in\_s} &= \frac{g_a}{g_a^2 + \omega^2 b_a^2}, && @\ C_{ctr} = 0 \\ R'_{in\_s} &= \frac{g_a}{g_a^2 + \omega^2 (b_a + C_{ctr})^2}, && @ C_{ctr} \neq 0 \end{aligned} \tag{4.10}$$

From (4.9) and (4.10), we can calculate the optimum Z_a and C_{ctr} for target

of impedance variation. Similarly, the output impedance of VBT (R'_{out_s}) can be expressed as follows:

$$R'_{out\_s} = \frac{nZ_a}{\left(nZ_a \cdot \omega C_c\right)^2 + \left(\omega^2 L_b C_c - 1\right)^2} \tag{4.11}$$

In this equation, nZ_a, L_b, and C_c are the output impedance of the 1:n coupled transformer, and the inductance and capacitance of the upward LC transformer, respectively.

The input and output impedances of VBT can be explained qualitatively via (4.10) and (4.11). As C_{ctr} increases, the R'_{in_s} is decreased and R'_{out_s} is increased. Fig. 4.6 shows simulated input and output impedance variations according to C_{ctr} at 2.4 GHz. The variation of C_{ctr} in the VBT network mostly affects the real part of the impedance with minimal changes of the imaginary part of the impedance, as shown in Fig. 4.6. An HFSS electromagnetic (EM) simulation was conducted to design the coupled balun transformer. The designed transformer has an insertion loss of 1.5 dB at 2.4 GHz. The values used for L_a, L_b, and C_c are 0.15 nH, 1.8 nH, and 2.0 pF, respectively. As shown in Fig. 4.7, the total resistance transforming ratio of VBT is from 50:50 Ω to 22:98 Ω for a C_{ctr} variation range of 0 pF to 1.4 pF. Therefore, the resistance variation of the proposed VBT can be controlled properly for the load modulation of the Doherty PA by C_{ctr}. Additionally, Fig. 4.8 shows the phase transfer characteristic of VBT as the function of C_{ctr} in the range of 0 pF to 1.4

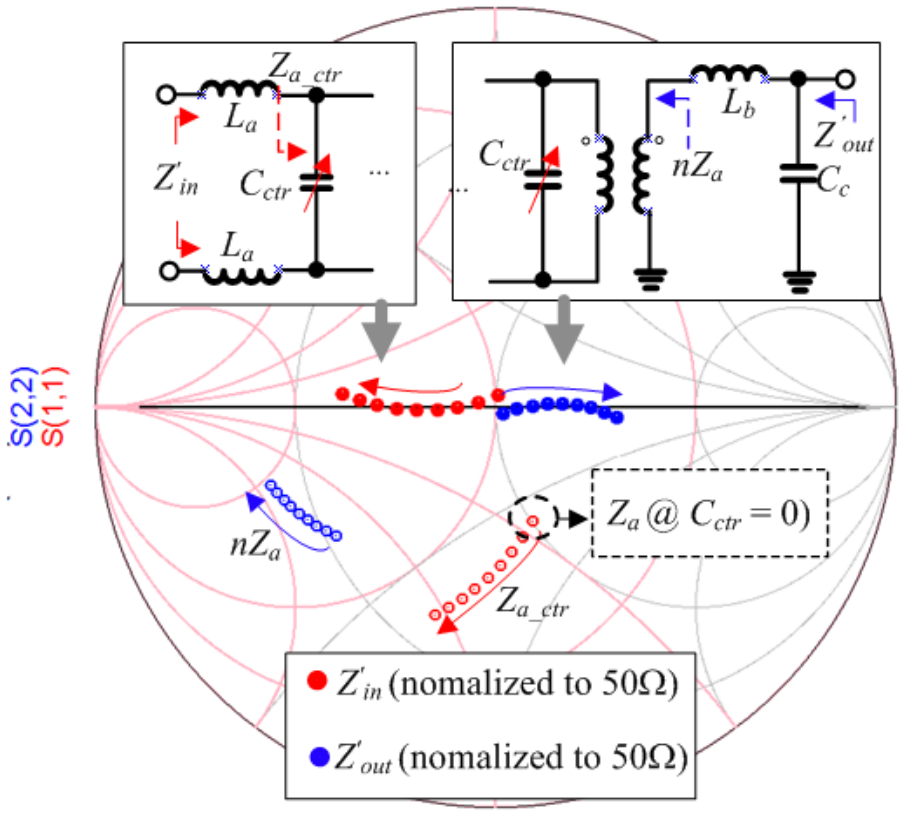


Fig. 4.6. Simulated input and output impedance variations of VBT according to C_{ctr} variation.

pF. Although the VBT has 23.1° of phase variation throughout the C_{ctr} range, the phase should be considered only within auxiliary amplifier operating range. When the auxiliary amplifier is operated at full capacity, C_{ctr} has to be 1.4 pF and the balun of the auxiliary amplifier has to be matched to obtain 180° phase transfer characteristic. Thus, the phase difference between two baluns is 5.4° when the PA is operated at maximum output power. This phase error can be compensated by tuning the matching network of the auxiliary amplifier. As a result, the proposed Doherty PA can be implemented at small size since it does

not require bulky λ/4 transmission lines and additional phase compensation circuit on the RF signal path of the auxiliary amplifier.

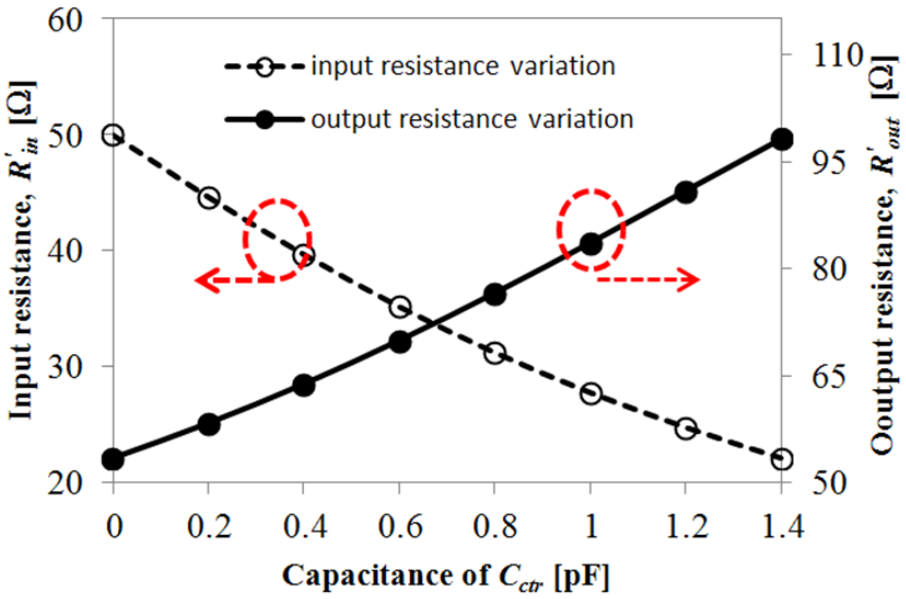


Fig. 4.7. The input and output resistance variation curves, with respect to value of C_{ctr}.

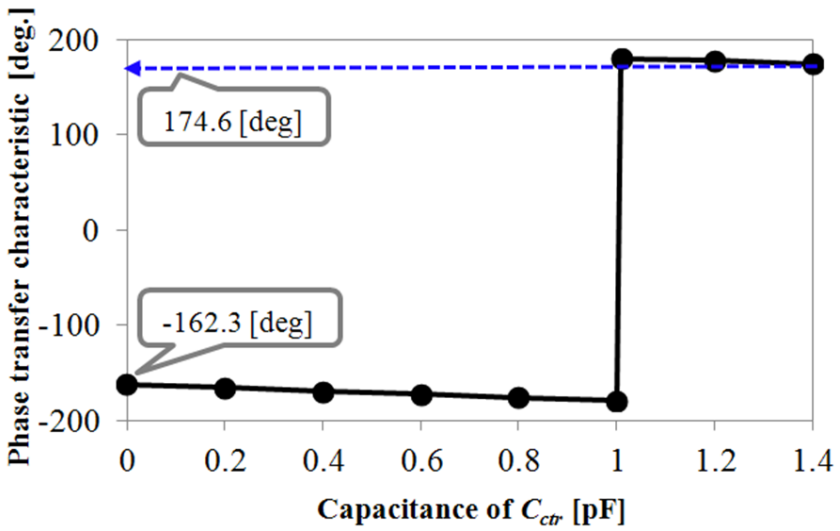


Fig. 4.8. Simulated phase-transfer characteristic of VBT as function of C_{ctr}.

4.2.2 Auxiliary Amplifier with Adaptive Bias

The load modulation of the Doherty PA is based on the amounts of current of the active devices with respect to the power level. For the proper load modulation of Doherty PA, the auxiliary amplifier rather than the main amplifier has important role in delivering an appropriate fundamental current [69]-[72]. As mentioned in sub-section 4.1, the drain current of the auxiliary amplifier has to be zero in the low-power region and must be identical to that of the main amplifier at the maximum input power level. However, in a real situation, the drain current of the auxiliary amplifier is slightly lower than that of the main amplifier at the maximum input power level due to the lower bias of the auxiliary amplifier. In addition, a class C biased auxiliary amplifier with a cascode structure does not have a zero drain current at the desired backed off power level due to the low thresh-hold voltage (V_{th}) and the gain of the common gate stage. For these reasons, an adaptive biased CMOS auxiliary amplifier can improve the efficiency at a backed-off power level and can increase the gain at the maximum input power level.

As shown in Fig. 4.3(a), the ideal transfer characteristic of the auxiliary amplifier can be expressed simply as follows.

$$\begin{aligned} I_{out}^{aux.} &= 2G_m \cdot (v_{in} - \frac{V_{in,\max}}{2}) \quad @ \ \frac{V_{in,\max}}{2} < v_{in} < V_{in,\max} \\ I_{out}^{aux.} &= 0 \qquad @\, 0 < v_{in} < \frac{V_{in,\max}}{2}, \end{aligned} \tag{4.12}$$

where G_m denotes the transconductance. If the characteristic of an ideal auxiliary amplifier follows that of the main amplifier, the adaptive G_m of the auxiliary amplifier has to serve the function of v_{in}.

Fig. 4.9(a) shows a simplified schematic and the equivalent circuit of the auxiliary cascode amplifier. As shown in Fig. 4.9(b), the output current of the cascode amplifier can be written as follows.

$$I_{out} = g_{m2}V_2 + g_{mb2}V_{bs2} = \frac{1}{2}k'_{M2}(V_b - V_x - V_{th})^2 \tag{4.13}$$

where

$$k'_{M2} = \mu_{n,M_2} C_{ox,M_2} \frac{W_{M_2}}{L_{M_2}}$$

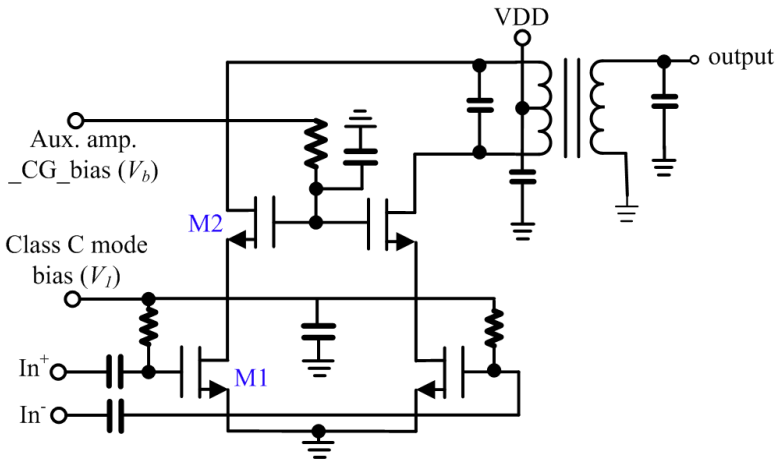
Given that V_x depends on the transconductance of the common source stage, (4.13) can be rewritten as follows.

$$I_{out} = \frac{1}{2}k'_{M2}(V_b + g_{m1}V_{in}r_{o1} - V_{th})^2 \tag{4.14}$$

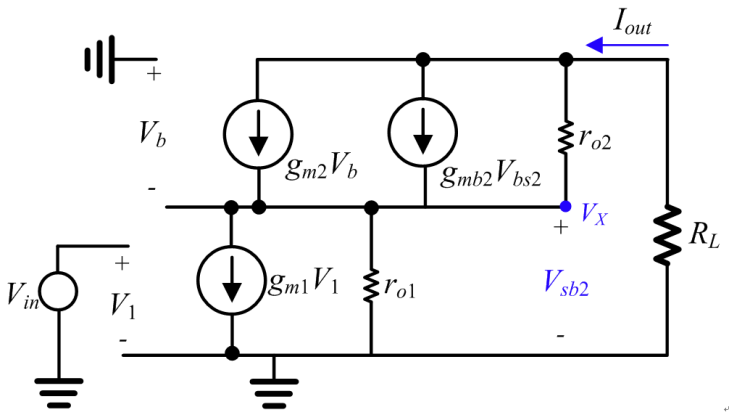
Therefore, the total transconductance of the cascode amplifier is given as shown below.

$$G_m^{cascode} = \frac{I_{out}}{V_{in}} = \frac{1}{2}k'_{M2} \cdot V_{in} \cdot (\frac{V_b - V_{th}}{V_{in}} + g_{m1}r_{o1})^2 \tag{4.15}$$

Thus, G_m of the cascode amplifier can be controlled by adjusting the gate bias of the common gate (CG) stage, which is the function of the input voltage. Fig. 4.10 shows the simulation results for the output current of the auxiliary amplifier with a fixed CG gate bias of 2.8 V and sweeping bias from 0 V to 2.8 V according to v_{in}. In the simulation, the gate bias of the common source stage is set to 0.18 V as class C mode bias. As shown in Fig. 4.10, the current



(a)



(b)

Fig. 4.9 (a) Simplified schematic of an auxiliary amplifier with a cascode structure and (b) simplified equivalent circuit of a single-stage cascode amplifier.

consumption of the auxiliary amplifier with the adaptive bias can reduce the input voltage by half of $V_{in,max}$. As a result, the efficiency of the Doherty PA can be improved in the low-power region. In addition, the reduced gain of the auxiliary amplifier can be offset by injecting the higher gate bias of the CG. Thus, the auxiliary amplifier with the adaptive bias can control the power gain according to the input power level while maintaining the nonlinearity cancellation characteristics.

4.3 Implementation and Measured Results

4.3.1 Implementation

The proposed PA is implemented using TSMC 0.13 μm technology. The

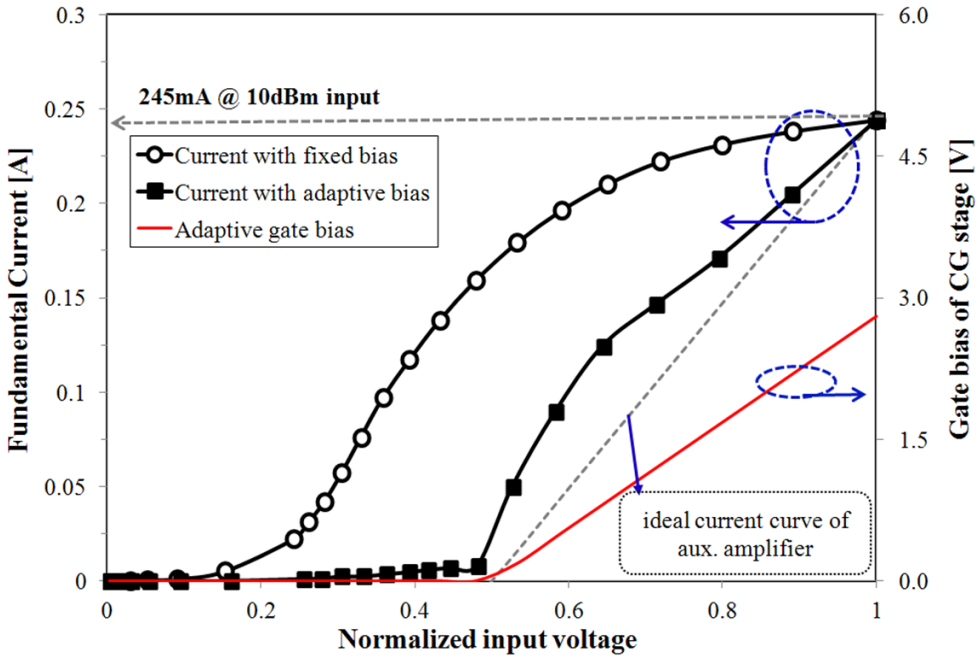


Fig. 4.10. Simulated fundamental currents of an auxiliary amplifier with/without the adaptive gate bias of the common gate stage.

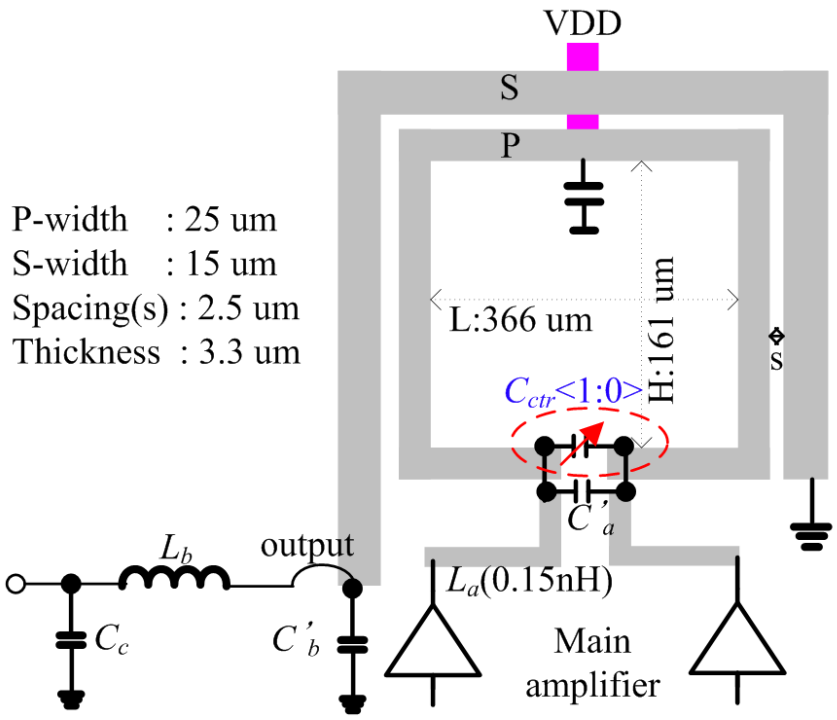


Fig. 4.11. The layout of the VBT network and block diagram with main amplifier and output matching stage

layout of the VBT network with the balun is shown in Fig. 4.11. The metal lines for the balun are ultra-thick metal with a high Q factor and high current capability. In addition, the variable capacitor of the VBT network is implemented with a two-bit switching capacitor array to minimize the nonlinearity caused by the variable capacitor [73]. A thick gate oxide transistor is used as the switching capacitor array and the size is optimized to be operated within available voltage swing range for reliability. Fig. 4.12 shows the simulation result for maximum drain/source voltage swings of the switching transistor with respect to the PA operation. In order to avoid forwarding bias

from body to drain or source while the switch is turned on, the transistor size should be large enough to make small drain voltage swing. However, due to large parasitic capacitance caused by switching transistors, C'_a should be optimized to compensate for the parasitic capacitance by C_{ctr}. Ultimately, a switch size of 360 μm/0.35 μm was selected and additional VBT insertion loss of 0.5 dB is caused by the turn-on resistance of C_{ctr}.

A simplified schematic of the designed PA is shown in Fig. 4.13 with the measurement setup. As shown in Fig. 4.13, differential cascode structures are used for the auxiliary and main amplifiers. The proposed VBT network is connected at the output stage of the main amplifier to serve as an impedance inverter. The power combination with the on-chip balun transformers of the main and auxiliary amplifiers is done with a current combining method, as explained in a previous chapter. Owing to the size reduction, the input transfor-

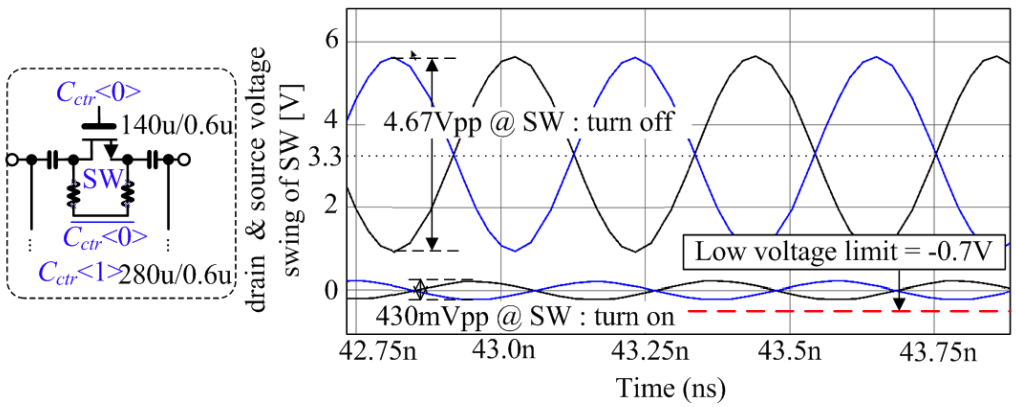


Fig. 4.12 The switching capacitor schematic and maximum V_{ds} voltage swings of that with respect to PA operation.

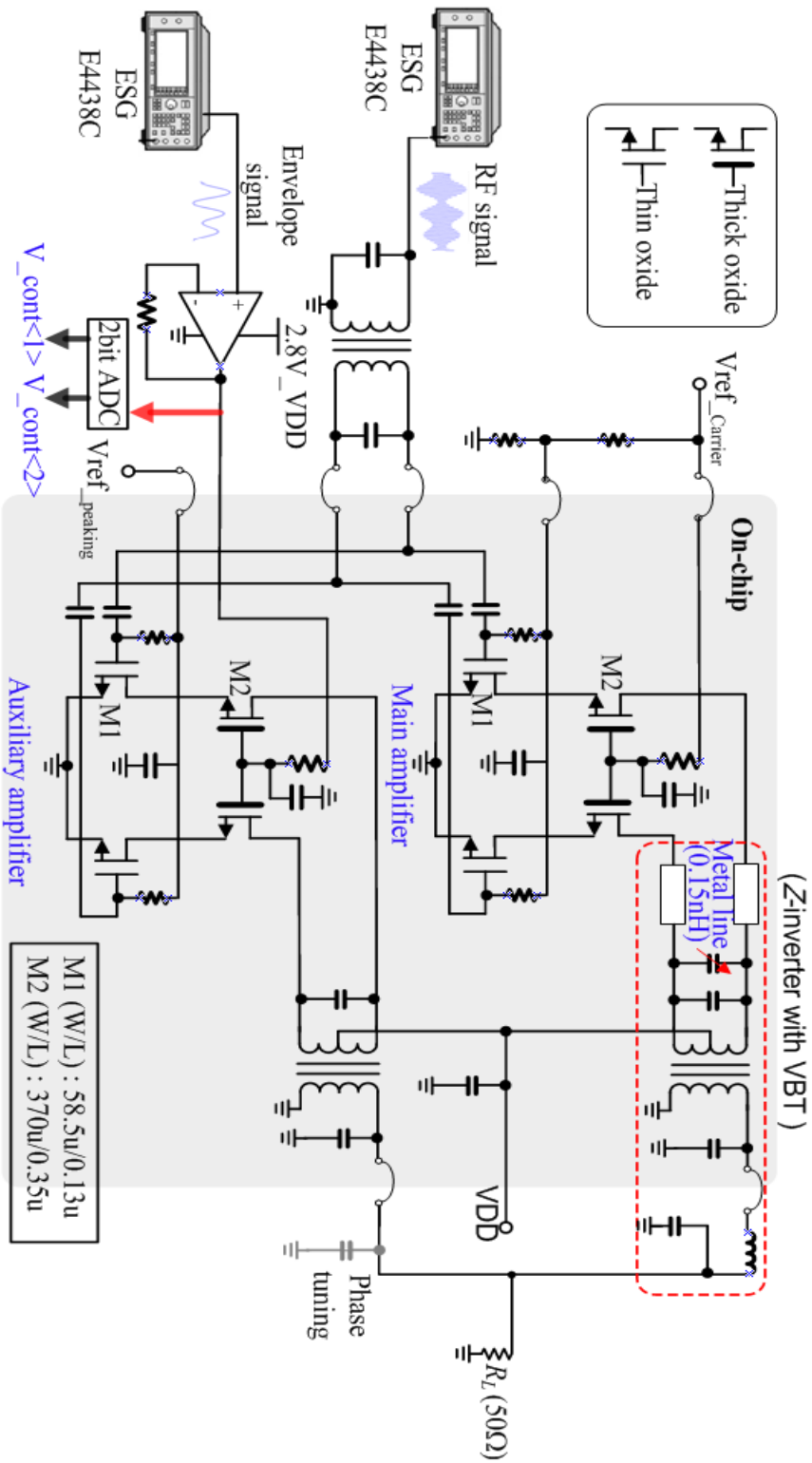


Fig. 4.13. Measurement environment and full schematic of the proposed Doherty amplifier.

mer is implemented with an off-chip component, and a direct driving method is adopted without an additional power splitter. In addition, since the proposed Doherty PA does not require an additional phase compensation circuit, the overall implementation size is very small. The common gate transistors of each amplifier are implemented with a high breakdown voltage device (Lmin= 0.35 μm) to reduce the output voltage swing limitation. In addition, the common source transistors are implemented using an RF transistor with a minimum gate length of 0.13 μm to achieve a desirable RF performance. The common source gate bias of the auxiliary amplifier is set to 0.18 V for class C operation which is below the threshold voltage of 0.3 V, whereas that of the main amplifiers is set to 0.4 V for class AB linear operation. Additionally, the gate bias of the common gate transistor for the main amplifier is set to 2.1 V to reduce the voltage stress on the common source transistors, whereas that of the auxiliary amplifier is adjusted from 0 V to 2.8 V, or fixed at 2.8 V, as mentioned in the previous sub-section. The same transistor size is used in both amplifiers to achieve proper Doherty operation. A photograph of the implemented Doherty PA is shown in Fig. 4.14. The overall chip size, including the pads, is 2,000 × 1,000 μm^2.

4.3.2 Measured Result for CW signal

The fabricated Doherty PA chip is mounted on a FR-4 printed circuit board (PCB) and measured with a single tone continuous wave (CW) of 2.4 GHz. Fig. 4.15 shows the power gain and PAE according to the output power. In the low-

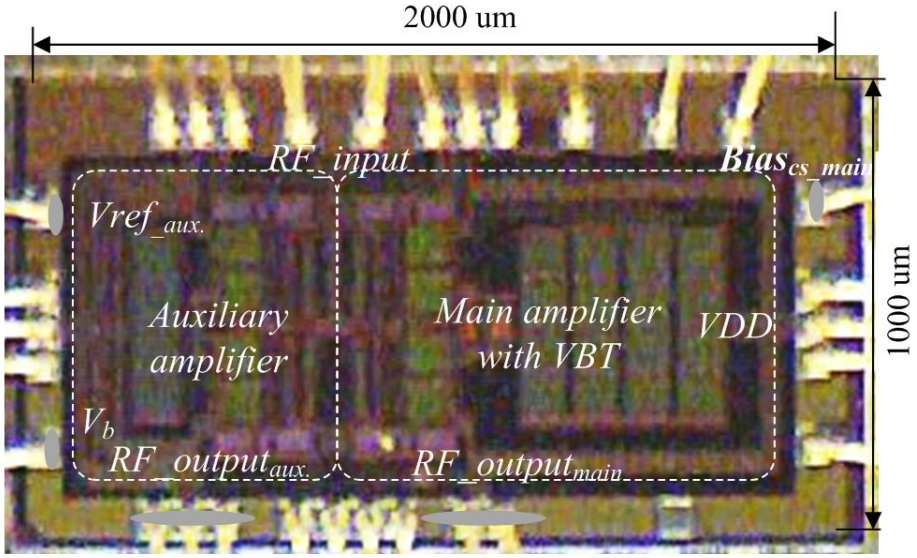


Fig. 4.14. Chip photograph of the implemented Doherty PA.

power mode (LPM), only the main amplifier is operated. Both the switching capacitor of VBT and the auxiliary amplifier are turned off in this mode.

However in the high-power mode (HPM), the main and auxiliary amplifiers are operated at a fixed bias level, and the switching capacitor of VBT is turned on. As shown in Fig. 4.15, the measured output power and PAE at the P_{1dB} in the LPM are 27 dBm and 50.9%, respectively, while those of the fabricated Doherty PA in the HPM are 31.9 dBm and 51%, respectively. Although the difference in the P_{1dB} between the HPM and LPM is 4.9 dB, two efficiency peak curves are obtained. Nonetheless, since the drain current consumption of the auxiliary amplifier with the fixed bias is too high at the LPM, the PAE of the amplifier is reduced rapidly at the transition power level from the LPM to the HPM. In order to reduce the drain current of the auxiliary amplifier at a low-power level, an adaptive bias scheme is used with the CG stage of the

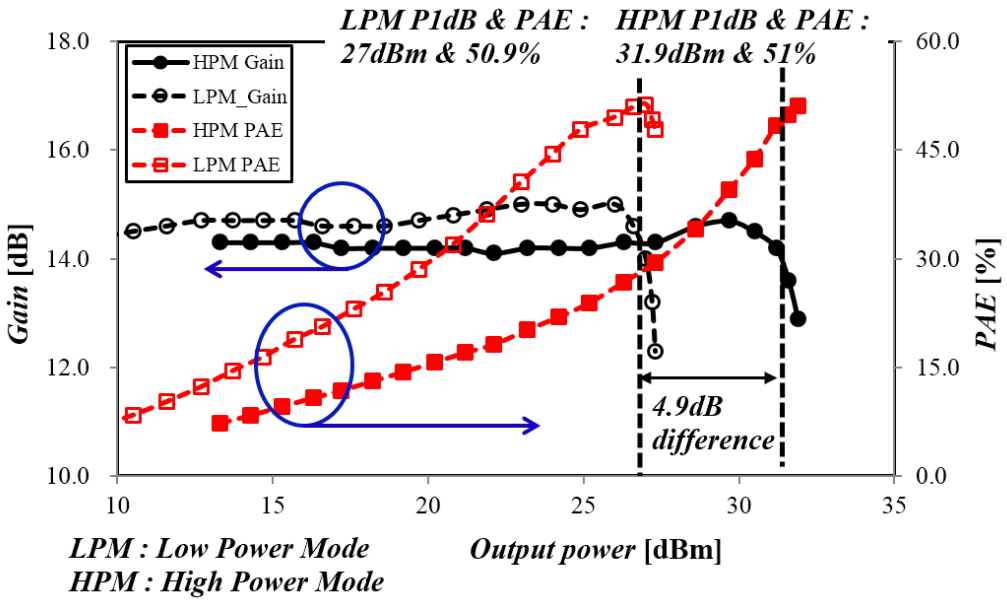
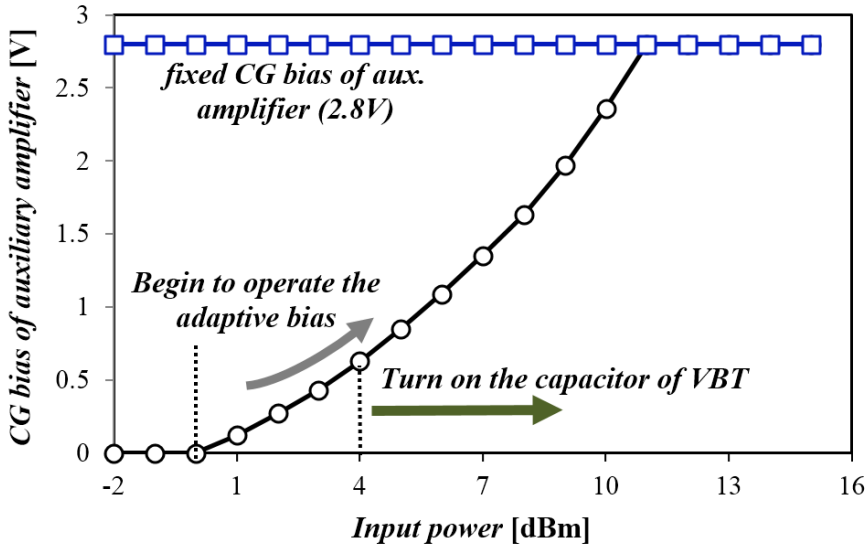


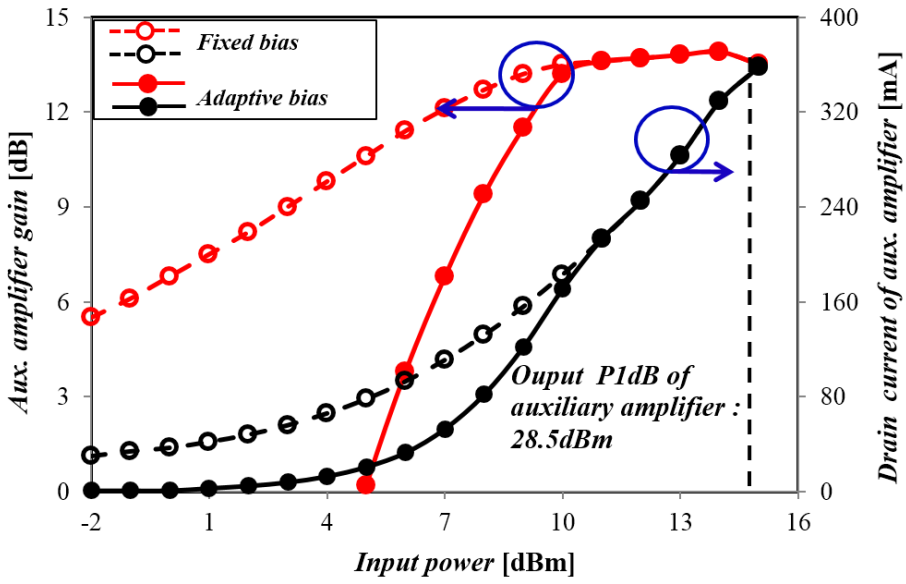
Fig. 4.15. In the switching mode, measured results for the power gain, PAE, and output power (Pout) with the CW signal.

auxiliary amplifier and the switching capacitor of VBT according to the input power level, as shown in Fig. 4.16(a). With the adaptive bias scheme, the auxiliary amplifier is properly turned on at backed-off output power levels, as shown in Fig. 4.16(b). As a result, the drain current and gain of the auxiliary amplifier can be reduced effectively, leading to the ideal operation of the auxiliary amplifier in the low power region. The measured efficiency and power gain performances are illustrated in Fig. 4.17. The PAE of the proposed PA is higher than 25.3% and the gain flatness is less than 1 dB in the backed-off output power region above 12 dB. If the adaptive bias scheme is turned on at higher input power, the efficiency will be better at backed-off power level.

However since the linearity and efficiency at backed-off power level should be concerned together, the turn-on power level of adaptive bias is determined by



(a)



(b)

Fig. 4.16. (a) Aux. CG bias voltage shape in the fixed bias mode and the adaptive bias mode, and (b) measured power gain and drain current of the auxiliary amplifier with/without adaptive bias.

trade-off between efficiency and linearity.

A two-tone test is performed at 2.4 GHz with a tone spacing of 5 MHz. The measured third-order IMD characteristics according to the output power are shown in Fig. 4.18. Relatively good linearity characteristics were obtained in the low-power region for the LPM case, whereas this was noted in the high-power region in the HPM case. For good linear operation with a third-order IMD of 28 dBc, the switching-mode PA must be changed from LPM to HPM at an output power of 15 dBm per tone. With the adaptive bias scheme, the fabricated Doherty PA can keep the IMD3 under 28 dBc up to an output power of 26.3 dBm per tone.

4.3.3 Measured Results for Modulation Signal

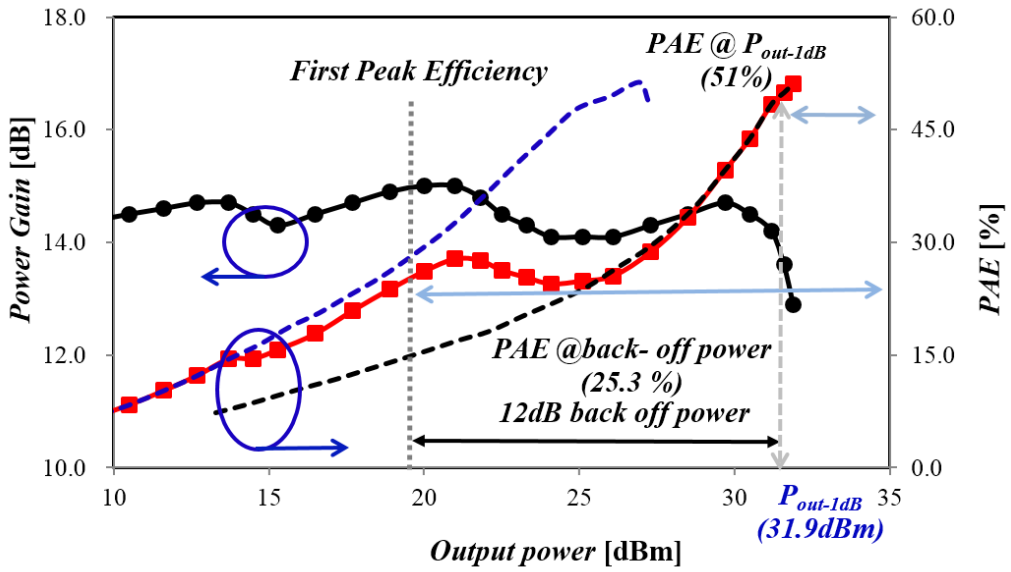


Fig. 4.17. Measured CW characteristics of the proposed Doherty amplifier with adaptive bias control.

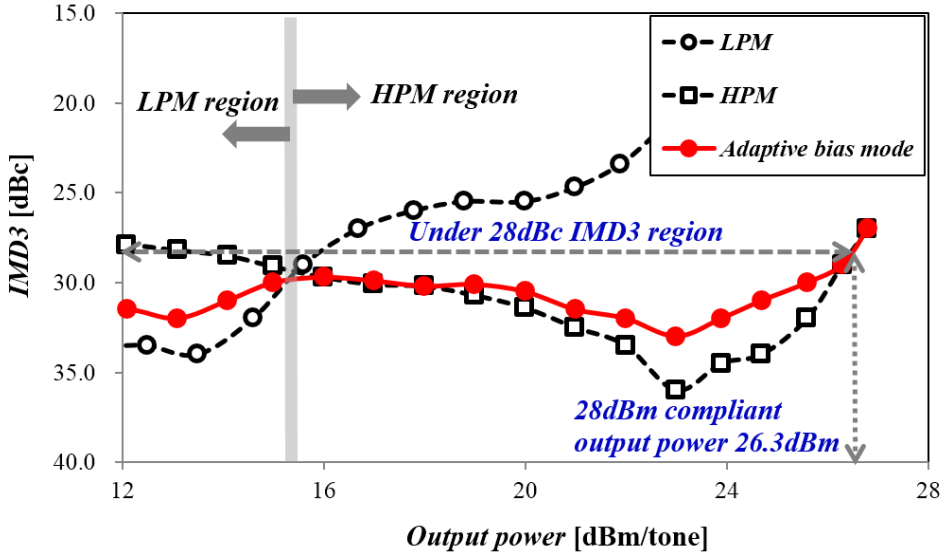
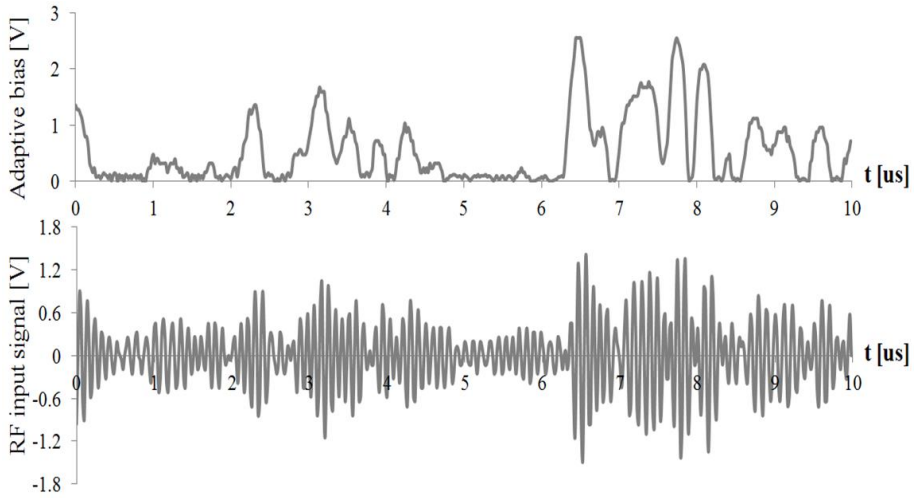


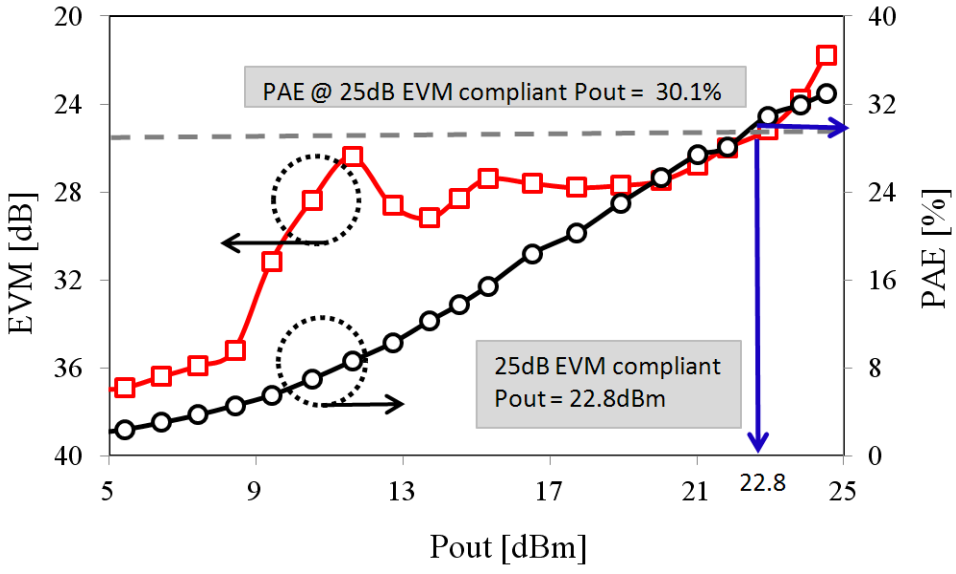
Fig. 4.18. Measured IMD3 performances for two-tone signals with a 5 MHz tone spacing at 2.4 GHz.

Finally, to verify whether the linearity characteristic of the fabricated Doherty PA is suitable for 802.11g WLAN system applications, a high-level modulation signal was applied. The modulation signal source was an OFDM signal with a data rate of 54 Mb/s using a 64 QAM. The measured CG stage-gate bias trace is compared with the OFDM modulated RF signal amplitude, as shown in Fig. 4.19(a). The CG stage-gate bias trace follows the envelope of the OFDM modulated RF signal well. The EVM at 2.4 GHz is shown in Fig. 4.19(b). The measured average output power that satisfies the EVM requirement of 25 dB is around 22.8 dBm, where the PAE at the EVM compliant output power is 30.1%. The measured EVM is lower than the expected value based on CW or two tone test due to AM-PM performance degradation caused by discontinuous load modulation. However, the proposed

amplifier demonstrates that it has high efficiency at an EVM compliant output power level of 25 dB.



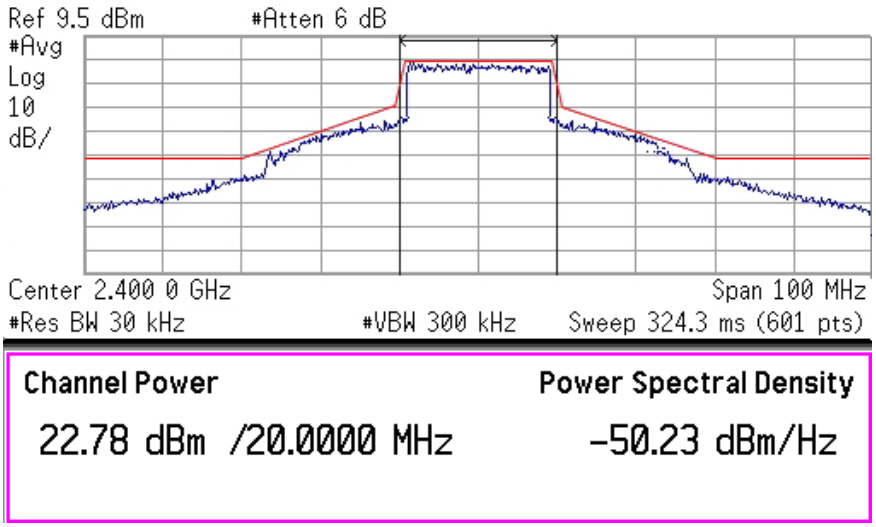
(a)



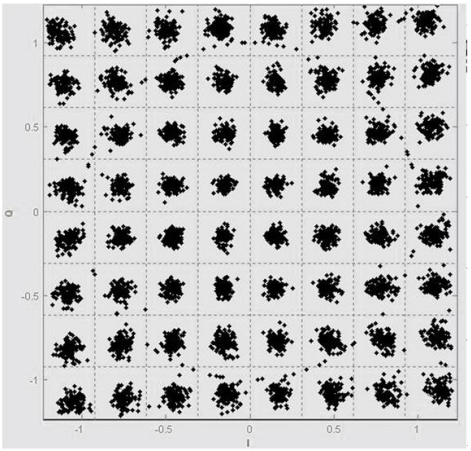
(b)

Fig. 4.19. (a) Measured CG stage gate bias of the auxiliary amplifier as compared to the modulated RF input signal amplitude for 802.11g WLAN and (b) measured EVM and PAE performances of the fabricated PA.

Fig. 4.20(a) shows the output spectrum mask of the fabricated Doherty PA with a channel average power of 22.8 dBm and an adjacent channel leakage ratio (ACLR) of -25 dBc. In addition, the constellation error of the amplifier at an average output power of 22.8 dBm is shown in Fig. 4.20(b). As a result, the



(a)



(a)

Fig. 4.20. (a) Measured output spectrum mask of the amplifier, and (b) constellation error of the amplifier with 64 QAM OFDM.

proposed Doherty PA satisfies the system specifications of 801.11g without a digital pre-distortion (DPD) algorithm.

The electrical performances of the fabricated Doherty PA are compared with previous research results in Table 4.1. The performances of the proposed Doherty PA are superior to those shown in table in terms of PAE at an EVM compliant output power of 25 dB and at the peak power. Although the PAE performance of proposed Doherty PA without considering actual input balun loss and on-chip matching loss cannot be fairly comparable with previous works, those loss factors have a small impact on PAE. Therefore, the proposed Doherty PA can be good candidate for highly efficient CMOS power amplifier.

4.4 Summary and Discussion

A conventional Doherty PA with a quarter-wavelength transformer has limitations in terms of CMOS implementation due to its size and bandwidth. The proposed VBT network is employed as a solution to overcome these limitations. In addition, an adaptive bias control technique necessary to obtain proper linearity and efficiency levels is demonstrated. The prototype achieves a peak power in excess of 31.9 dBm and satisfies the 802.11g linearity requirement up to an output power of 22.8 dBm. In addition, the measured results clearly show that the prototype is capable of superior efficiency levels for WLAN applications. Thus, the CMOS Doherty PA with VBT and an adaptive bias control technique is very effective for high-efficiency CMOS power amplifier designs for WLAN applications.

TABLE 4.1. 2nd comparison of CMOS PAs for WLAN application.

Ref.	Process	Supply [V]	P_{sat} [dBm]	Peak PAE [%]	P_{out} / PAE @ 25 dB EVM	Size [mm^2]	Linearization technique
JSSC 2009 [61]	65 nm CMOS	3.3 V	31.5 dBm	25	22.7 dBm/16%	N/A	g_m (class AB ~ B)
ISSCC 2010 [59]	65 nm CMOS	3.3 V	33.5 dBm	37.6	26 dBm/20%	15	g_m (class AB ~ B)
ESSCIRC 2010 [60]	0.25 µm	3.3	20.5	26.7	13 dBm/19%	1.92	voltage combining Doherty
*RFIC 2*008 **[77]**	SeGe HBT	3.3 V	30.0 dBm	33	18.5 dBm/19 %	3.68	adaptive bias
Chapter 3	180 nm CMOS	3.3 V	29.5 dBm	41.7	22 dBm/22 %	1.5	g_m (class A and C)
This work	**0.13 µm CMOS**	**3.3 V**	**31.9 dBm**	**51**	**22.8 dBm/30.1%**	**2**	**current combining Doherty**
* 801.11g specification		Minimum EVM with 64-QAM-OFDM signal (54 Mbps): 25 dB. Maximum transmitted output power: 100 mW (20 dBm).					

CHAPTER 5

A FULLY INTEGRATED HIGH EFFICIENCY RF POWER AMPLIFIER FOR WLAN APPLICATION IN 40 nm STANDARD CMOS PROCESS

This chapter describes the PA design techniques using dual gate bias to realize high power and high efficiency in a small area using the standard 40 nm CMOS technology for 802.11g WLAN application. The designed PA consists of a high power amplifier (HPA) for high linear operation, a programmable gain amplifier (PGA) for output power adjustment, and bypass switches to support the external PA mode, as shown in Fig. 5.1. In addition, an internal balun is designed for impedance transforming and combining differential output signals to a single load (R_L). The concept and principle of designed PA will be explained and validated by

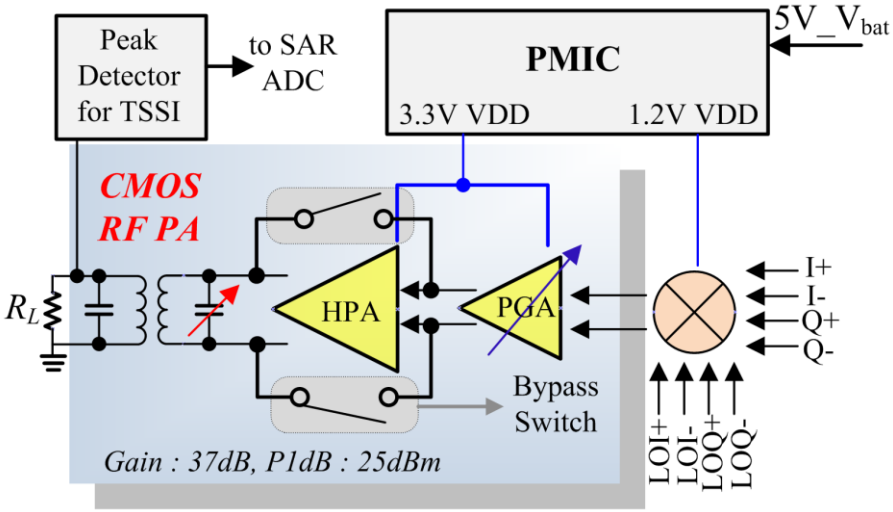


Fig. 5.1. Simplified block diagram of fully integrated power amplifier.

measurement in this chapter.

5.1 CMOS PA using Dual Gate Bias.

5.1.1 Operation Principle of Proposed HPA

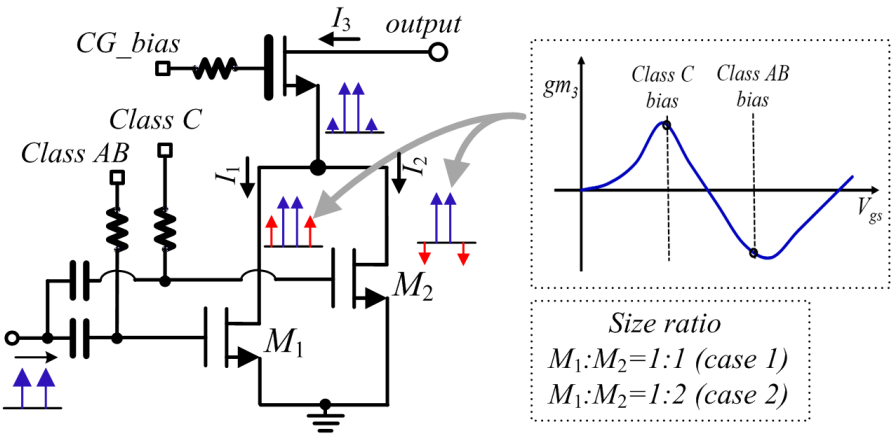
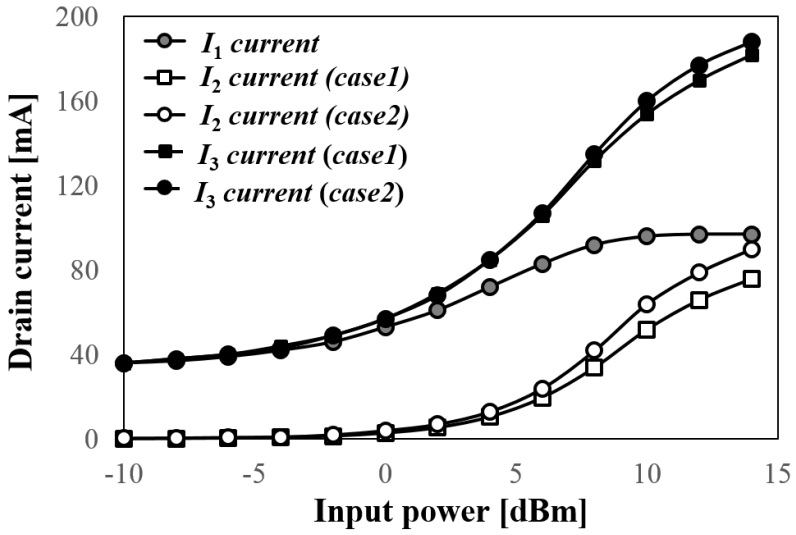
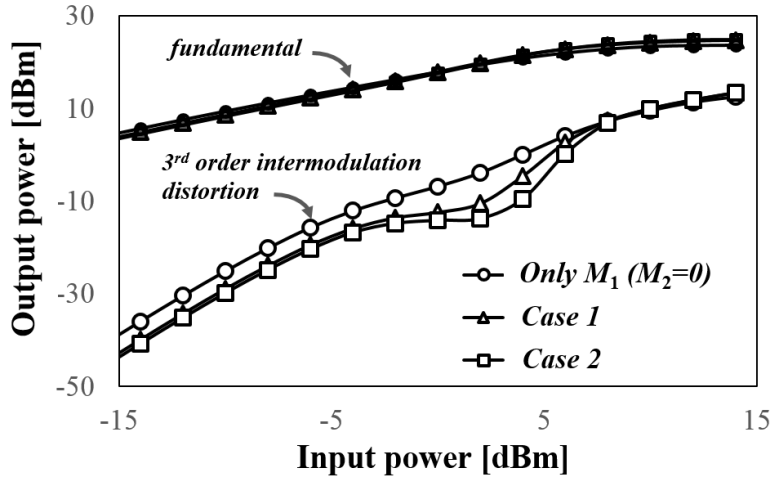


Fig. 5.2. Simplified schematic of HPA and principle of g_{m3} cancellation.

Fig. 5.2 shows the operation principle of an un-even biased HPA. This HPA is a pseudo-differential amplifier with a cascode configuration. A thick gate oxide transistor was used for the common gate (CG) stage to avoid the breakdown issue, whereas a thin gate oxide transistor with a minimum gate length of 40 nm was used for the common source (CS) stage to obtain the maximum RF gain. In addition, the transistors of the CS stage are separated into main transistor (M_1) and auxiliary transistor (M_2), and the gates of M_1 and M_2 transistors are biased at class AB of 0.65 V and class C of 0.15 V, respectively. Although M_1 and M_2 transistors have different nonlinear characteristics, the nonlinear factors of each transistor can be destructively combined due to the different biases, as shown in Fig. 5.2 [74]-[75].



(a)



(b)

Fig. 5.3. Simulation results : (a) simulated drain current flow curves for each transistors and (b) simulated power curves for fundamental and 3rd order intermodulation distortion signal power based on M_2 sizes (with 5 MHz tone spacing).

In addition, since M_2 does not consume the current at the low power region by a gate bias voltage that is lower than the threshold voltage (V_{th}), the average efficiency of the PA can be improved in the overall power range. However, since

the transconductance (g_m) of M_2 is smaller than that of M_1, the size of M_2 should be optimized to obtain the proper linearization effect. Fig. 5.3(a) shows the drain current simulation results of the HPA transistors, and Fig. 5.3(b) shows the simulated power curves of the fundamental signal and the 3rd order intermodulation distortion signal according to the input power levels. As shown in Fig. 5.3, the amplifier with M_1 and M_2 transistors of 1:2 size ratio (case 2) can be achieved higher linear output power than that with 1:1 size ratio (case 1). As a result, the proposed technique can improve the average efficiency and linearity simultaneously by using differently biased M_1 and M_2 transistors with a 1:2 size ratio.

5.1.2 Fully Integrated CMOS PA Circuit

Fig. 5.4 shows an overall schematic of the designed CMOS PA. The programmable gain amplifier (PGA) is implemented by employing a variable resistor at the input stage of the drive amplifier (DA). The DA is designed to be available for a 3.3 V supply voltage and to support enough linear power with an OIP3 of 22 dBm. The variable resistor for the RF gain control of 18 dB is realized with ladder type 2-bit resistors so that the output power of the CMOS PA can be controlled by 6 dB step. Finally, the implementation of a bypass switch connected at the HPA output node is very challenging due to reliability problems [76]-[78]. When the bypass switch is turned off and the HPA is turned on, the drain node of the switch transistor has a large voltage swing, and it leads to a forwarding bias between the body and drain nodes. To address these reliability issues of the switch

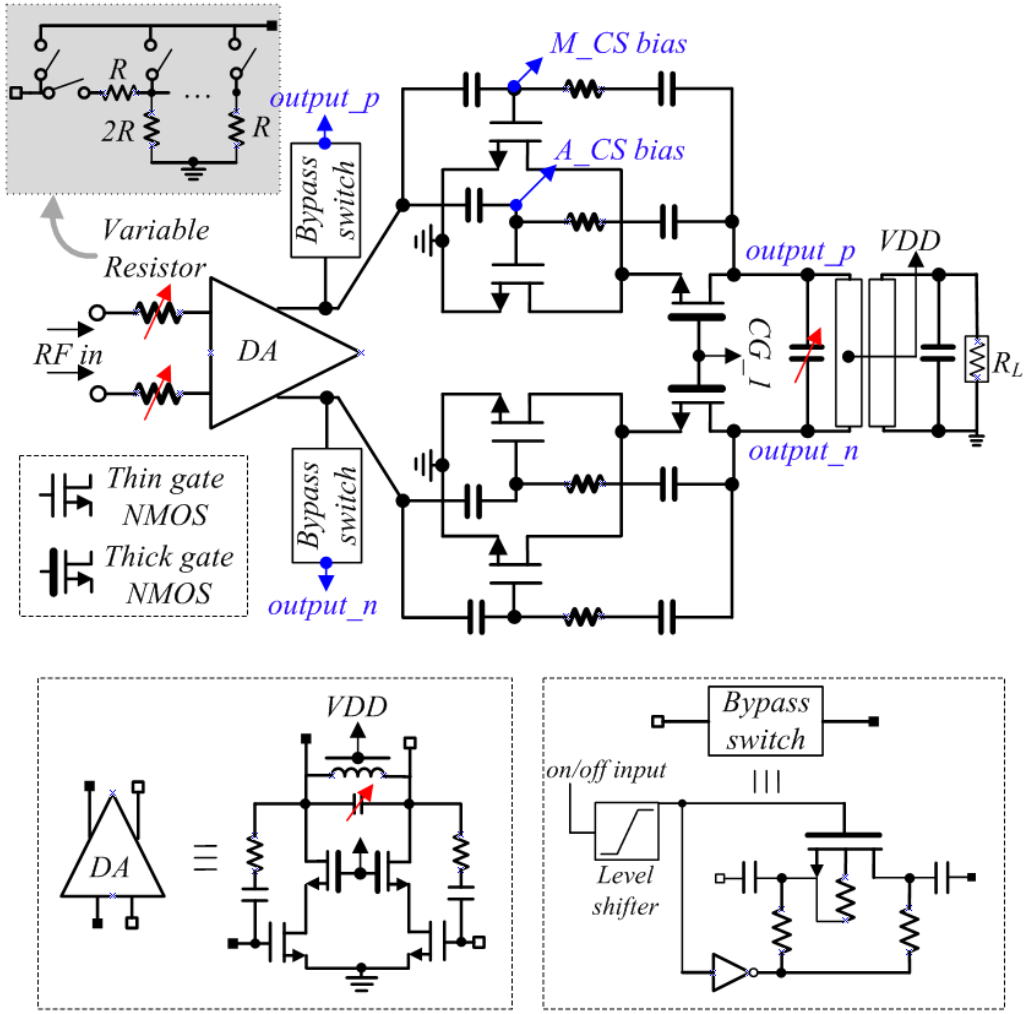


Fig. 5.4. Overall schematic of the designed CMOS power amplifier.

transistor, it has been designed to fix the DC bias at the drain/source nodes according to the on/off operations, as shown in Fig. 5.4. The output internal balun is designed using the EMX tool so that a differential impedance of 20 Ω is transformed to a single output impedance of 50 Ω.

5.2 Measurement Results

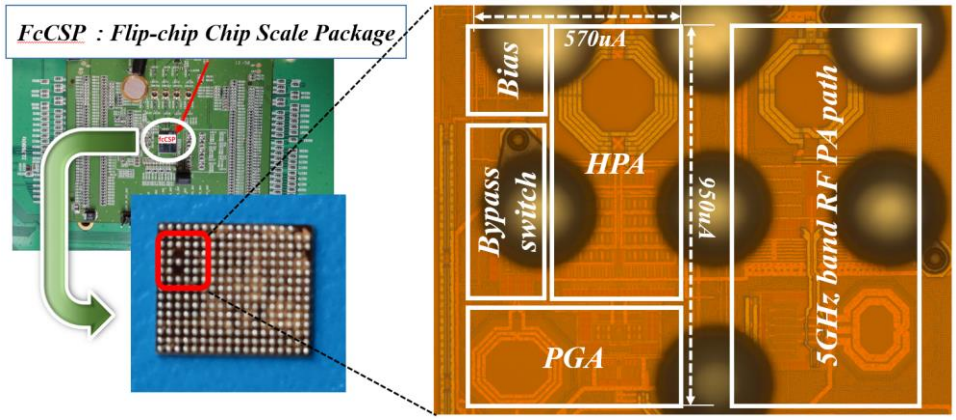


Fig. 5.5. Photographs of the designed WLAN SoC with FcCSP package and fabricated CMOS PA chip.

The proposed CMOS PA was fabricated in the standard 40 nm CMOS process and was packaged in a flip chip chip scale package (FcCSP). The test board and chip photographs of the PA are shown in Fig. 5.5. The two stage PA is implemented

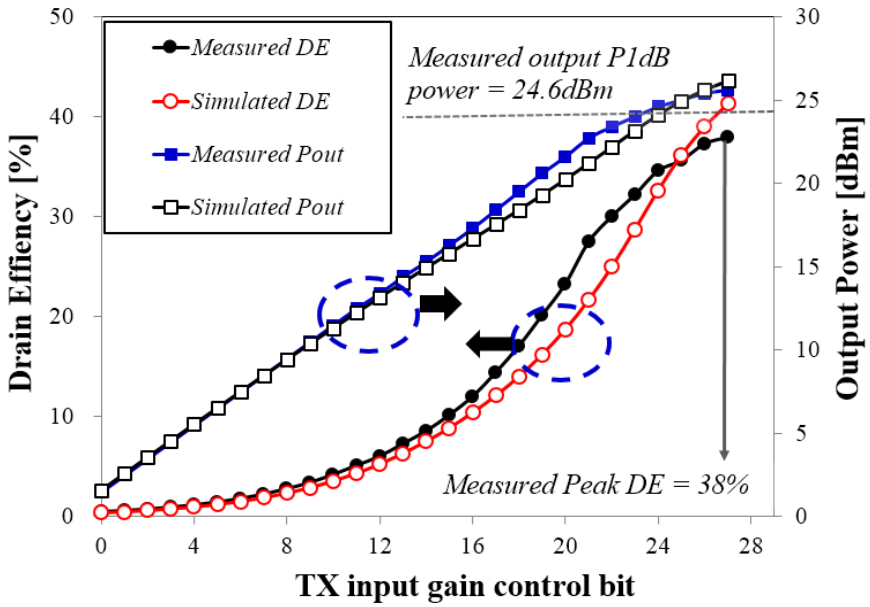


Fig. 5.6. Measurement results of output power and drain efficiency performances with a continuous wave of 2.445 GHz

in a small area of 0.57 × 0.97 mm^2 including the output balun and bypass switch, so that additional off-chip matching components are not required. The fabricated PA is mounted on an FR-4 PCB for the measurement.

The measured output power and drain efficiency (DE) traces according to the RF input power level are shown in Fig. 5.6. The RF input power is adjusted using an analog variable gain amplifier and a digital-to-analog converter. The measurement is performed with a CW single tone at a center frequency of 2.445 GHz. The fabricated PA achieves a P_{1dB} of 24.6 dBm with a peak DE of 38%, as shown in Fig. 5.6. In addition, the PA performance shows a close agreement between the simulated and measured results by achieving a small signal gain of 37 dB.

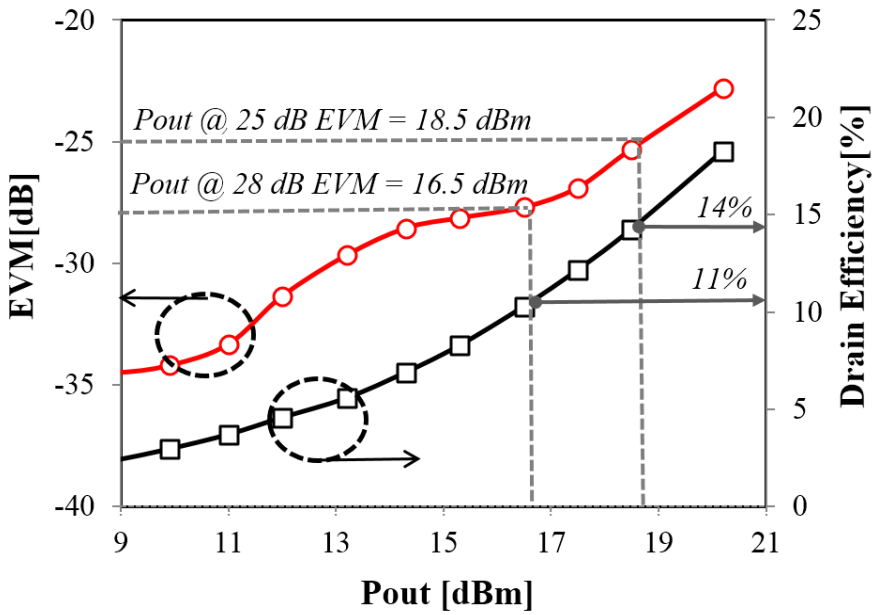


Fig. 5.7. Measurement results for EVM and drain efficiency performances with 64-QAM OFDM signal.

Finally, to verify the linear characteristic of the fabricated PA, the OFDM signal with a 20 MHz channel bandwidth of 802.11g WLAN was applied. Fig. 5.7 shows the measured error vector magnitude (EVM) and the DE characteristics according to the output power level. The maximum output power satisfying the 802.11g linearity specifications with the EVM of -25 dB was 18.5 dBm with the DE of 14%. The PA consumes the quiescent current of 101 mA (35 mA in the DA stage and 66 mA in the HPA) from the 3.3 V supply voltage. The performances of the designed PA are compared to other state-of-the-art linear CMOS PAs in Table 5.1. By using the proposed scheme in this work, the PA was achieved good efficiency in a small area.

5.3 Summary and Discussion

This chapter presents a two-stage highly efficient and linear CMOS power amplifier using a standard 40 nm CMOS process. The fabricated power amplifier

TABLE 5.1. Comparison of 2.4GHz OFDM CMOS PAs for commercialization (without DPD)

	Ref. [57]	Ref. [76]	This work
Small signal gain	33.5 dB	22 dB	37 dB
Peak PAE	37.6%	34.9%	38% (DE)
Pout at -25 dB EVM	24 dBm	24 dBm	18.5 dBm
PAE at -25 dB EVM	14%	14%	14% (DE)
Supply	3.3 V	3.3 V	3.3 V
Size	6 mm^2	6 mm^2	0.54 mm^2
Technology	65 nm CMOS	65 nm CMOS	40 nm CMOS

demonstrates suitable linearity, low current consumption, and enhanced average efficiency for 802.11g WLAN application. High performance results can be obtained from a destructive summation of nonlinear factors caused by the un-even biasing technique. In addition, the PA can be implemented in a small area since the un-even biasing strategy does not require any additional area. As a result, the PA can be integrated in a SoC chipset and can operate appropriately for use in communication systems.

CHAPTER 6

CONCLUSION AND FUTURE WORK

This chapter presents the conclusion of this thesis contribution and some future research directions in the area of CMOS RF power amplifier that could be developed based on the design and synthesis method presented in this thesis.

6.1 Conclusion

Many wireless communication standards such as wireless local area networks (WLAN), world-wide interoperability for microwaves (WiMax), wideband code division multiple access (WCDMA), long term evolution (LTE) etc, have been developed throughout the whole world and apparently more standards are to emerge in the near future. The integration of separate standards into one mobile unit or base-station increases the size, cost, and complexity of the wireless systems. Thus, the need for highly integrated system on chip (SoC) based on CMOS process is growing and many RF chip companies are trying to improve CMOS power amplifier performances such as output power, efficiency, and linearity. However, the design techniques of CMOS RF PAs for wireless communications are not yet fully matured.

For the purpose of developing CMOS RF PAs for wireless mobile communications, this research shows both a novel design scheme for enhancements

of linearity and efficiency, and the successful implementation within fully integrated CMOS SoC chip.

In chapter 3, a highly efficient and linear CMOS power amplifier design scheme by combination of class A and class C biased amplifiers has been presented. The proposed amplifier enhanced the linear power and reduced quiescent and low power current consumption compared to conventional class AB amplifier. However, since class C biased amplifier has a large impedance variation according to input power level, the proposed amplifier had a limitation of amount of improvement.

In chapter 4, in order to obtain more efficiency enhancement, variable balun transformer (VBT) for load modulation of Doherty scheme was presented. In addition, the adaptive bias control technique was used for maximizing the efficiency at backed off power level. As a result, the designed PA achieved superior efficiency compared to previous works for WLAN PA. However, the amplifier was not only fully integrated.

In chapter 5, a fully integrated CMOS PA using 40 nm standard CMOS process was presented. To implement fully integrated SoC for WLAN application, the power amplifier block should be implemented in small area. So, unlike previous design, just one output balun was used and class A and class C biases were injected to separated gate nodes of transistor with different size. Thus, the designed PA was integrated on WLAN SoC chipset while achieving enhancements of linearity and efficiency, and the prototype was validated experimentally that it was applicable for WLAN system.

6.2 Future Research Direction

According to advancement of wireless communication system, in order to obtain higher data rate, RF power amplifier is required to operate more efficiently and more linearly for wider bandwidth signal. Although various techniques for highly efficient CMOS power amplifier design techniques was presented in this thesis, the linearity performance was not good enough. The proposed amplifiers are applicable for WLAN system, in which require weaker linearity relatively than other mobile communication systems, but it does not have enough linearity and output power for other mobile communication such as LTE, 802.11ac WLAN. Especially, although the proposed Doherty amplifier has the highest efficiency among designed amplifiers, the linearity of that has a limitation by discontinuous load modulation of VBT. Therefore, it should be noted that AM-PM behavior should be studied carefully as switching capacitors are turned on/off. For modulated signals with high peak-to-average ratio, the probability of signals with large envelope is very small, so does the probability to switch capacitors. Therefore, switched capacitor arrays work at low frequency. Nonetheless, quantization noise from switching actions needs to be carefully investigated. Ultimately, a natural extension of this work is to study for effective implementation method of dynamic load modulation in order to achieve higher linear output power and efficiency.

More in-depth study for CMOS PA is very necessary to perfectively applicable for modern or future wireless mobile communication systems.

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RESEARCH INTERESTS

I have worked on the linear and high efficiency RF transceiver design for mobile wireless communication system, mostly based on CMOS and HBT process. I have a rich experience in circuit and system design through simulation, layout, implement, and measurement. And now I would like to broaden my knowledge to millimeter wave integrated circuit design (MMIC) using GaN, PHEM process, especially to the development of next generation system such as 5G.

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PUBLICATION

INTERNATIONAL PEER-REVIEWED JOURNALS

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