Master Dissertation

Harmonic Suppression Microwave Amplifier using Defected Ground Structure

결합접지 구조를 이용한 고조파 차단 마이크로파 증폭기

2014. 08. 22

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Academic Advisor: Professor Yongchae Jeong

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Chonbuk National University

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Graduate School of
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To my beloved family

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ABSTRACT

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Power amplifier is one of the most critical and the challenging aspects in the wireless communications system, because it is a key building block in all RF transmitters. To achieve high output power of the amplifier, it is necessary to design with optimum impedance. In this work, load-pull method has employed in this design in order to obtain optimum source and load impedance.

This dissertation presents *defected ground structure* or DGS technique can suppress unwanted signal caused by non-linear device. In this design structure with a single asymmetry spiral DGS could suppress the harmonic form 2^{nd} up to 5^{th} order harmonic. The proposed DGS power amplifier with the proposed topology experimentally achieved a maximum output power and power-added efficiency of 29.2dBm, 35% respectively in the operating center frequency 880MHz.

Keywords: Load-Pull, DGS, Harmonic, Power Amplifier.

ABSTRACT IN KOREAN

요약

RF 송신기의 주요 구성요소 중 하나인 전력 증폭기는 무선 통신 시스템의 성능을 좌우하는 가장 결정적이며, 어려운 도전 과제 중 하나이다. 높은 출력 전력을 갖는 증폭기를 설계하기 위해서는 최적의 임피던스 설계 방법이 필요하다. 본 논문에서는 최적의 소스 및 로드 임피던스를 얻기 위해 로드-풀 측정 방법이 사용되었다.

본 논문에서는 비선형 장치에 의해 발생되는 원치 않는 신호를 억제할 수 있는 결합 접지 구조(DGS) 기술을 제안하며, 설계된 구조에서는 하나의 비대칭 나선형 DGS 구조를 통해 2 차에서 5 차까지의 고조파 성분을 억제할 수 있었다. 제안된 DGS 구조가 적용된 전력 증폭기는 880 MHz 의 동작 주파수 내에서 29.2 dBm 의 최대 출력 전력 및 35 %의 전력 부가 효율을 얻을 수 있었다.

주요어 : 로드-풀, DGS, 고조파, 전력 증폭기

ABBREVIATIONS

ADS	advanced design system
DE	drain efficiency
DC	direct current
DGS	defected ground structure
GSM	global system for mobile communications
HFSS	high frequency structure simulation
MN	matching network
PA	power amplifier
PAE	power added efficiency
PCB	print circuit board
RF	radio frequency
TL	transmission line
TV	television

CHAPTER 1 INTRODUCTION

1.1 Literature Review

Power amplifiers are used in many different applications including the majority of wireless and radio communications equipment, wireless and cable TV broadcast systems, optical driver amplifiers, audio systems and radars. As Modern wireless communication systems demand increasingly more power conservation and channel capacity. Consequence, higher efficiency and linearity are expected from power amplifiers. Therefore, the requirements and the design target for a radio-frequency (RF) power amplifier (PA) include high efficiency, linearity, stability, broadband operational ability, and small size device are very important for many wireless communication systems.

Power amplifier is a non-linearity device and most of the designer face the problem with output of the power amplifier existed unwanted signal that caused power amplifier could not reached the maximum power. Therefore, several techniques have been applied in order to achieve high performance in power amplifier such as harmonic termination load network, filter, etc. In this thesis DGS is one of the solutions that can reduce unwanted signal and lead the power amplifier to the maximum output power.

1.2 Dissertation Objectives and Organization

The important goals in this designing amplifier are to increase its output power and efficiency by using *defected ground structure* or DGS technique. Also, the goal

in this dissertation was to compare the load-pull test system results with conventional power amplifier and DGS power amplifier to determine if device characteristics such as output power and efficiency were comparable.

The dissertation is organized as follows. Chapter 1 introduces you to power amplifier including some of its applications. Chapter 2 covers power amplifier classification and discussion with several kind of efficiency. Moreover, in this chapter define power capability and compression point. Chapter 3 introduces the DGS and advantage of using DGS. Chapter 4 describes the method to perform load-pull measurement and how to extracted source and load impedance. Also, in this chapter cover the design and implementation of the input and output matching network. Chapter 5 will present the proposed DGS output matching structure and the measurement result.

Finally, Chapter 6 summarizes the fundamental and design goal that contributions in the dissertation.

CHAPTER 2 POWER AMPLIFIER FUNDAMENTALS

2.1 Basic Power Amplifiers

RF and microwave power amplifiers are devices that amplify the input RF or microwave signals and deliver much higher power at the output. The power amplifier can also be considered a device that converts DC power provided from the supply into RF power at the output.

2.2 Gain

An amplifier's gain can be described as voltage gain, current gain, or power gain. The power amplifier is generally defined as its power gain. If magnitude of the output signal is shown as A_o, and input signal is shown as A_i, the gain will be their ratio as shown below.

$$G = \frac{A_o}{A_i} \tag{2.1}$$

2.3 Efficiency

For wireless transmitters in satellites and cellular telephone, where size, weight, durability and battery lifetime are demanded, power consumption is a very important factor when designing a power amplifier. In other words, a power amplifier must be highly efficient. When designing a power amplifier to be efficient, the available power from the transistor must be transferred to the load in an efficient manner. Without an efficient way to transfer power, the wasted power

will produce a considerable amount of energy in the form of heat. This causes increases in the junction temperature of the transistor that will lead to reduced performance and ultimately, transistor failure. Therefore, a high-efficiency power amplifier design will not only reduce the power consumed but also insure that the transistor does not overheat.

2.3.1 Overall Efficiency

Generally, there are two sources of input power into the amplifier. The RF signal drive power (P_{in}) and the DC power (P_{dc}) used to bias the transistor. The output powers include the reflected power by input mismatch (P_{ref}), the delivered RF power to the load (P_{out}) and the dissipated power (P_{diss}) in the form of heat. At low frequencies, the amplifier's overall efficiency (η_0) is commonly used since it is assumed that amplifiers produce high gain at lower frequencies.

$$\eta_{OVERALL} = \frac{P_{out}}{P_{dc} + P_{in}} = \frac{P_{out}}{P_{dc} + \frac{P_{out}}{G_P}} \tag{2.2}$$

Where

$$G_P = \frac{P_{out}}{P_{in}} \tag{2.3}$$

2.3.2 Power-Added Efficiency

However, in the RF, microwave and millimeter frequency range, the amplifier gain decreases. The typical definition used in higher frequency power amplifiers is Power-Added Efficiency (*PAE*) as shown in (2.4).

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \tag{2.4}$$

2.3.3 Drain Efficiency

Another useful definition that will help explain the different class of amplifiers in the next section is the output efficiency **(η_0)** or drain (collector) efficiency, which describes the ratio of output power to the DC power.

$$\eta_0 = \frac{P_{out}}{P_{dc}} \tag{2.5}$$

Where, P_{out} is the RF output power (dissipated into the load) and $P_{dc} = V_{dc} \times I_{dc}$ is the input power supplied by the dc supply to the drain circuit of the power amplifier. P_{out} usually includes both the RF fundamental power and the harmonics power. In many applications, harmonic suppression filters are included in the output-matching network. Because the harmonic power is negligible, the RF fundamental power is a very good approximation for P_{out}.

2.4 Power Output Capability

One of the most important characteristics of power amplifier is output power. The power output capability (C_p) provides a means of comparing different types of power amplifiers or amplifier designs. The power output capability is defined as the output produced when the device has a peak drain voltage of 1 volt and a peak drain current of 1 ampere. After the real voltage and current values of the drain are obtained, the multiplication of these values gives the maximum output power of the amplifier. If the power amplifier uses two or more transistor (as in push-pull designs, or in circuits with transistors connected in parallel, or using combiners), then the number of devices is included in the denominator (thus allowing a fair comparison of various types of amplifiers, either single-ended or using several transistors).

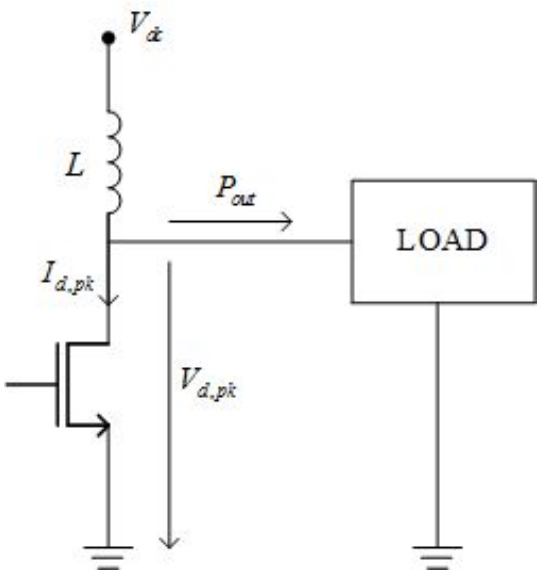


Fig. 2.1. Power output capability in RF power amplifiers.

If P_{out} is the RF output power, $I_{d,pk}$ is the peak drain current, $V_{d,pk}$ is the peak drain voltage, and N is the number of transistors in circuit, then the power output capability is given by (2.6).

$$C_p = \frac{P_{out}}{NI_{d,pk}V_{d,pk}} \tag{2.6}$$

Power transistors are the most expensive components in power amplifiers. In cost-driven designs, designers are constrained to use the lowest cost transistors. This means the devices have to be used as close as possible to their maximum voltage and current ratings. There, the larger the power output capability of the circuit, the cheaper its practical implementation.

2.5 Biasing and Power Amplifiers Classification

There are several types of power amplifiers and they differ from each other in terms of their linearity, efficiency and power output capability. The first step in designing a power amplifier is to understand the most important design factor and choose the power amplifier type most suited for that purpose. Depending on the linearity and efficiency requirements in the application, the operation classes of amplifier can be divided into two groups, the first covers high linear amplifiers such as Pas in mobile communication applications, and the second group belongs to high efficient amplifiers such as high Pas in satellite applications.

2.5.1 Class A Amplifier

In Class A amplifier, the drain current is needed to be at the half of the maximum drain current. So, the waveform of the current becomes sinusoidal and maximum possible conduction angle (2π) is obtained. This also means that the transistors in the output stage conduct for the full cycle of the input signal. Theoretically, maximum power efficiency in this class is 50% and Heat dissipation is high due to this 2π conduction angle. An example of a Class A output stage can be seen in Fig. 2.2.

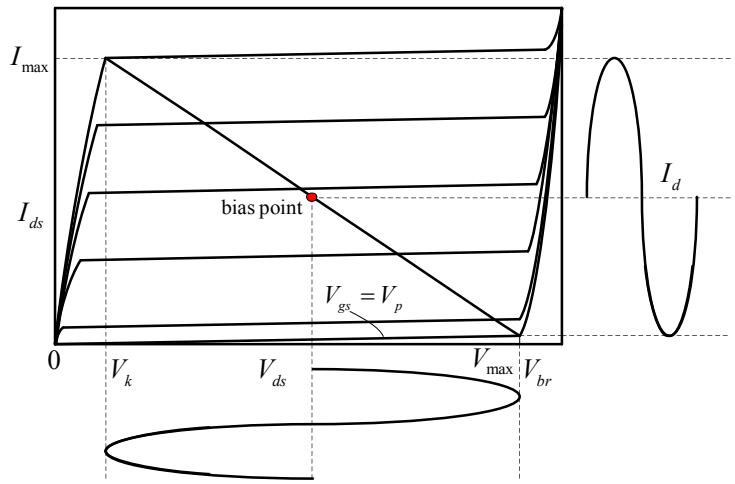


Fig. 2.2. Class A bias condition and output waveform.

2.5.2 Class B Amplifier

For class B operation, the quiescent point selected to keep the transistor in its active of 180 degree conduction angle, which the operating point of current is zero. The conduction angle is π in this class, which is the half of Class A. this also means

that the device is on during the half period of the input wave. Theoretically, maximum efficiency of Class B is 78%. An example of a Class B output stage can be seen in Fig. 2.3.

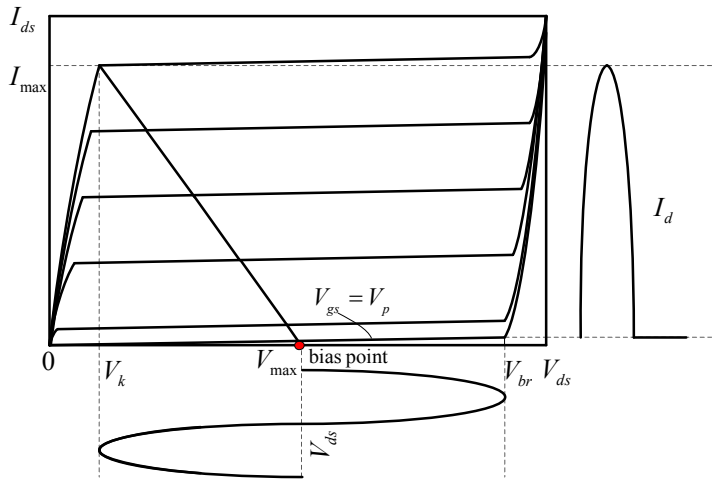


Fig. 2.3. Class B bias condition and output waveform.

2.5.3 Class AB Amplifier

The operating point of Class AB amplifier is chosen between the former classes. Conduction angle of this class is between π-2π, which mean that the Output stage is over 180 degree, but it is still less than 360 degree. The transistor is biased as close to pinch-off as possible. In this case, the transistor will be on for more than half a cycle, but less than a full cycle of the input signal. An example of a Class AB output stage can be seen in Fig. 2.4.

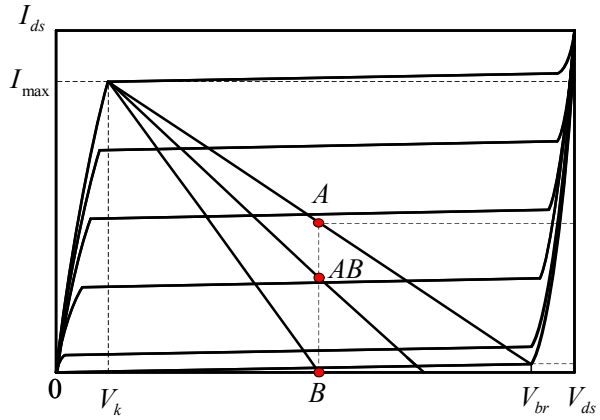


Fig. 2.4. Class AB bias condition.

2.6 1dB Compression

1dB compression point or can be called the maximum output power level is defined as the power level for which the input signal is amplified 1dB less than the linear gain. After this point, amplifier is in the nonlinear region. This means the 1dB compression point is a measure of the linear range of operation.

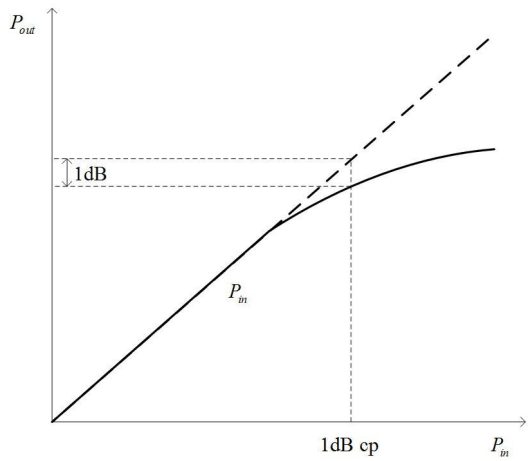


Fig. 2.5. 1dB-compression poin.

2.7 Impedance Matching Networks

To design amplifier, it is necessary to understand matching network in order to deliver maximum power to a load or to perform in a certain desired way. Fig. 2.6 illustrates a typical situation in which a transistor, in order to deliver maximum power to the 50Ω load, must have the terminations Z_S and Z_L. The input matching network is designed to transform the generator impedance (show as 50Ω) to the source impedance Z_S, and the output matching network transforms the 50Ω termination to the load impedance Z_L. There are many different type of matching networks can be describe in [2].

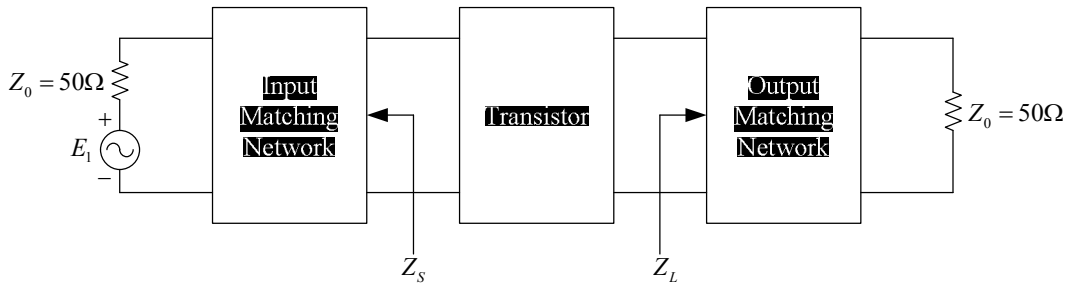


Fig. 2.6. Block diagram of a amplifier.

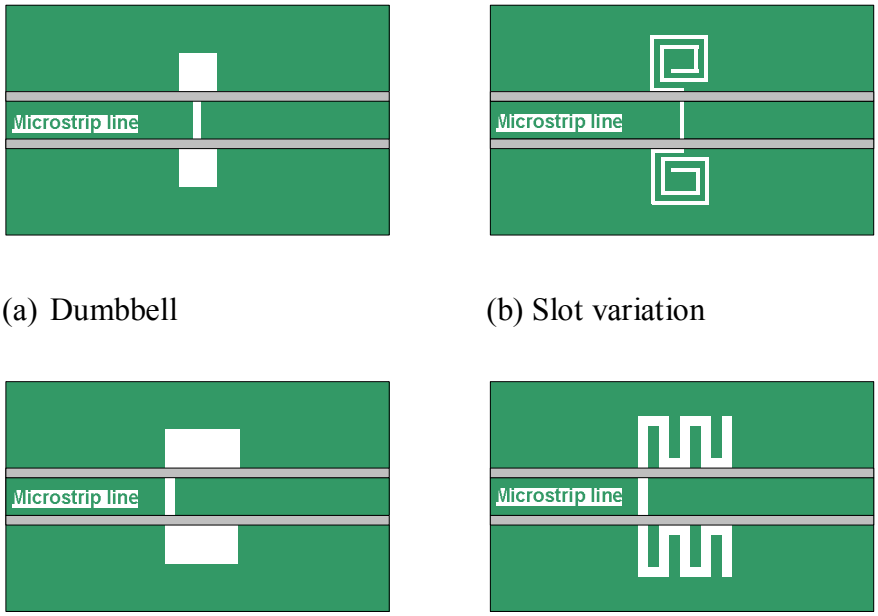
CHAPTER 3 DEFECTED GROUND STRUCTURE

3.1 DGS Basic

The most important design targets of power amplifiers are high output power, efficiency, and excellent linearity. In order to obtain good performance, there are several techniques are employed such as filter, harmonic termination load network, harmonic injection, pre-distortion power amplifier, etc. One of the methods to improve the performances is to tune the harmonics at the output. Therefore, a technique *defected ground structure* or DGS is proposed, where the ground plane metal of a microstip circuit is intentionally modified to enhance performance. The purpose of using DGS is to improve the performance of power amplifier by suppressing and tuning harmonic.

DGS is an etched periodic or non-periodic cascaded configuration defect in ground of a planar transmission line (e.g., microstrip, coplanar and conductor backed coplanar wave guide) which disturbs the shield current distribution in the ground plane cause of the defect in the ground. This disturbance will change characteristics of a transmission line such as line capacitance and inductance. Any defect etched in the ground plane of the microstrip can give rise to increasing effective capacitance and inductance, which raising the phase constant and slow-wave effects. Therefore, DGS produces band rejection in certain frequency band.

Fig. 3.1 shows the various kinds of defected ground structures (DGS), realized by etching a defected pattern on the ground plans.



(a) Dumbbell (b) Slot variation

(c) Spiral (d) Meander lines

Fig. 3.1. Four kinds of defected ground structure.

3.2 DGS Power Amplifier

There are three steps to design DGS amplifier in this dissertation. First, load-pull method is employed to achieve optimum source and load impedance. Second, designed input and output matching network. Third, DGS is applied to the output matching circuit in the ground of a planar transmission line. Using DGS to suppress the harmonic is not complex and needs no additional transmission line, just apply the DGS unit to the ground plane metal in the circuit. The detail of design DGS power amplifier will describe in next chapter.

CHAPTER 4 POWER AMPLIFIER DESIGN

4.1 Load-Pull Method

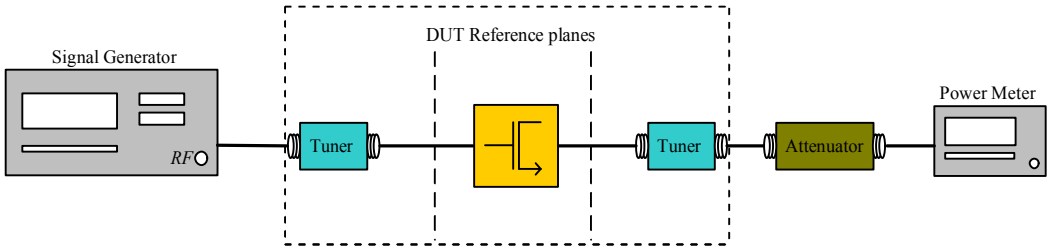
Load-pull consists of changing the load impedance seen by the DUT and measuring the device operation simultaneously. This technique is called load-pull because the load impedance is varied or "pulled" using a load tuner. Similarly, the source impedance can also be varied using a source tuner when making measurements of the device performance. This is called source-pull. Load-pull and source-pull are often used to characterize microwave and RF power devices**.**

According to maximum power transfer rule, the load impedance has to be equal to the conjugate to the output impedance for delivering maximum power. The optimum source and load impedances have to be found in order to obtain the maximum output power. Therefore a procedure call load-pull method is used.

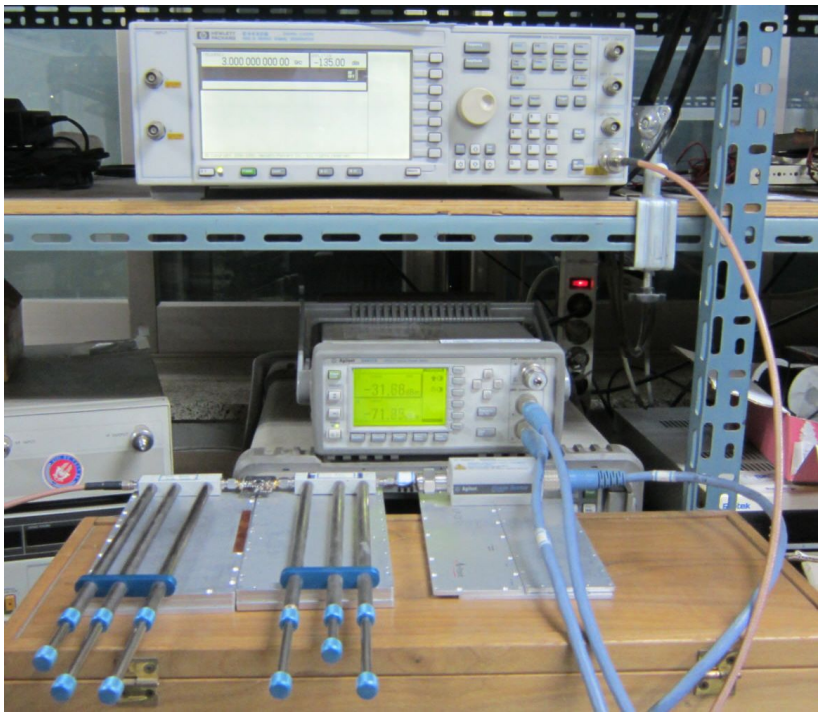
In the load-pull measurement, the TQP7M9103 InGaP/GaAs HBT was measured under a single supply voltage of 5V and I_q of 235mA at the operating center frequency 880MHz. The performance of the device is tracked through varying source and load impedance. In this work, impedance values are varied by the manual tuners as shown in Fig. 4.1. The tuners then fit the measured performance parameters on a gamma source or gamma load plane. Appropriate impedances for source and load are then have been extracted so that the matching networks can be designed.

Fig. 4.1. Manual tuner.

Load-pull measurement setup in this work is intended to measure the optimum source and load impedance, so that the input and output matching networks for gain and power stages can be designed. Detailed illustration of the load-pull setup and the actual setup can be seen in Fig. 4.2(a) and Fig. 4.2(b), respectively. The schematic of a load-pull setup in Fig. 4.2(a) consists of a Signal generator in order to provide CW signal, impedance tuners, device under test (DUT), 10dB attenuator, and power meter. Fortunately, signal generator could provide enough input power into the DUT, so we do not need any additional pre-amplifier.



(a)



(b)

Fig. 4.2. (a) Load-pull block diagram and (b) load-pull measurement setup.

4.2 Load-Pull Method Result

Maximum output power obtained by using manual tuner, this mean that the optimum source and load impedance was achieved. Then we extracted the impedances from the source and load tuner at the device reference plane as shown in Fig. 4.3. The optimum source and load impedances that were thus obtained are tabulated and shown in table 4.1. The optimum source and load impedance circles are also shown in Fig. 4.4.

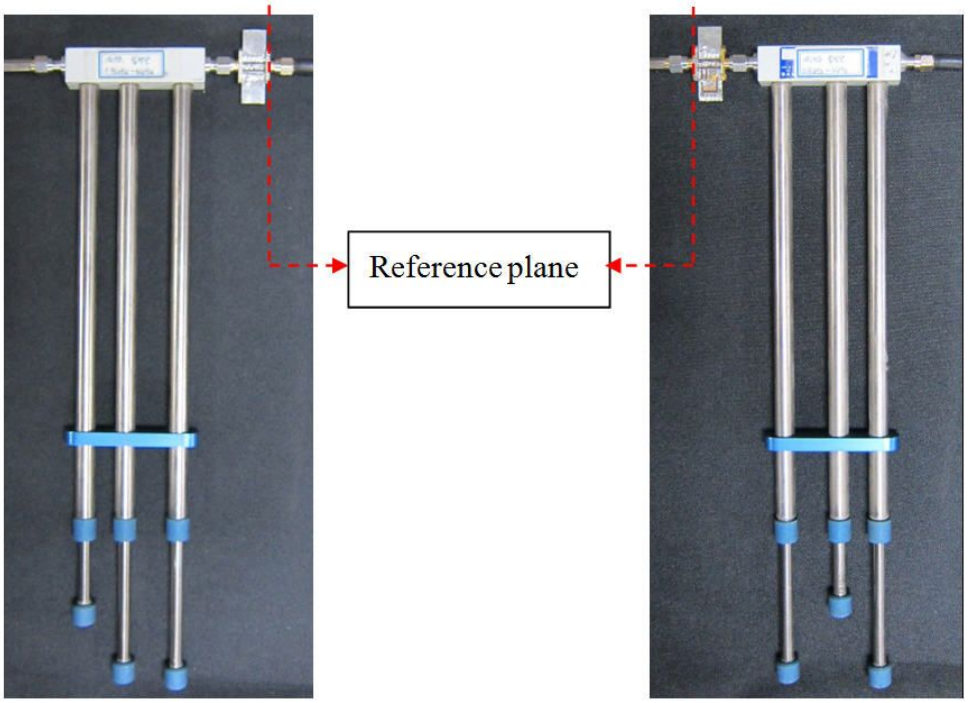
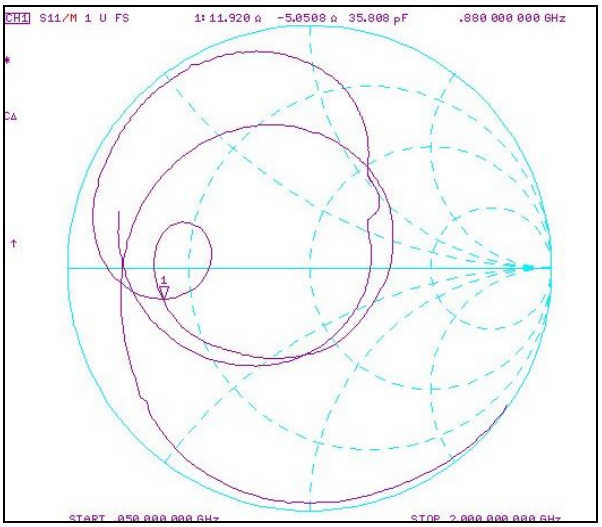


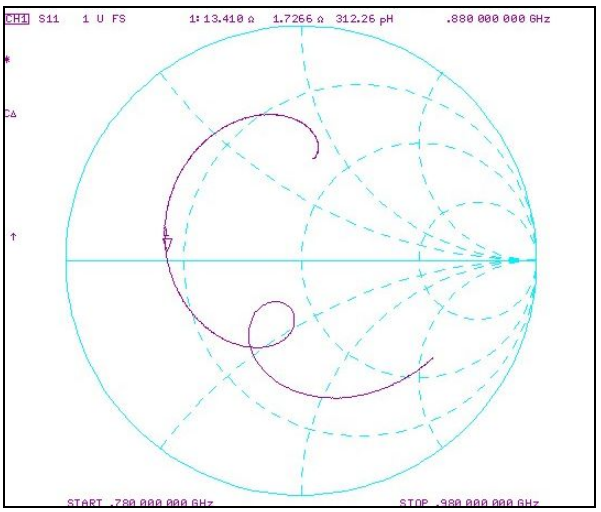
Fig. 4.3. Extracted source and load impedance from tuner.

Table 4.1: Optimum load and source impedance of DUT.

Frequency (MHz)	Source Impedance (Ω)		Load Impedance (Ω)	
	Real	Imaginary	Real	Imaginary
880	11.9	-5	13.4	1.72



(a)



(b)

Fig. 4.4. (a) Optimum source impedances for DUT and (b) optimum load impedances for DUT.

In the load pull measurement had provided maximum output power about 27.3dbm with efficiency (PAE) 34.5%. Result of the load-pull measured shown in the Fig. 4.5.

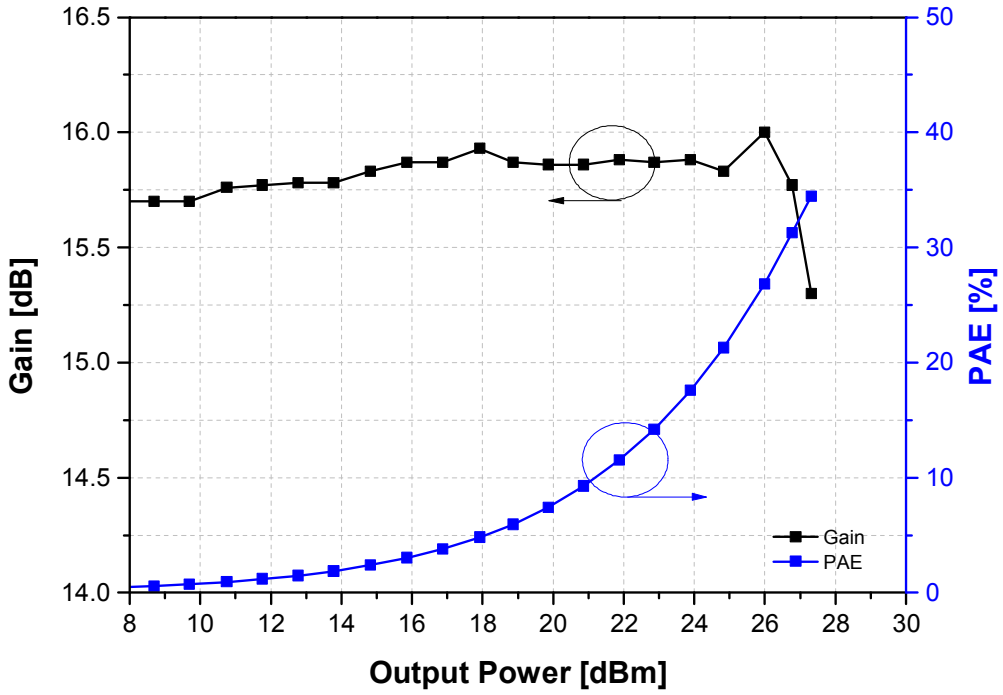


Fig. 4.5. Result of the load pull measurement.

Not that the maximum output power achieved in this measured are including the SMA connector, source and load tuner losses. Therefore, maximum output power will increase when measurement with fabricate PCB.

4.3 Matching Network

Matching networks provide transformation from Z_{source} and Z_{load} to standard 50Ω terminations. These Z_{source} and Z_{load} values are required in order to provide desired max power, gain or PAE. Therefore it is important to find these optimum values through source-load pull measurements. These values are then used to design the input and output matching networks with distributed components.

4.3.1 Bias Line

In general, small signal amplifier at UHF uses a chip inductor as the RF chock for bias. The ideal inductors would have zero resistance and zero capacitance. However, the real lumped inductors have the parasitic resistance and capacitance. With those parasitic, the inductor can make a self-resonant frequency (SRF), and it looks like capacitor (negative inductance) at above SRF. So the quarter wavelength ($\lambda/4$) transmission lines, terminated with chip capacitor or radial stubs, are preferred as bias lines in microwave frequencies. Fig. 4.6 shows the conventional $\lambda/4$ bias line. In this figure, the bypass capacitor will short in view of frequency and then $\lambda/4$ transmission line transforms short impedance to the open at point A.

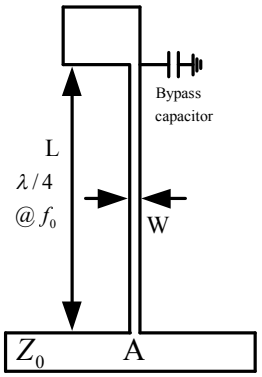


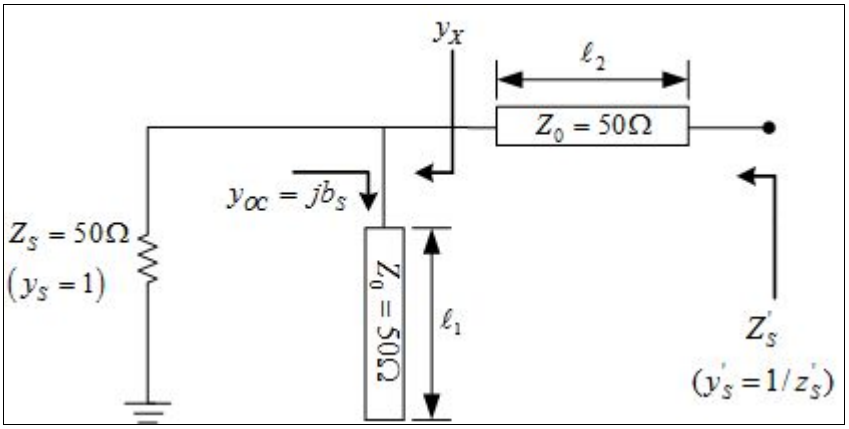
Fig. 4.6. $\lambda/4$ bias line.

To minimize the interference between bias and signal transmission lines, the difference between their characteristic impedances should be as large as possible. Therefore, $\lambda/4$ transmission lines with very high impedance are generally used.

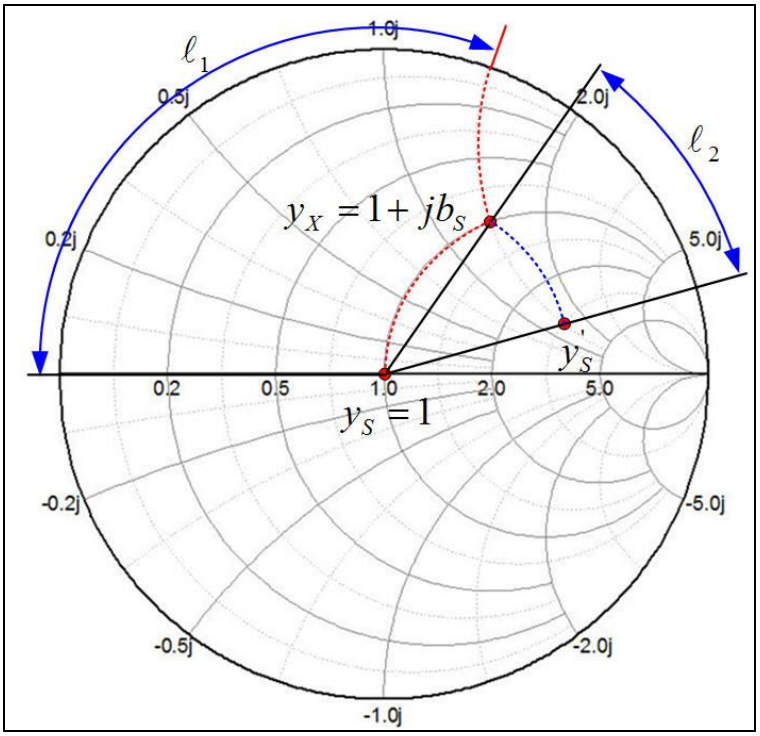
4.3.2 Input Matching Network

The matching circuit configuration in which an open-circuited stub is connected in parallel with the 50Ω (Z_s) followed by a series microstrip transmission line is show in the Fig. 4.7(a). The characteristic impedance of the microstrip lines is shown as 50Ω. In this design procedure, it is convenient to use the Y smith chart to design the circuit. Fig. 4.7(a) shows the matching circuit where $z_S = Z_S / Z_0 = 50/50 = 1$ (or $y_S = 1/z_S = 1$). The normalized admittance of the open stub is written, for convenience, in the form $y_{OC} = jb_S$. The length ℓ_1 determines the value of jb_S. The admittance y_X is given by equation:

$$y_X = y_S + y_{OC} = 1 + jb_S \tag{4.1}$$



(a)

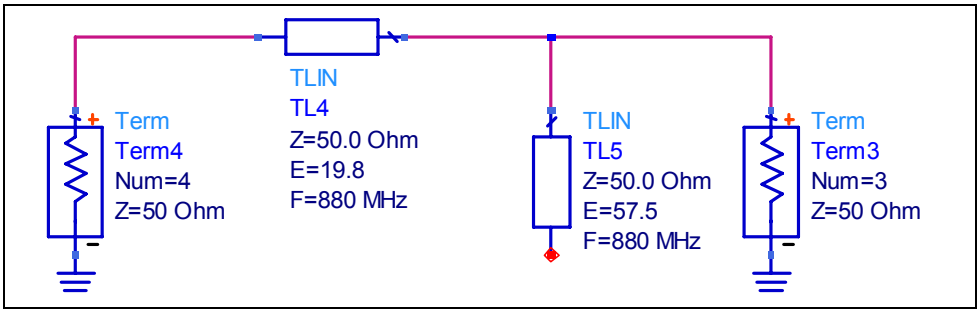


(b)

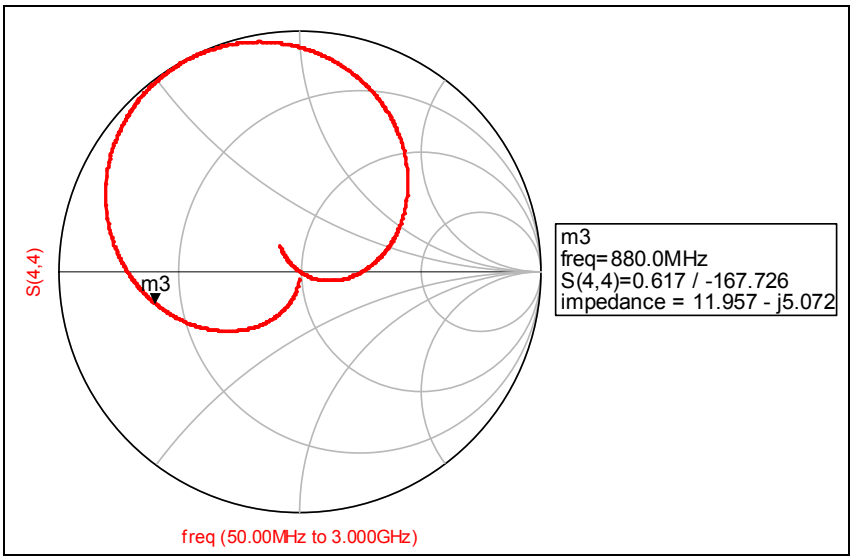
Fig. 4.7. (a) A microstrip network to transform $y_S = 1$ to y_S' and (b) the design in the Y Smith chart with $y_{OC} = jb_S$.

As shown in the Y Smith charts in Fig. 4.7(b), the addition of $y_{OC} = jb_S$ to y_S produces a motion along the unity constant-conductance circle from $y_S = 1$ to $y_X = 1 + jb_S$. Finally, the design of the series transmission line of length ℓ_2 is such that y_X is transformed to the admittance y_S' (a typical y_S' is shown in Fig. 4.7(b)). The length of 50Ω characteristic impedance open stub transmission line ℓ_1 and serial transmission line ℓ_2 obtained from Smith chart are 57.5 and 19.8 degree, respectively with input impedance looking into matching circuit $z_S' = 11.9 - j5$ $(y_S' = 1/z_S' = 3.57 + j1.5)\ \Omega$.

The input matching circuit was designed and simulated with ADS and HFSS simulation. Fig. 4.8(a) shows input matching simulated with ideal element in ADS simulation and Fig. 4.8(b) shows the source impedance circle simulated with ideal element.



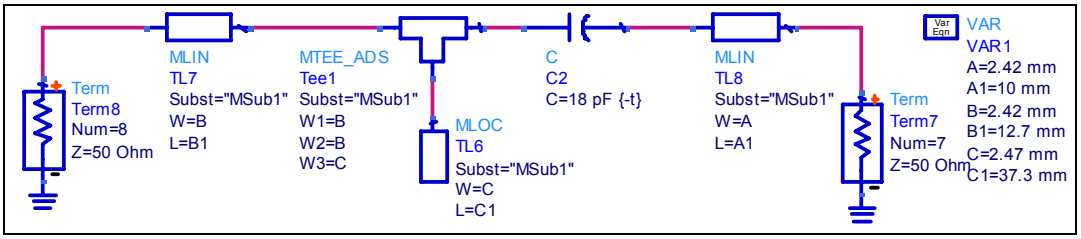
(a)



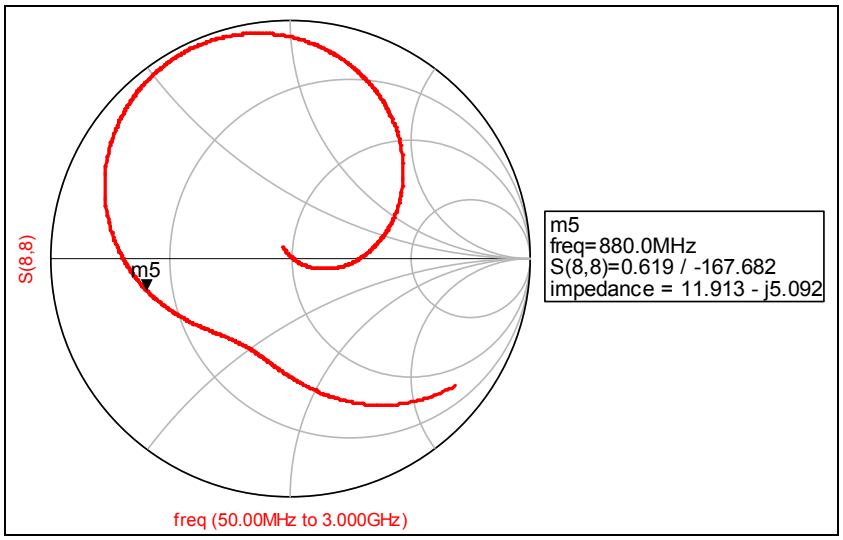
(b)

Fig. 4.8. (a) ADS simulation setup showing input matching network with ideal element and (b) source impedance circle with ideal element.

Fig. 4.9(a) shows the ADS simulation setup input matching circuit with non-ideal element. In this simulation, a T-connection inserted between a serial transmission line and an open-circuit shunt stub transmission line. Moreover, a DC block capacitor serial with 50Ω short length transmission line added to the T-connection as shown in Fig. 4.9(a). The source impedance circle also shown in Fig. 4.9(b).



(a)



(b)

Fig. 4.9. (a) ADS simulation setup showing input matching network with non-ideal element and (b) source impedance circle with non-ideal element.

Fig. 4.10 shows the layout of input matching circuit and simulation in HFSS. The source impedance extracted from tuner, ADS and HFSS are tabulate in table 4.2. The extracted from tuner, ADS and HFSS source impedance circles are also shown in Fig. 4.11.

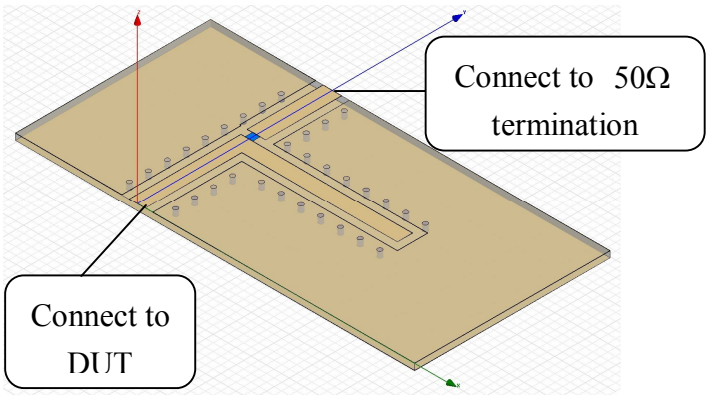


Fig. 4.10. Layout of input matching network.

Table 4.2: Source impedances extracted from tuner, ADS, and HFSS simulation

Frequency @ 880MHz	Source Impedance (Ω)	
	Real	Imaginary
Tuner	11.9	-5
ADS	11.95	-5.05
HFSS	12	-5.2

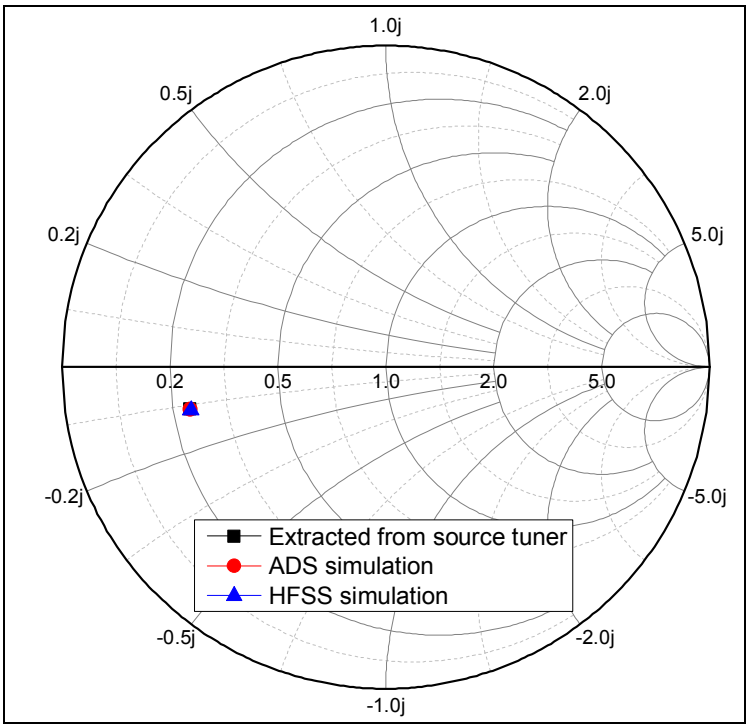


Fig. 4.11. Source impedance extracted from tuner, ADS and HFSS.

To validate the proposed structure of input matching circuit operating center frequency (f_o) of 880MHz is fabricated on the substrate with a dielectric constant

($_r$) of 2.2 and thickness (h) of 31 mils as shown in the Fig. 4.12. Fig. 4.13 shows the measured impedance circle of the proposed input matching circuit. As seen in the figure, the measurement result is in good agreement to the simulation results at the operating frequency. The source impedance extracted from tuner, ADS, HFSS, and measurement are tabulate in table 4.3.

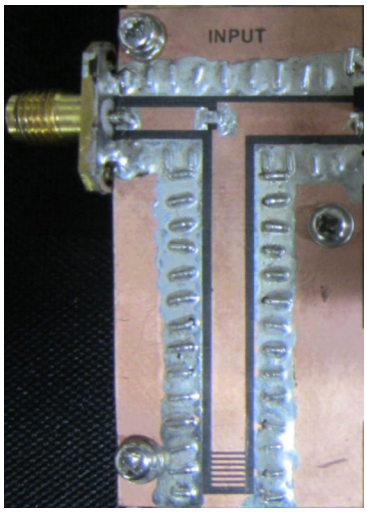


Fig. 4.12. Photograph of the fabricated input matching circuit for 880MHz.

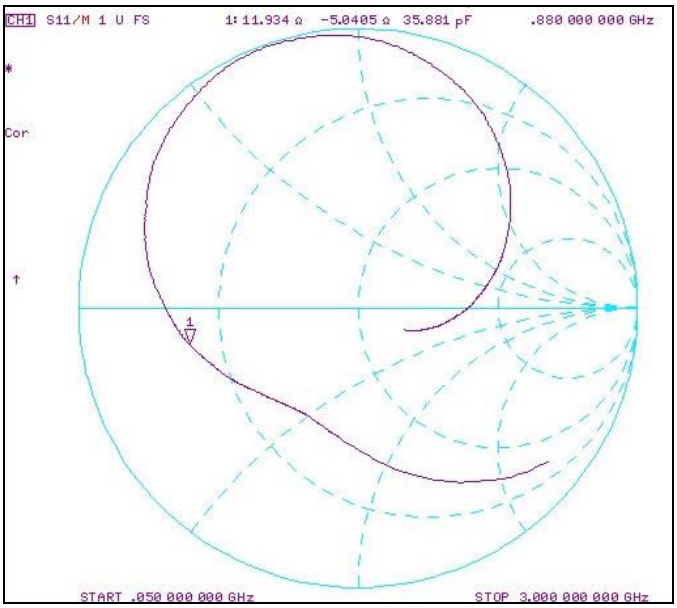


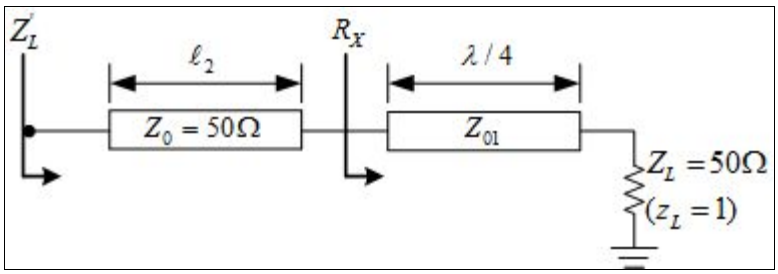
Fig. 4.13. Source impedance circle.

Table 4.3: Source impedances extracted from tuner, ADS, HFSS, and Measurement

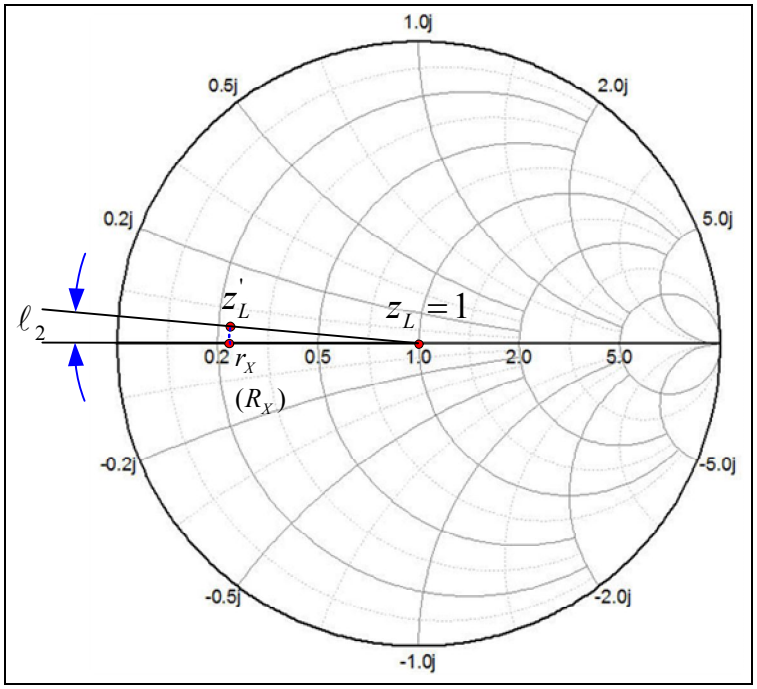
Frequency @ 880MHz	Source Impedance (Ω)	
	Real	Imaginary
Tuner	11.9	-5
ADS	11.95	-5.05
HFSS	12	-5.2
Meas	11.9	-5

4.3.3 Output Matching Network

A microstrip matching network which can be easily designed using a Z Smith chart is shown in Fig. 4.14. This matching network uses a $\lambda/4$ line with characteristic impedance Z_{01} to transform the 50Ω load ($z_L = 1$) to resistance R_X ($r_X = R_X/50$) that lies on the constant $|\Gamma|$ circle that passes through $z_L = Z_L/50$. The value of characteristic impedance Z_{01} is given by $Z_{01} = \sqrt{50R_X}$. Then, the 50Ω transmission line with length ℓ_2 changes the normalized resistance r_X to the input impedance z_L' .



(a)



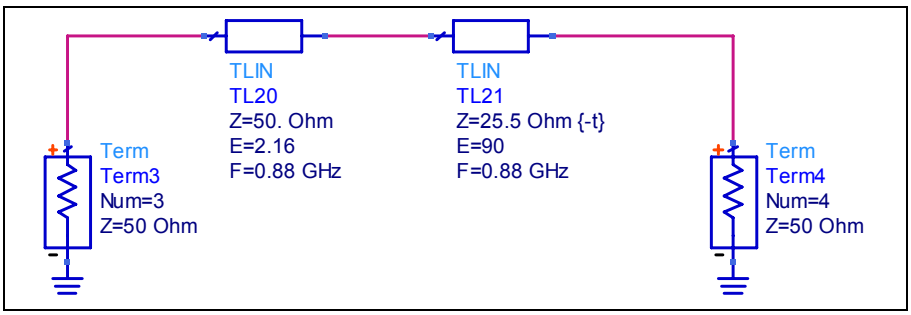
(a)

Fig. 4.14. (a) Microstrip matching circuit and (b) design in the Z Smith chart that results in Z_{01} smaller than 50Ω.

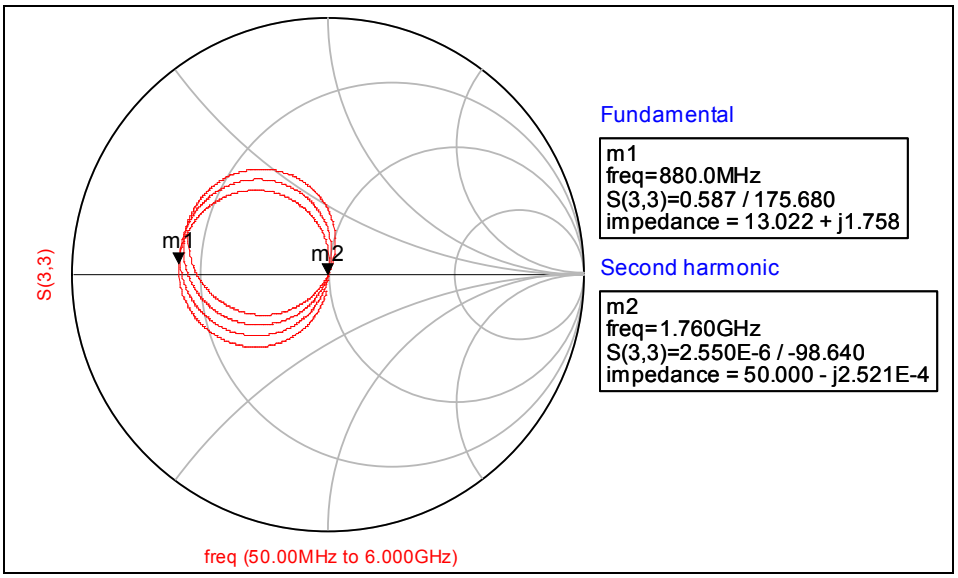
Equation (4.2) show the characteristic impedance of the $\lambda/4$ transmission line Z_{01} and characteristic impedance $Z_0 = 50\Omega$ with length $\ell_2 = 0.006\lambda = 2.16$ degrees read from smith chart. Input impedance looking into output matching circuit is $Z_L' = 13 + j1.7$.

$$Z_{01} = \sqrt{50R_X} = \sqrt{50*13} = 25.5\Omega \tag{4.2}$$

The output matching circuit was designed and simulated with ADS and HFSS simulation. Fig. 4.15(a) shows output matching simulated with ideal element in ADS simulation. Fig. 4.15(b) shows the load impedance circle.



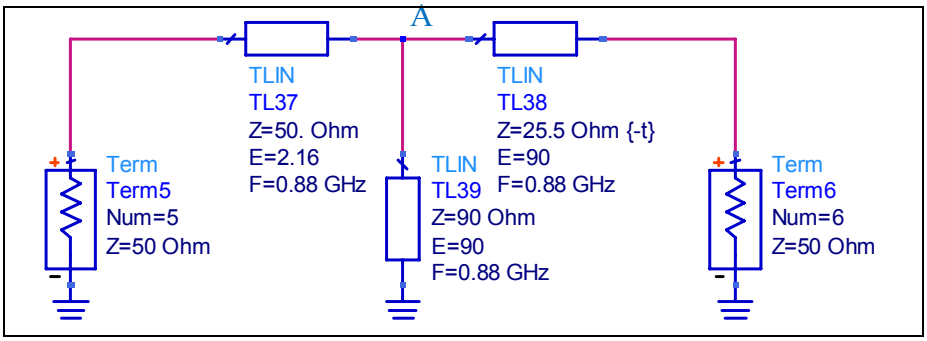
(a)



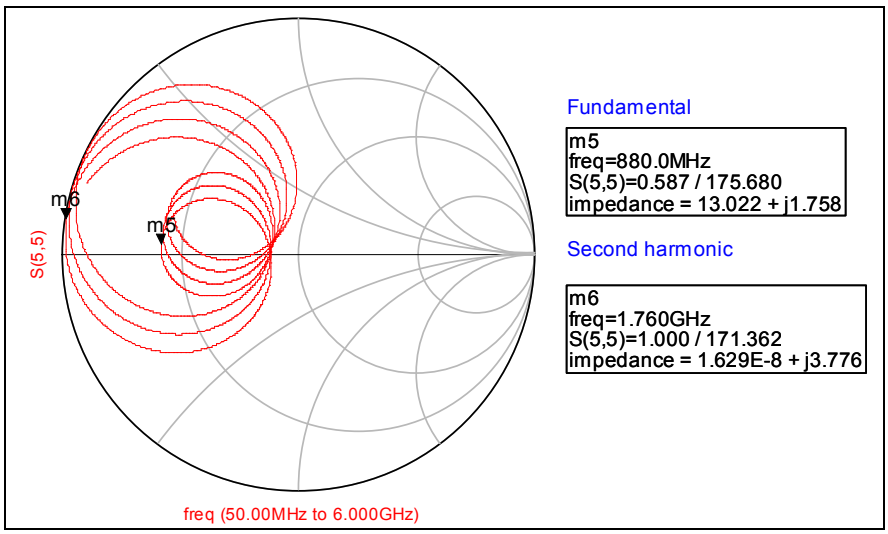
(b)

Fig. 4.15. (a) ADS simulation setup showing output matching schematic with ideal element and (b) source impedance circle.

Fig. 4.16 (a) shows the output matching network inserted $\lambda/4$ high impedance transmission line. This $\lambda/4$ transmission line preferred as bias line and open at the fundamental, but short at second harmonic in the view of frequency. Fig. 4.16 (b) shows the load impedance circle with second harmonic located at very low impedance of the smith chart with fundamental impedance is maintained.



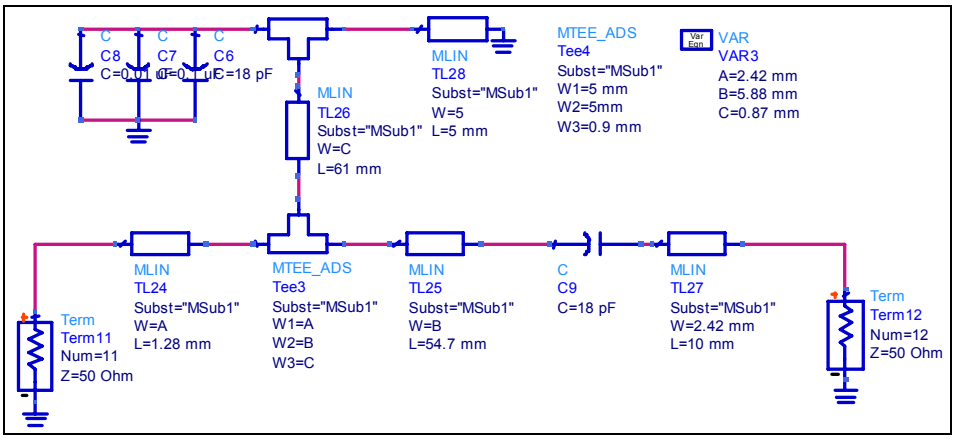
(a)



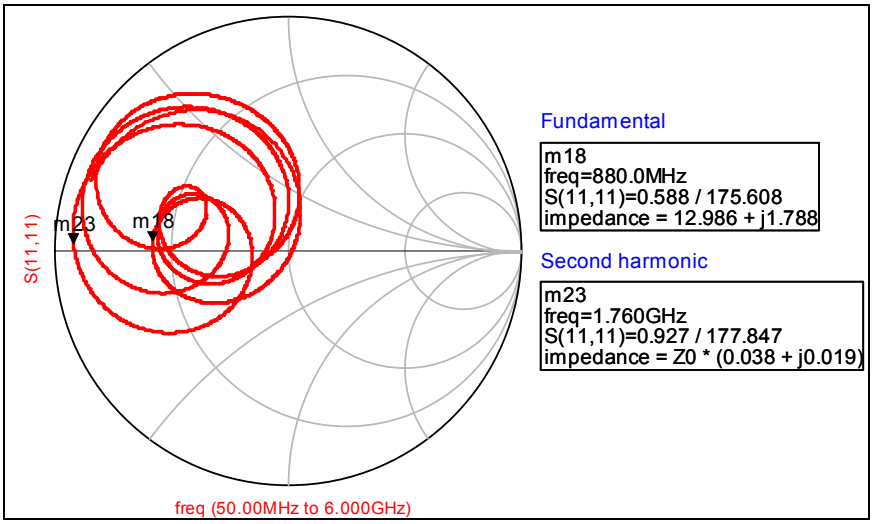
(b)

Fig. 4.16. (a) ADS simulation setup showing output matching schematic is inserted $\lambda/4$ bias line and (b) load impedance circle.

Fig. 4.17 (a) shows the ADS simulation setup output matching circuit with non-ideal element. T-connection inserted between triangles at point A as shown in Fig. 4.16 (a). DC block capacitor serial with 50Ω short length transmission line added to the $\lambda/4$ transmission line which transform $Z_L = 50\Omega$ to resistance R_X. Moreover, island and three capacitors are added to the bias line. The three capacitors are used to eliminate the noise and to short the bias feed end due to $\lambda/4$ line transform the short into open at the operating frequency 880MHz. Load impedance circle also shown in Fig. 4.17 (b).



(a)



(b)

Fig. 4.17. (a) ADS simulation setup showing output matching schematic with non-ideal element and (b) load impedance circle.

Fig. 4.18 shows the layout of output matching circuit and simulation in HFSS. The load impedance extracted from tuner, ADS and HFSS are tabulate in table 4.4. The extracted from tuner, ADS and HFSS load impedance circles are also shown in Fig. 4.19.

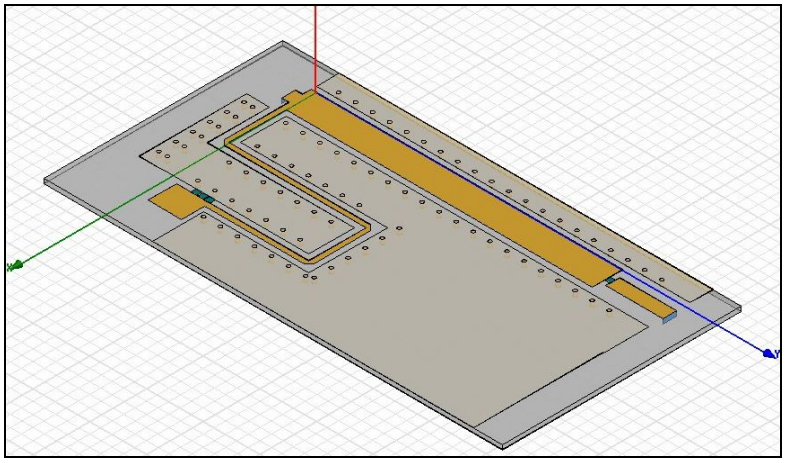


Fig. 4.18. Layout of output matching network.

Table 4.4: Load impedances extracted from tuner, ADS and HFSS simulation

Frequency @ 880MHz	Load Impedance (Ω)	
	Real	Imaginary
Tuner	13.4	1.72
ADS	12.9	1.78
HFSS	13.3	1.52

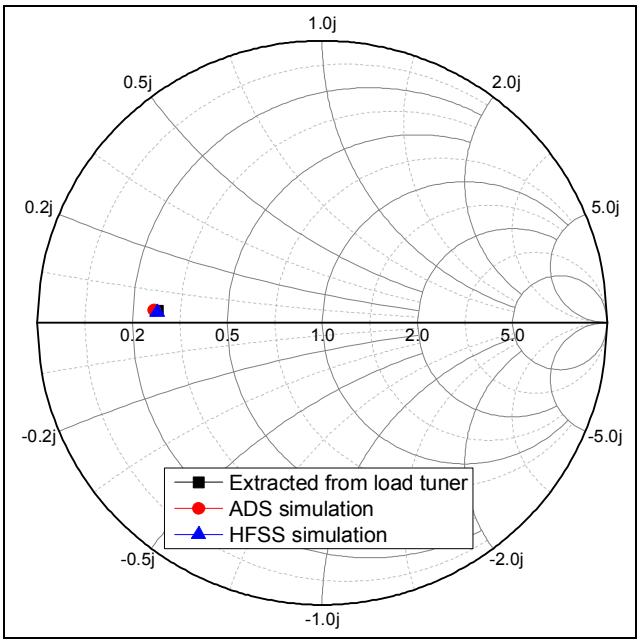


Fig. 4.19. Load impedance of tuner, ADS, and HFSS circle.

To validate the proposed structure of output matching circuit operating center frequency (f_0) of 880MHz is fabricated on the substrate with a dielectric constant (ε_r) of 2.2 and thickness (h) of 31 mils as shown in the Fig. 4.20. Fig. 4.21 shows the measurement impedance circle of the proposed input matching circuit. As seen in the Fig. 4.21, the measurement result is in good agreement to the simulation

results at the operating frequency. The load impedance extracted from tuner, ADS, HFSS, and measurement are tabulate in table 4.5.

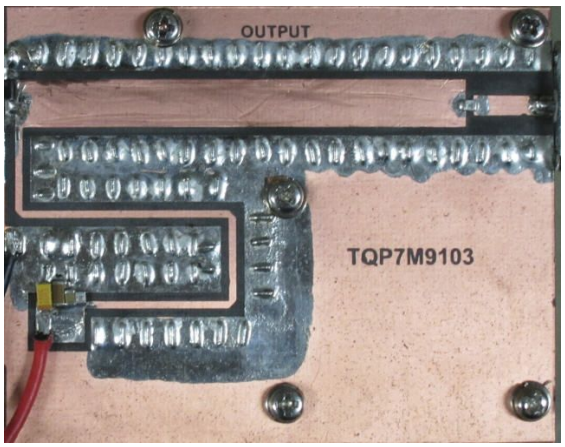


Fig. 4.20. Photograph of the fabricated output matching circuit for 880MHz.

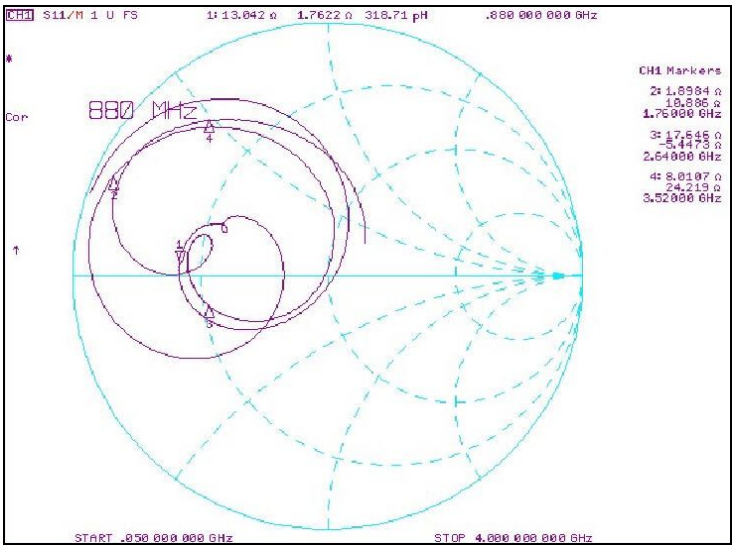


Fig. 4.21. Load impedance circle of measured result.

Table 4.5: Load impedances extracted from tuner, ADS, HFSS, and Measurement

Frequency @ 880MHz	Load Impedance (Ω)	
	Real	Imaginary
Tuner	13.4	1.72
ADS	12.9	1.78
HFSS	13.3	1.52
Meas	13	1.76

CHAPTER 5 IMPLEMENTATION AND MEASUREMENT RESULT

5.1 Conventional Power Amplifier

The power amplifier is implemented as shown in the Fig. 5.1. Measurement of P1dB, PAE and gain will be illustrated in this section. Power amplifier bias conditions are supply voltage of 5V and current of 240mA. According to the result shown in the Fig. 5.2, the measured gain, maximum output power and Power-Added Efficiency at P1dB are 16.45dB, 28.92dBm, 33.6% respectively.

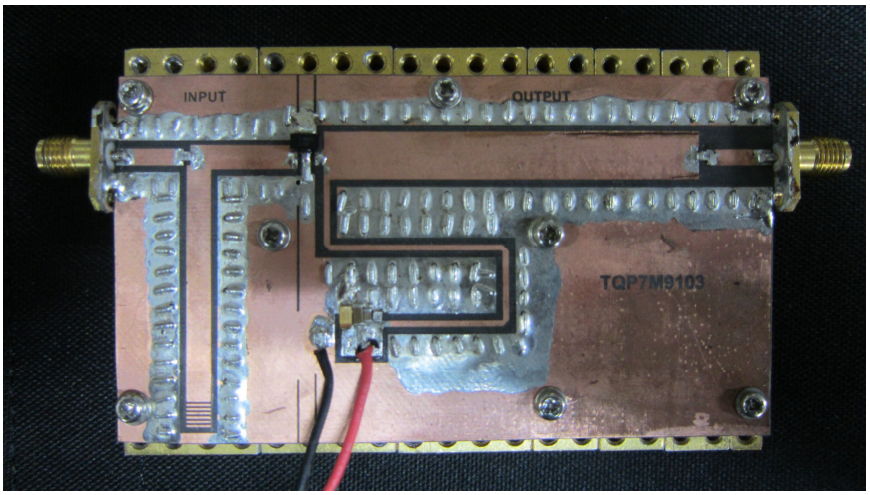


Fig. 5.1. Photograph of fabricated power amplifier.

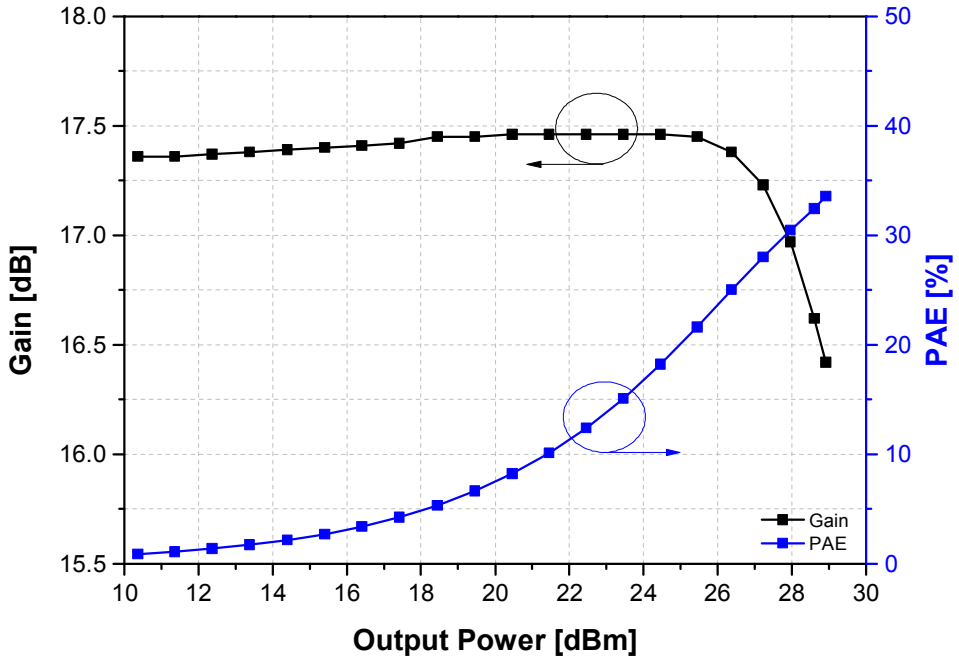


Fig. 5.2. Conventional PA measurement result.

Fig. 5.3 shows the comparison of the result between conventional amplifiers with load-pull measured. As shown in Fig. 5.3, maximum output power of the conventional amplifier is improved about 1.6dBm. P1dB, PAE, and gain of conventional PA and load-pull measured result are tabulated in table 5.1.

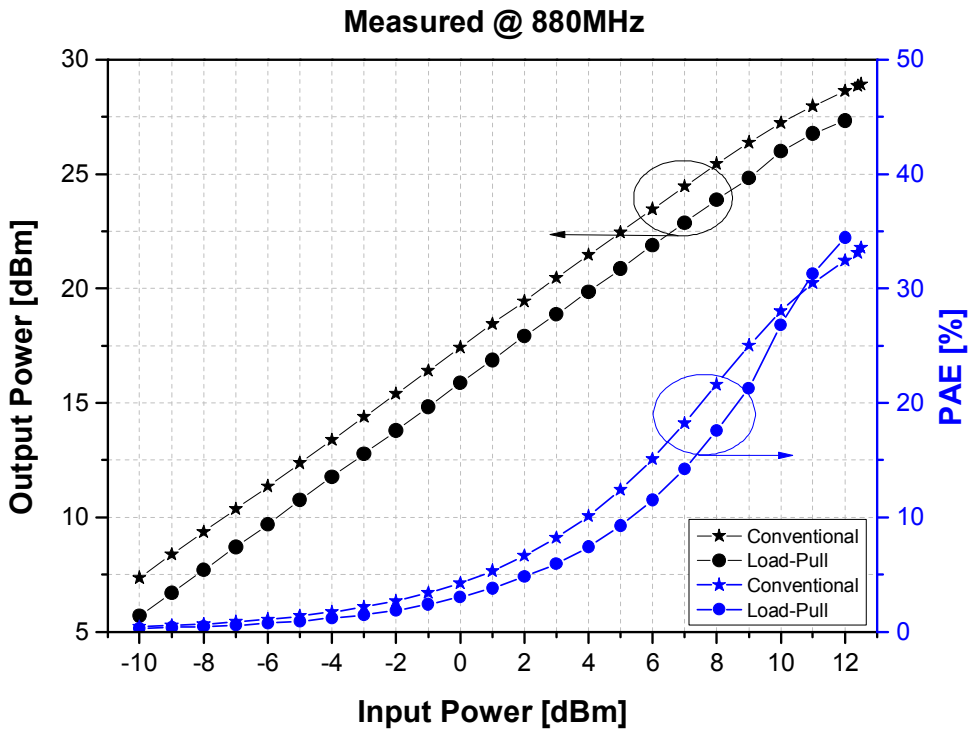


Fig. 5.3. Compare the result between conventional PA with load-pull measurement result.

Table 5.1: Conventional PA and load-pull method measurement result

Frequency @ 880MHz	Pout [dBm]	Gain [dB]	PAE [%]
Load-Pull	27.32	15	34
Conventional	28.92	16.45	33.6

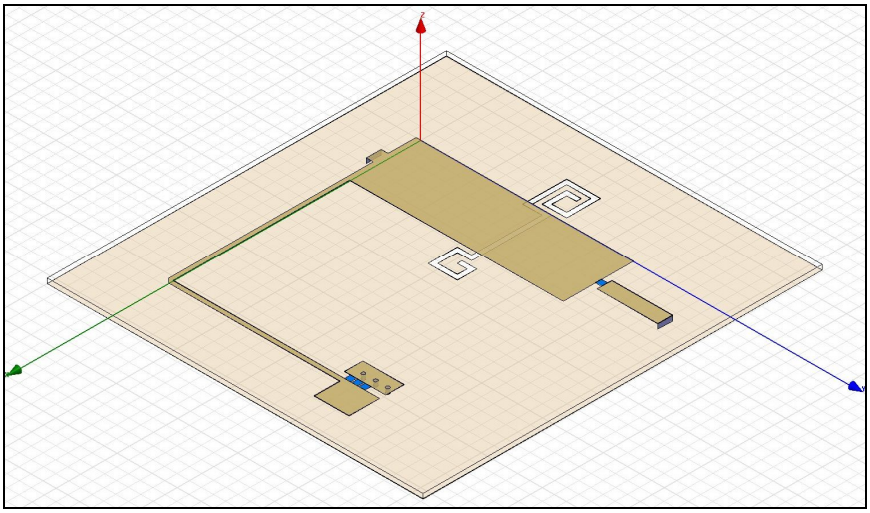
5.2 DGS Power Amplifier

An ideal harmonic termination condition should be satisfied in performing conventional power amplifier analysis, so the fundamental current is taken into consideration only. Previous studies assumed a weakly nonlinear case, therefore higher order harmonics were not considered.

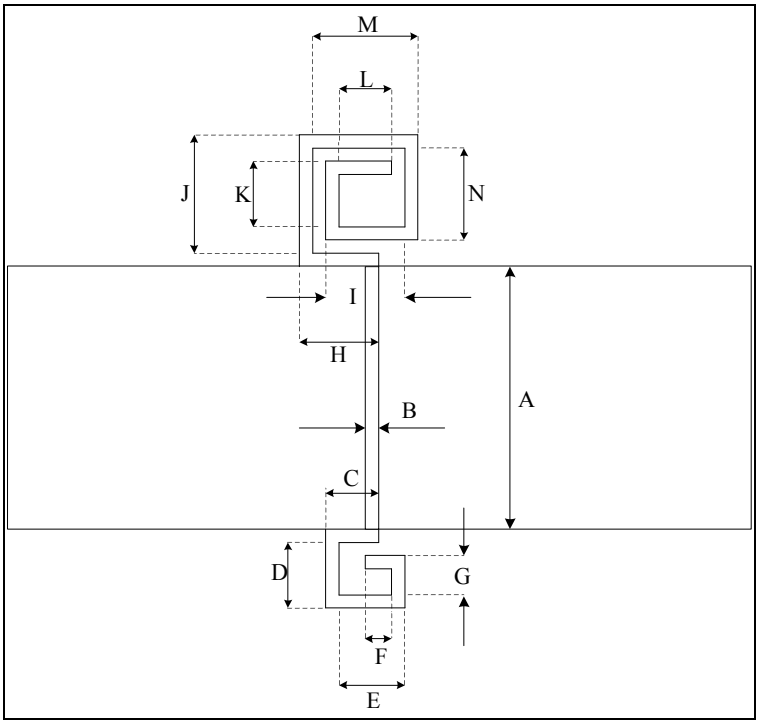
In this work, we propose a new design method for defected ground structure (DGS) power amplifier having ideal harmonic termination. Using DGS is not only maximize the output power and efficiency, also reduced the size of amplifier.

5.2.1 DGS Output Matching

We designed output matching with DGS line using an asymmetry spiral shaped DGS to obtain higher order harmonic termination condition. The DGS line has to maintain low insertion loss and a good reflection characteristic at the fundamental frequency as it should be placed at the output of the power amplifier (PA). Fig. 5.4 (a) shows the layout of DGS output matching in HFSS simulation. It is noted that no additional transmission line to apply DGS patterns has been inserted. We did just apply DGS unit on the ground pattern. Fig. 5.4 (b) shows the geometry of the proposed DGS line of which implemented on the substrate with $\varepsilon_r = 2.2$ and $h = 31$ mil. Width and length of the DGS line are tabulated in the table 5.2. Fig. 5.5 shows the simulation impedance circle of the proposed DGS output matching.



(a)



(b)

Fig. 5.4. (a) DGS output matching layout and (b) geometry of the DGS line.

Table 5.2: DGS output matching geometry.

Parameters	Physical length	Unit
A	11.6	mm
B	0.8	mm
C	3.2	mm
D	4	mm
E	4	mm
F	1.6	mm
G	2.4	mm
H	4	mm
I	3.2	mm
J	6.4	mm
K	3.2	mm
L	1.6	mm
M	4.8	mm
N	4.8	mm

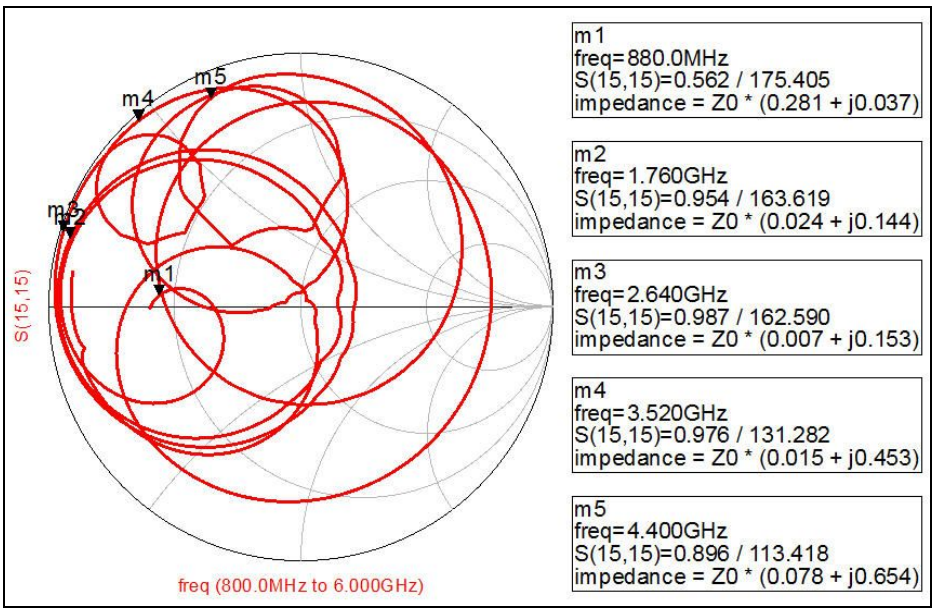
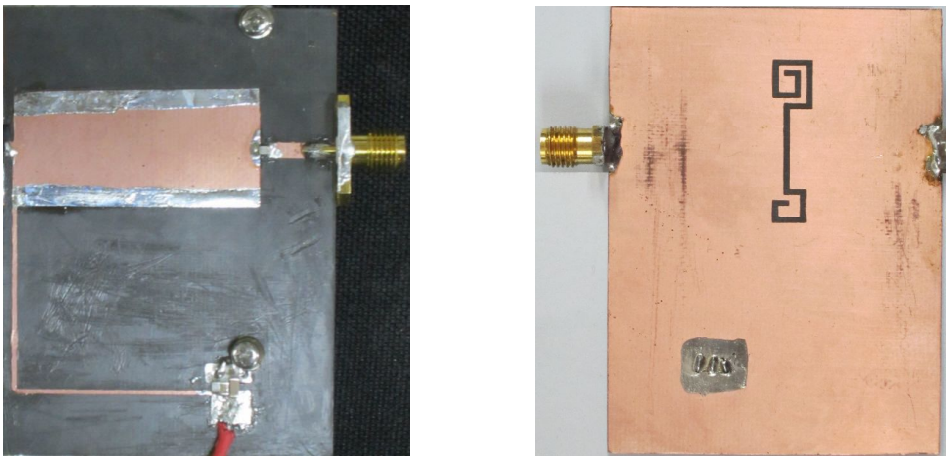


Fig. 5.5. HFSS simulated load impedance circle of proposed DGS output matching.

To validate this proposed structure, DGS output matching is fabricated as shown in the Fig. 5.6(a) and Fig. 5.6(b). Fig. 5.7 shows the measured impedance circle of the proposed DGS output matching circuit. As seen in the figure, second and third harmonic are located at the short impedance point in the smith chart. Fourth and fifth harmonic are located at low real part impedance of the Smith Chart.



(a) (b)

Fig. 5.6. Load impedance circle of proposed DGS output matching (a) top view and (b) bottom view.

Fig. 5.8 shows the comparison of the load impedance circle measured result between conventional and DGS output matching. As seen in the Fig. 5.8, harmonics of the conventional matching network are not located at the short impedance point. Second harmonic impedance only located at the short impedance point in the Smith Chart.

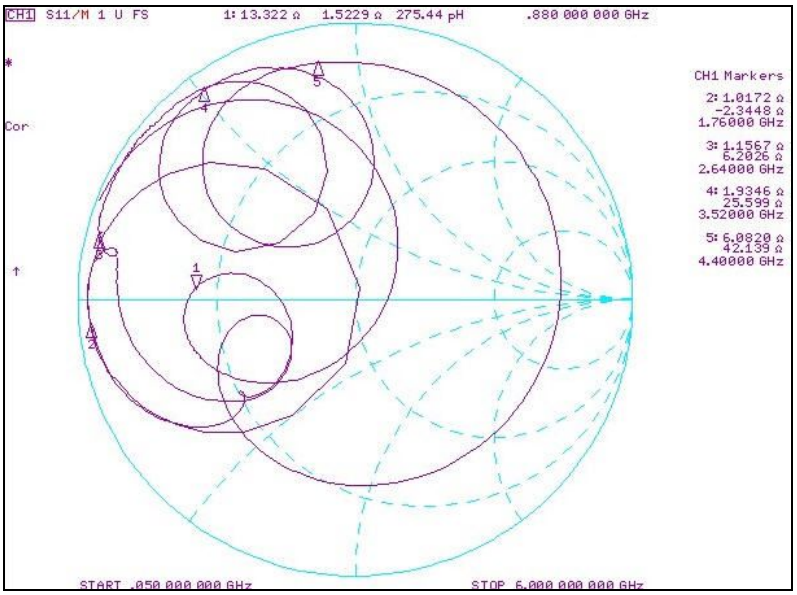


Fig. 5.7. Load impedance circle measurement result of proposed DGS output matching network.

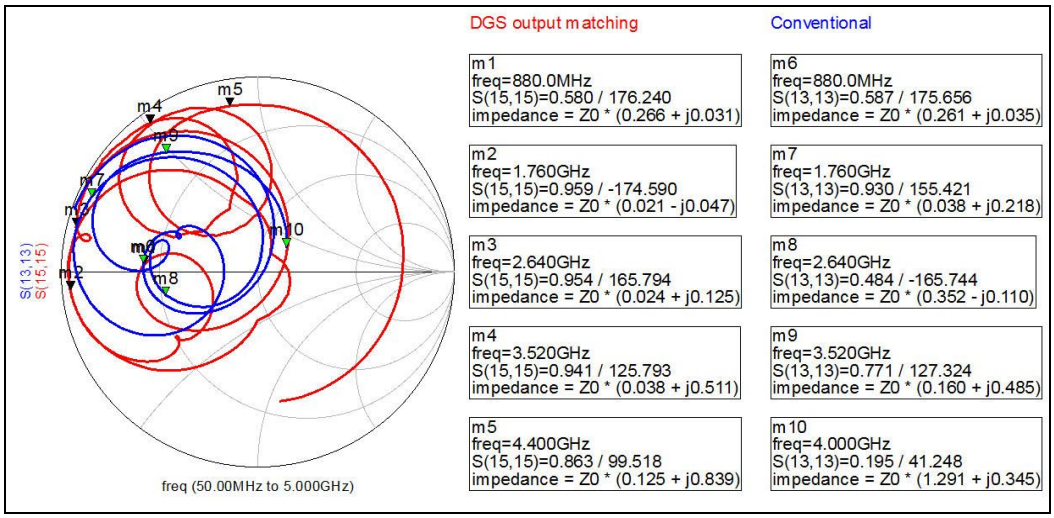


Fig. 5.8. Load impedance circle of the Measurement result between conventional and proposed DGS output matching network.

5.2.2 DGS Power Amplifier Implementation

DGS power amplifier implemented as shown in the Fig. 5.9. Measured P1dB, PAE and gain are shown in Fig. 5.10 where bias conditions are same to conventional amplifier. According to the result, the measured gain and maximum output power at P1dB are 16.8dB, 29.2dBm, respectively. Power Add Efficiency (PAE) of 35% reached at maximum output power.

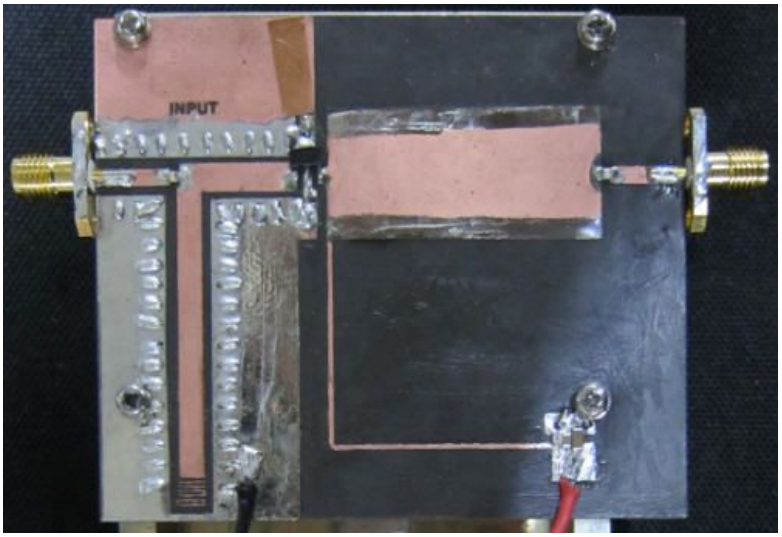


Fig. 5.9. Photograph of fabricated DGS power amplifier.

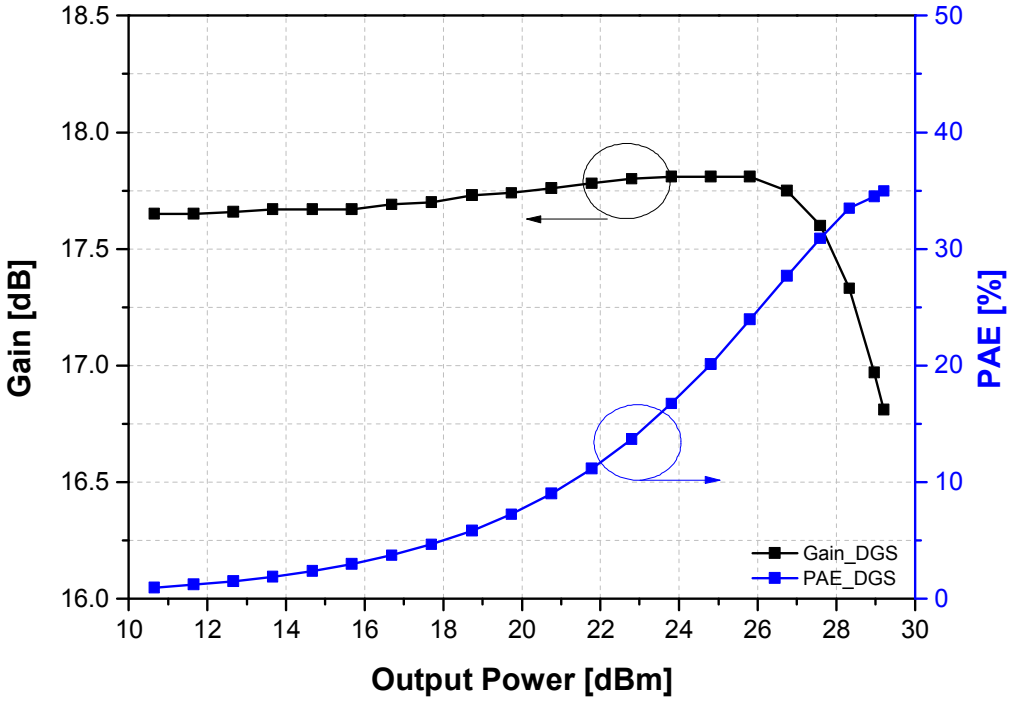


Fig. 5.10. DGS power amplifier measurement result.

This section also shows the comparison of the measured maximum output power and Power-Added Efficiency (PAE) at P1dB between conventional amplifiers with DGS power amplifier as shown in the Fig. 5.11. As seen in Fig. 5.11, Power-Add Efficiency (PAE) of 35% reached at maximum output power, where the conventional amplifier could obtained 33.6%. According to the result in Fig. 5.11, maximum output power and Power-Added Efficiency (PAE) are improved 0.3dBm and 1.4%, respectively. The result of the conventional and DGS power amplifier are tabulated in the table 5.3.

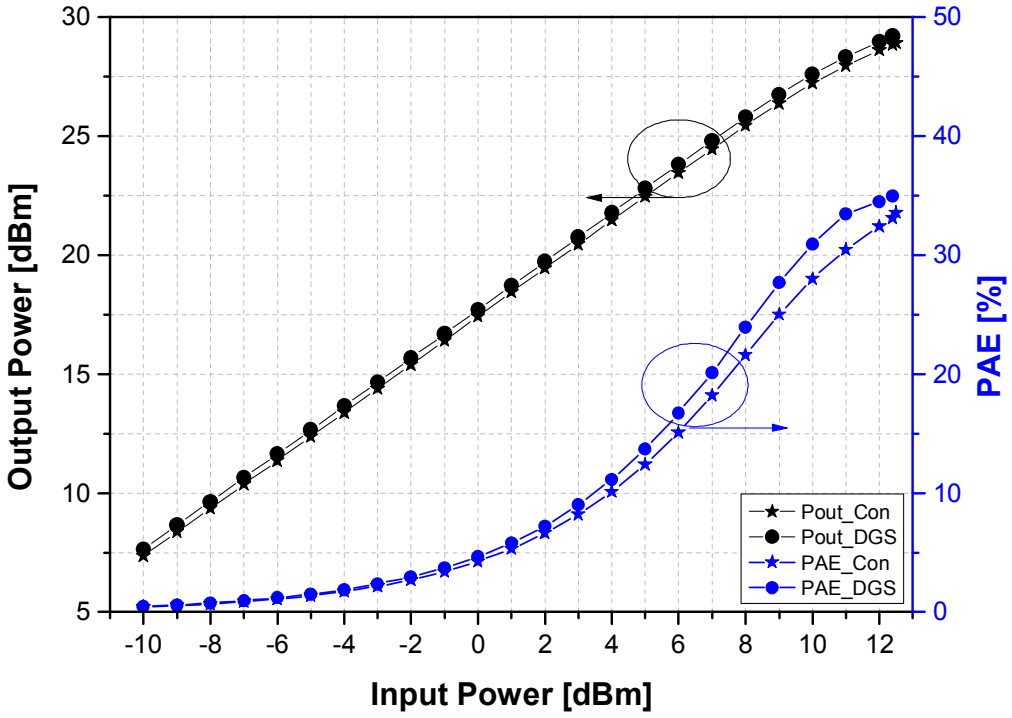
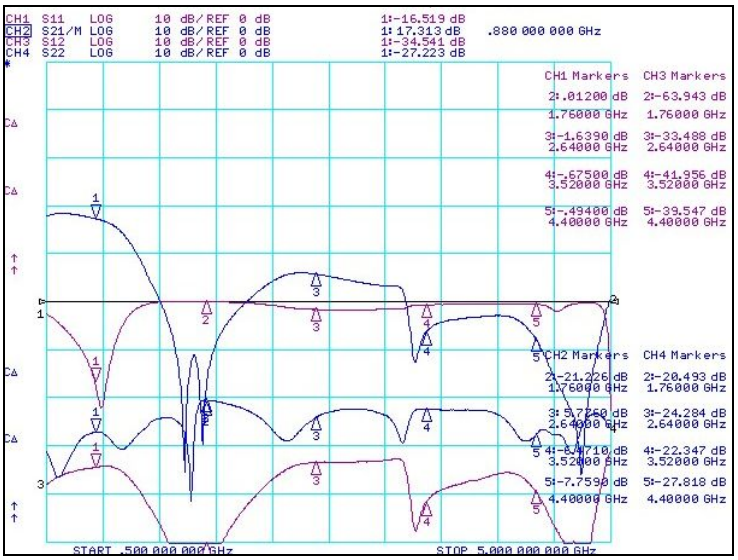


Fig. 5.11. Compare the measurement result between conventional and DGS power amplifier.

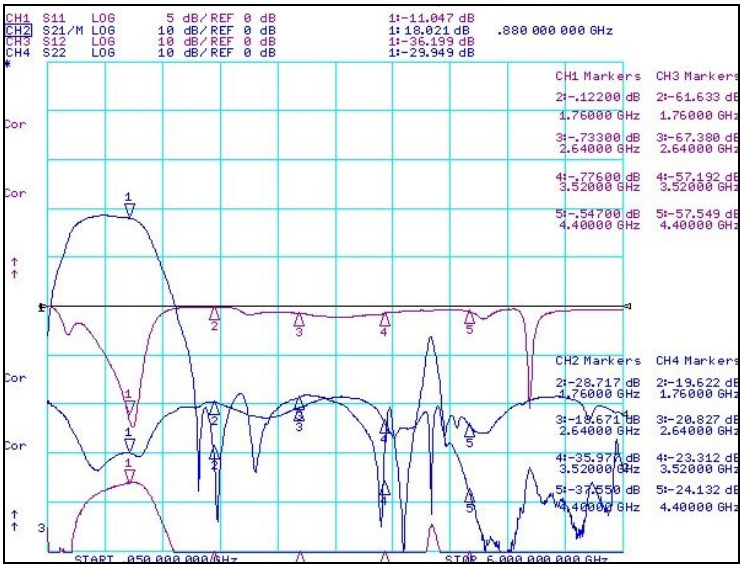
Table 5.3: Conventional and DGS PA result.

Frequency @ 880MHz	Pout [dBm]	PAE [%]
Conventional PA	**28.9**	**33.6**
DGS PA	**29.2**	**35**
Improvement	**0.3**	**1.4**

Fig. 5.12 shows the harmonics characteristics of the power amplifier with and without DGS. According to the results has shown in the Fig. 5.12, second, third, forth, and fifth harmonic of the DGS power amplifier are suppressed better than 18dB.



(a)



(b)

Fig. 5.12. Harmonics characteristics of the power amplifier with (a) conventional power amplifier and (b) DGS power amplifier.

CHAPTER 6 CONCLUSION

Load-pull measurement has been performed in order to obtain source and load impedance. The primary goal of this thesis is to improve the maximum output power by employed DGS (Defected Ground Structure) in to the output matching of the power amplifier. We could suppress higher order harmonics and reduce the circuit size effectively by the negligible insertion loss, excellent harmonic termination characteristic. As a result of harmonic termination, considerable improvements in maximum output power, gain, and efficiency have been achieved.

It is expected that the proposed design technique is well applicable to the conventional power amplifier to improve P1dB without any additional lumped elements or transmission lines, while the total circuit size is reduced at the same time.

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