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A Design of the Multiplier for Fundamental Signal and over the 3rd Harmonic Components Suppression

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Abstract

In this paper, we designed and implemented the multiplier that multiply 2.14GHz to 4.28GHz . The designed multiplier uses the feedforward technique for fundamental signal suppression and DGS transmission line for over the 3rd order harmonic suppression. For -10dBm input level, the implemented multiplier shows suppression characteristics of 50dB at fundamental, 34dB at the 3rd harmonic, and more than 20dB at the 4th harmonic frequency.

. FET
 pinch - off
 Single - ended
 $\lambda/4$
 single - ended
 open - stubs balun
 Monolithic transceivers
 2.14GHz 2
 ERA - 4SM , Feed -
 forward , 4
 DGS(Defected Ground Structure)
 3 , 4 [1] - [6].

2.14GHz, -10dBm
 Feedforward DGS
 3

DGS
 DGS
 (slow - wave) 가
 DGS 2
 3
 2 Feedforward DGS
 3 DGS

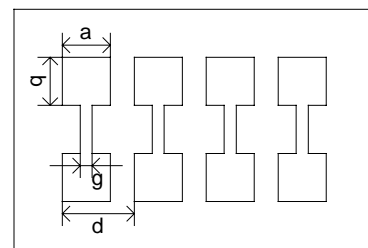
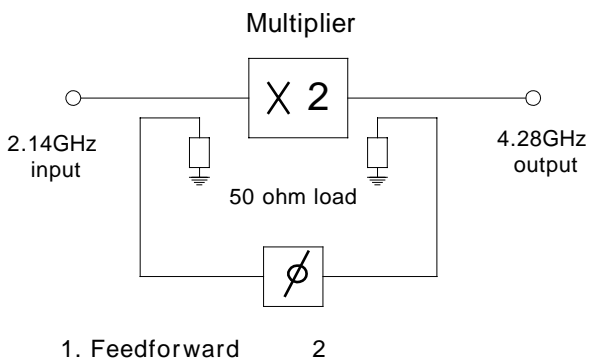
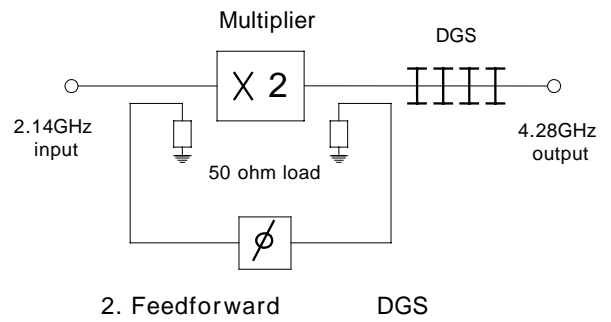
1) Feedforward

Feedforward
 [1] - [3],

a=3.5mm,
 b=3.5mm, d=7mm, g=0.5mm , DGS
 32mm x 17mm
 2fo , 3fo 4fo

ERA - 4SM MMIC

P_{1dB}
 2
 1
 forward 2
 가



3. DGS

2) Feedforward DGS

3 4

4

2

5 Feedforward

6 7 DGS

Feedforward DGS

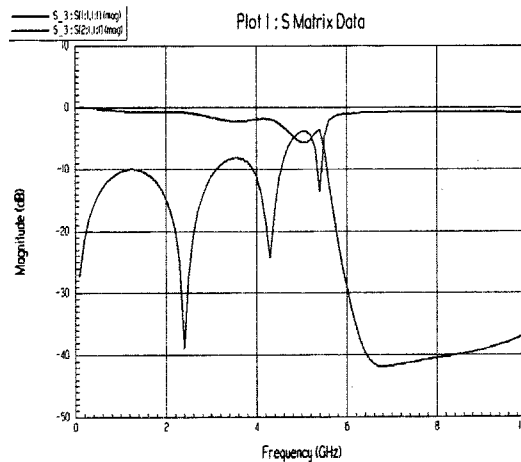
2

8

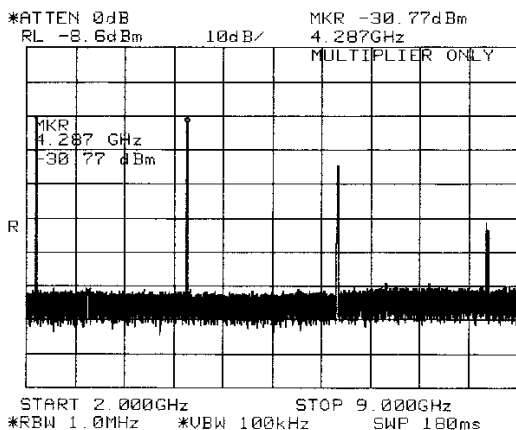
49.4dB, 3

33.5dB, 4

20dB

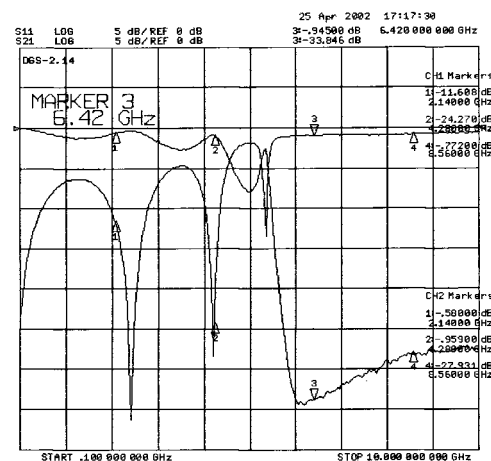


6. DGS

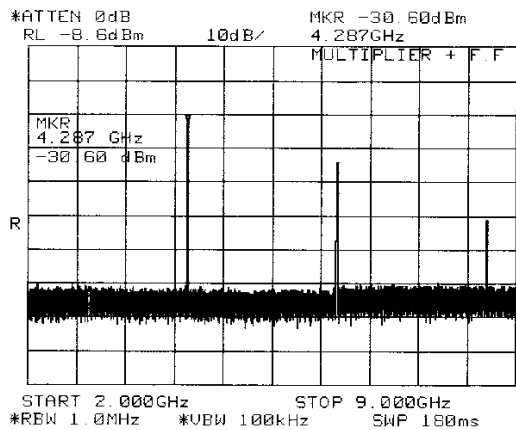


4.

2

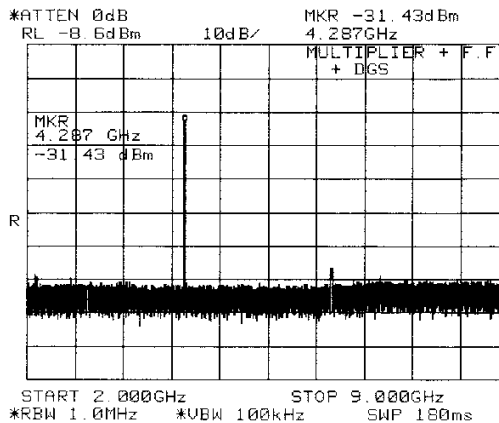


7. DGS



5. Feedforward

2



8. Feedforward

DGS

	1.	[dBm]	
		Feedforward	Feedforward DGS
f_0	-28.6	-78.6	-78
$2f_0$	-29.8	-30.6	-31.4
$3f_0$	-43.1	-42.9	-76.6
$4f_0$	-60.3	-60	

MMIC

(R01 - 2000 -

00257)

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