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A NOVEL FREQUENCY DOUBLER USING FEEDFORWARD STRUCTURE AND DGS MICROSTRIP FOR FUNDAMENTAL AND HIGHER-ORDER COMPONENTS SUPPRESSION

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In this paper, a novel design concept of a frequency doubler using feedforward technique and defected ground structure(DGS) microstrip line is proposed. The feedforward loop plays a role of fundamental frequency suppression and DGS microstrip line suppresses over the 3rd order harmonic components. By using this new concept, the high suppression for the undesired signals could be achieved easily. The proposed technique is experimentally demonstrated in 1.85GHz to 3.7GHz frequency doubler. The output power of –3dBm at the frequency of 3.74GHz ($2f_o$) is measured with 42.9dB suppression of the fundamental frequency signal (f_o), 20.2dB suppression of the 3rd harmonic signal ($3f_o$) and 29.7dB suppression of the 4th harmonic signal ($4f_o$). The conversion loss of –2.34dB ~ –5.8dB at the bandwidth of 100MHz, the phase noise of –97.51dB/Hz(@10KHz) were measured.

1. Introduction

There is a demand for high stability and low phase noise signal source in microwave and millimeter-wave communication and radar systems. These sources can be easily obtained by multiplying low frequency signal that has high stability and low phase noise relatively. Generally multiplier include a fundamental component and harmonic components besides multiplied signal, so it makes serious problems when multiplier is operated with other microwave circuits such as mixer and amplifier and so on. To solve these problems, a quarter-wavelength open stub or balanced multiplier design is used to suppress fundamental frequency component. But these methods show limitation of fundamental signal suppression about 25dB generally. Also a band pass filter can be used for suppression of the fundamental and several harmonic signals. But the insertion loss of a band pass filter causes multiplied signal level to diminishment of multiplied signal level, and impossible to make fully monolithic transceiver because of high Q-factor bandpass filter[1][2].

In this paper, a new structure of doubler that suppresses fundamental frequency component and the 3rd order harmonic signals without band pass filter is proposed. Proposed method is composed of feedforward technique that can effectively suppress intermodulation distortion in power amplifier design and defected ground structure(DGS) microstrip line realized by etching a few dumb-bell shaped patterns on the ground plane of microstrip line. Feedforward technique is used to suppress the fundamental signal and DGS microstrip line is used to suppress 3rd order harmonic components.

2. Theory

2.1. General frequency doubler

The output current waveform to input voltage waveform of the transistor according to conduction angle is showed in figure 1. The harmonic signals generation to the bias is represented by (1) and (2), where α is conduction angle of input signal. Figure 2 shows the amplitudes of the DC to 5th harmonic signal. When the conduction angle is 120°, the amplitude of the 2nd harmonic signal is maximum, therefore a bias point of transistor must be selected in the vicinity of pinch-off, between class B and C.

After the bias selection, the input and the output port have been matched by fundamental signal (f_o) and 2nd harmonic signal ($2f_o$) respectively, to maximize the 2nd harmonic component in the output port .

$$I_n = \frac{1}{\pi}\int_{-\frac{\alpha}{2}}^{\frac{\alpha}{2}} \frac{I_{max}}{1-\cos\frac{\alpha}{2}}\left(\cos\omega t - \cos\frac{\alpha}{2}\right)\cos n\omega t\, d\omega t \quad (1)$$

$$I_{dc} = \frac{1}{2\pi}\frac{I_{max}}{1-\cos\frac{\alpha}{2}}\left(2\sin\frac{\alpha}{2} - \alpha\cos\frac{\alpha}{2}\right) \quad (2)$$

2.2 The frequency doubler using the feedforward structure

The feedforward technique is widely used to remove the intermodulation distortion in power amplifier design and it has a wide operating frequency band and hardly oscillates because there is no feedback path. In this paper, the 1st loop scheme of feedforward technique has been used for fundamental frequency suppression and figure 3 shows block diagram of the doubler. Because active multiplier attenuates the fundamental signal level theoretically, the fundamental signal can be suppressed by adjusting the coupling coefficients of the couplers which are located before and after the multiplier and the phase constant of the phase shifter[3][4].

2.3 The DGS microstrip line

Etching a few dumb-bell shaped patterns on the ground plane located just below microstrip line are equivalent to increase of serial inductance of transmission line impedance. The width of the DGS microstrip line must be broader than that of the conventional microstrip line to maintain the specific characteristic impedance. That is equivalent to increase of shunt capacitance of transmission line impedance. Increasing the series inductance and the shunt capacitance induces increase of phase constant and slow-wave effect. So the DGS microstrip line contributes to circuit downsizing. If we apply the DGS microstrip line at output terminal of frequency doubler, the harmonic signals over the 3rd order can be suppressed effectively due to low pass filtering characteristic of DGS microstrip line[5].

2.4. The frequency doubler using the feedforward structure and the DGS

In this paper, the feedforward technique and the DGS transmission line are used to suppress over the 3rd order harmonics as well as fundamental frequency. Figure 3 shows the block diagram and the expectable frequency spectra. The structure of the DGS microstrip line is represented in figure 4. The defected cell parameters are a=4mm, b=3.5mm, d=9.3mm, g=0.5mm, w=2.38mm, w_{dgs}=4.37mm. Adjusting the etching cell parameters, the DGS microstrip line controls the low-pass filtering characteristic under 2nd harmonic frequency. EM simulation is done with Ansoft HFSS v.8.0.

3. Experiment and Measured results

To show the validation of proposed frequency doubler, we designed frequency doubler multiplying 1.87GHz to 3.74GHz. The used transistor is ATF10136 MESFET of HP and the drain voltage is set 1.2V and the gate voltage is –1.25V to operate near pinch-off voltage region, between class B and C. Then we extracted the input and output matched points using the load-pull method and implemented matching circuits using ADS of Agilent. Figure 5 shows the output characteristic of the fabricated single-ended frequency doubler, which spectra shows the fundamental frequency signal and over the 3rd order harmonic signals as well as the 2nd order multiplied signal. The single-ended doubler has -2.55dB conversion loss and -25.94dB suppression of the fundamental signal for 0dBm input signal. Figure 6 shows the output characteristic of the frequency doubler that suppresses the fundamental signal by applying the feedforward structure. The result shows that the fundamental frequency signal is suppressed about 42.2dB. Figure 7 shows the

fabrication characteristic of the DGS microstrip line. It shows low-pass filter characteristic that cut-off frequency is 4GHz and insertion loss is 0.4dB at 3.74GHz and attenuation value at 5.55GHz is more than 23dB. This means that the DGS microstrip line can terminate over the 3rd order harmonic signals. Figure 8 shows the characteristic of frequency doubler applying the feedforward structure and DGS microstrip line. For the input power of 0dBm, the output power level of frequency doubler is -3dBm with 42.9dB, 20.2dB and 29.7dB suppression of the fundamental, the 3rd harmonic and the 4th harmonic signal, respectively. Table 1 summarizes signal levels of the fabricated frequency doubler. We can see the fundamental frequency signal level before using feedforward structure and after using feedforward structure. Figure 9 shows the conversion loss according to the frequency variation. The conversion loss is -2.9dB at the 3.74GHz and the variation of the conversion loss is -2.34dB(@3.71GHz) to -5.8dB (@3.79GHz), ±1.73dB within 100MHz bandwidth. Figure 10 shows the input and output phase noise characteristic of frequency doubler. Output phase noise measurement shows 97.51dBc/Hz (@10KHz offset) in case of input signal –101.3dB, which is better than the theoretical phase worse condition, 20logN = 20log(2) = 6dB, by 2.2dB. Maybe this result is due to elimination of the fundamental signal and matching of over the 3rd order harmonic signals. Figure 11 shows the photograph of the fabricated frequency doubler. The DGS structure is circled by dashed line. Table 2 summarizes the characteristics of the fabricated frequency doubler.

4. Conclusion

In this paper, the new design technique of the frequency doubler was proposed to obtain sources that have high stability and low phase noise. The fundamental frequency signal was suppressed by using feedforward structure and over the 3rd order harmonics were suppressed by using DGS structure. As a result, variations of suppression were 42.9dB, 19.2dB and 29.7dB for the fundamental, the 3rd order harmonic and the 4th order harmonic signal, respectively. Because the fabricated doubler consists of a transistor, diodes and hybrid circuits, overall circuits can be integrated in monolithic form. We expect that monolithic frequency doubler, that doesn't contain the fundamental and over 3rd harmonics, can contribute to improve communication quality without any high Q bandpass filter.

Acknowledgements

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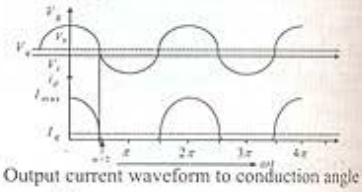


Fig. 1. Output current waveform to conduction angle

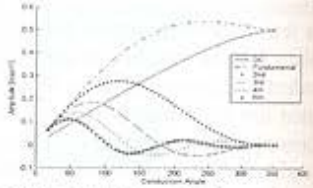


Fig. 2. Amplitude comparison of the harmonic components to conduction angle

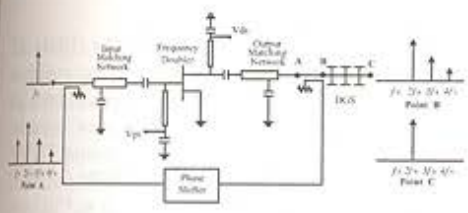
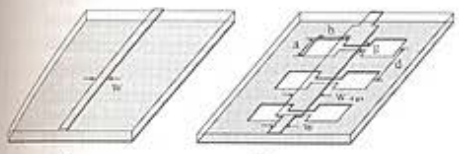


Fig. 3. Block diagram of doubler using feedforward structure and DGS



(a) (b)

Fig. 4. (a) Layout of a standard microstrip line
(b) Layout of DGS microstrip line

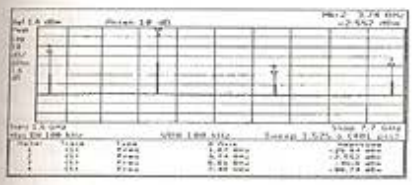


Fig. 5. Output characteristic of the fabricated frequency doubler

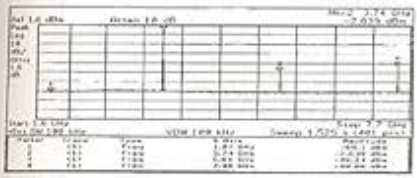


Fig. 6. Output characteristic of the frequency doubler using feedforward.

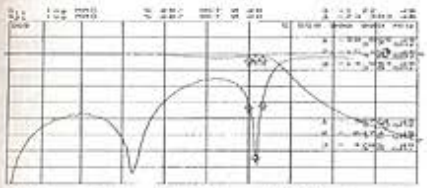


Fig. 7. Characteristic of the fabricated DGS microstrip line.

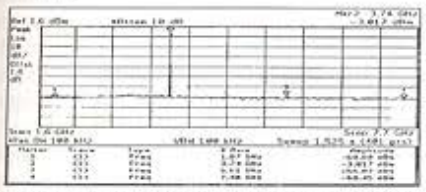


Fig. 8. Output characteristic of the frequency doubler using feedforward and DGS

Table 1.
Output characteristic of each doubler structure[dBm]

	P_{f0}	P_{2f0}	P_{3f0}	P_{4f0}
Only Doubler	-25.94	-2.55	-46.8	-38.74
F.F+ Doubler	-68.1	-2.64	-46.24	-40.08
F.F+DGS +Doubler	-68.88	-3.02	-66.02	-68.45

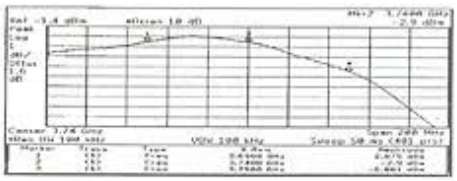
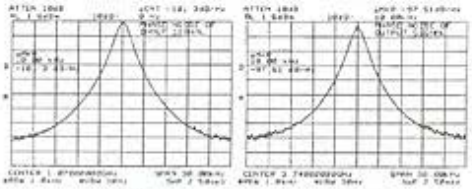
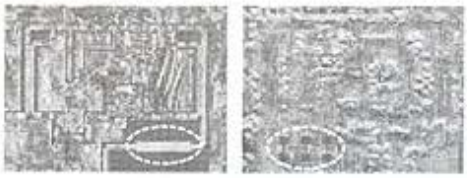


Fig. 9. Conversion loss according to the frequency variation



(a) (b)

Fig. 10. Phase noise measurement results of the fabricated frequency doubler (a) input signal (b)output signal



(a) (b)

Fig. 11. Photographs of the fabricated frequency doubler
(a)Top view (b) Bottom view

Table 2. Output Characteristic of the frequency doubler

Item	Results	Unit
Frequency range	3.69 ~ 3.79	GHz
Bandwidth	100	MHz
Output power	-2.34 ~ -5.8	dBm
Conversion loss	-2.34 ~ -5.8	dB
P1dB	-1.5	dBm
Phase noise improvement	2.2	dB
Current	14	mA
Voltage	1.2	V

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