HBT Doherty Amplifier Using Ballast Resistor Control and Arbitrary Termination Impedance Power Divider

Nam-Sik Ryu, Su-Tae Kim, Su-Jin Seo, Yong-Chae Jeong
Dept. of Information & Communication Engineering, Chonbuk National University,
664-14, Duckjin-Dong, Duckjin-Gu, Jeonju, Korea, 561-756

***Abstract* — In this paper, a new HBT Doherty amplifier is designed with arbitrary termination impedance power divider and ballast resistor control method to enhance the dynamic gain flatness. By using the arbitrary termination impedance power divider, circuit size of the proposed HBT Doherty amplifier has been reduced considerably. Also, due to the fact that the gain of a peaking amplifier usually deteriorates the dynamic gain flatness of a Doherty amplifier, we proposed a novel technique of controlling ballast resistors according to the bias condition of a peaking amplifier. By tuning the ballast resistors and bias of peaking amplifier, we improved gain flatness of a Doherty amplifier maintaining permissible power added efficiency (PAE) at the same time. The proposed Doherty amplifier is designed at 1.9GHz with Knowledge-on HBT process. Obtained the maximum power and the power gain through the simulation are 29dBm and 14.4dB, respectively. The PAE at the maximum output power was 64% with 3.3V supply voltage and achieved more than 60% over 5dB range.**

Key Words: HBT Doherty amplifier, ballast resistor control, arbitrary impedance matching.

I. INTRODUCTION

Recently, many studies for performance improvement of power amplifier that is one of important part in wireless communication system have performed. These studies mostly concentrate on the improvement of output power, linearity and PAE. Among these, Doherty amplifier which uses a method of load modulation and maintain high efficiency for wide output power range is interested by many amplifier designers [1][2].

The Doherty amplifier essentially needs a peaking amplifier to adapt the load impedance of the carrier power amplifier. However, it is difficult to implement load for realizing this, even if it is realized, it has problem of nonlinear behavior of dynamic gain. In previous, bias control according to the power level has been introduced but has problem of increase in circuit size [2] [3].

In this paper, we propose the ballast resistors control according to peaking amplifier bias condition, so that the Doherty amplifier has a flat gain for dynamic input power range. Also, by using the power divider having arbitrary termination impedance, the proposed Doherty amplifier could have reduced the number of components for matching and phase compensation, so that the overall circuit size is reduced.

II. DOHERTY AMPLIFIER

The output power of a peaking amplifier in the Doherty amplifier is combined with that of a carrier amplifier through the λ/4 transformer, as shown in Fig. 1. In ordinary, the input signal is divided with hybrid and then impedance-transformed to source impedance of transistor. In IC circuit design, the transmission line and matching network are realized with lumped-elements. So the number of the lumped-elements determines the overall circuit size. If Wilkinson power divider having arbitrary termination impedance is adopted, input matching of transistor is changed simply and the number of element is reduced remarkably and the operation bandwidth of the power divider is broaden.

Fig. 2 shows the proposed Doherty amplifier topology using arbitrary termination impedance power divider. Fig. 3 shows lumped element equivalent circuit of transmission line and Fig. 4 shows Wilkinson power divider having arbitrary termination impedance.

Usually carrier amplifier operates as class A or class AB and peaking amplifier operates as class C. In the low input power level, only the carrier amplifier operates and the peaking amplifier is in off state due to low bias condition. In this region, the efficiency of carrier amplifier increases linearly according to the output power and reaches its first peak value. In the

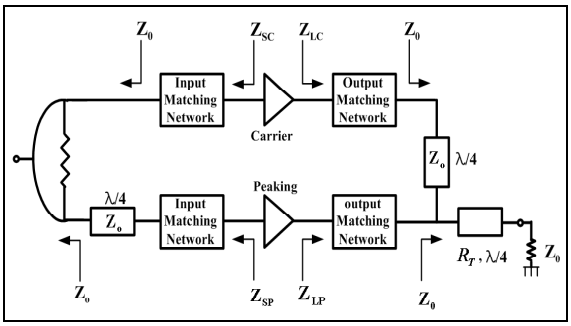


Fig. 1 The conventional Doherty amplifier topology

region from the first peak to the maximum output power, the peaking amplifier begins to operate and the current contribution from it affects the effective load impedance of the carrier amplifier. By the load modulation, the carrier amplifier maintains saturation and the efficiency of a peaking amplifier increases linearly.

In Fig.5, you can find saggy portion between the two efficiency peaks, and it is due to the fact that the efficiency is low when the amplifier operates at the low output power region.

Generally, the gain and the maximum output power of peaking amplifier that is operating in class C are lower than

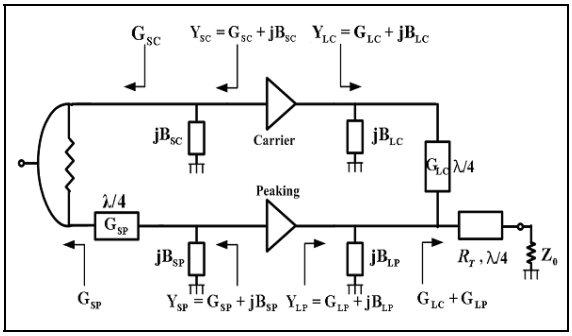


Fig. 2. The proposed Doherty amplifier topology.

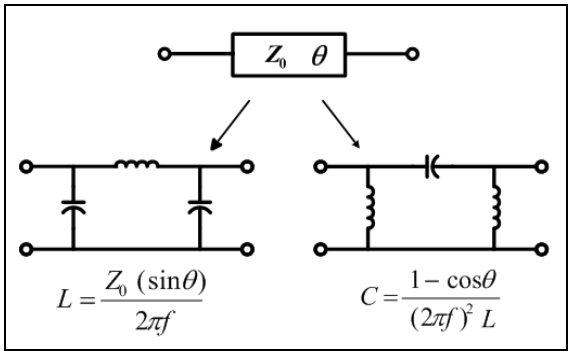


Fig. 3. π-type equivalent circuit of transmission line.

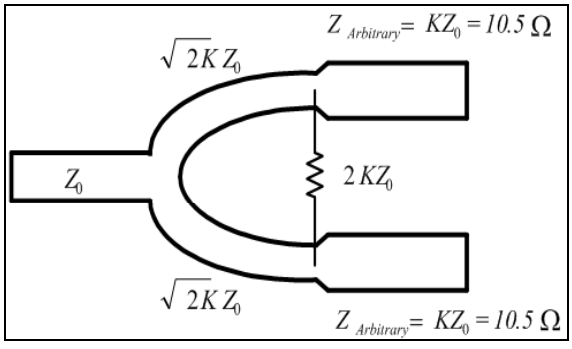


Fig. 4. Wilkinson power divider terminated by arbitrary impedances.

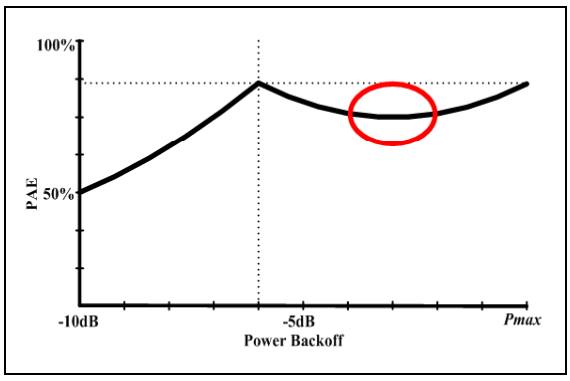


Fig. 5. Efficiency vs power backoff of Doherty amplifier.

that of the same size carrier amplifier that is operating in class A or class AB. Compared to CMOS process which gain is increased with the width of transistor, HBT process changes a little gain according to number of cell. And the maximum output power of the peaking can be exalted, but the circuit size and the power consumption are also increased. If the same transistor is used as the carrier and the peaking amplifier, this deteriorates the constant gain in dynamic range. From a linearity point of view, it means AM-to-AM distortion. In optimizing the Doherty amplifier dynamic gain characteristics, it is essential that (1) class C peaking amplifier should have increased gain at maximum power level and (2) it should not operate at low power level.

In designing HBT amplifier, ballast resistors are essential to compensate the stability of transistor and protect bad influences from thermal effect. And selection of ballast resistor is an important factor in DC and RF characteristics. Since peaking amplifier designed with class C is more stable than carrier amplifier designed with class AB, we used the method of gain increase of peaking amplifier by controlling the bias point and value of ballast resistors to compensate dynamic gain flatness.

III. Design of Doherty Amplifier

We used the GaAs HBT VBIC model of Knowledge-on in Korea to design the Doherty power amplifier. And the same structure is used for carrier and peaking amplifier, but ballast resistor of these is different. This Doherty amplifier is designed with fully on-chip at the center frequency of 1.9GHz. On comparing of conversion the Wilkinson power divider and other hybrid divider to π-type equivalent lumped circuit, Wilkinson power divider has much less number of lumped elements. So we adopt Wilkinson power divider structure, and reduced the circuit size and insertion loss. Since input impedance of carrier amplifier and peaking amplifier are 10.5Ω at maximum output power level, output port termination impedance of Wilkinson power divider is designed with 10.5Ω instead of 50Ω to reduce the number of input matching lumped

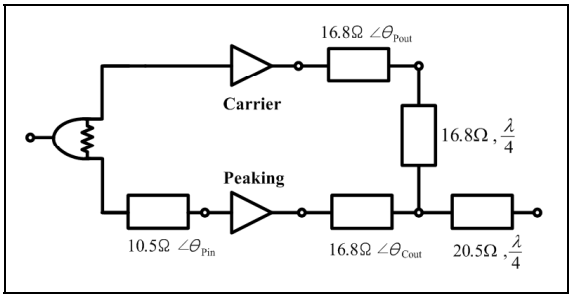


Fig. 6. Designed Doherty amplifier schematic.

elements. Output impedance of carrier amplifier and peaking amplifier are 16.8Ω at maximum output power level of 26dBm, and λ/4 impedance transformer is decided to 16.8Ω for load impedance modulation. When low power signal is applied, peaking amplifier should not operate and output offset transmission line is attached to infinite Z_{out}. And for the in-phase combining at output junction, phase compensation is also considered. These specific transmission lines and λ/4 impedance transformer are converted into π-type lumped elements to realize in fully on-chip.

When low power signal is applied, peaking amplifier should not operate and output offset transmission line is attached to infinite Z_{out}. And for the in-phase combining at output junction, phase compensation is also considered. These specific transmission lines and λ/4 impedance transformer are converted into π-type lumped elements to realize in fully on-chip. Fig. 6 shows designed Doherty amplifier schematic finally.

To show validity of the proposed Doherty amplifier, the general class AB amplifier, the conventional Doherty amplifier that consists of class AB carrier amplifier and class C peaking amplifier, and the unequal Doherty amplifier that is the conventional Doherty amplifier with 2:1 unequal power divider to compensating the gain of peaking amplifier are also designed.

Fig. 7 shows PAE characteristic of designed conventional Doherty amplifier and class AB amplifier. Doherty amplifier has improved PAE characteristic over class AB amplifier through whole dynamic range. But a demerit of decreased gain characteristic at high input power level and lowered P_{1dB} characteristic are appeared because the gain of peaking amplifier is lower than carrier amplifier at high input power level.

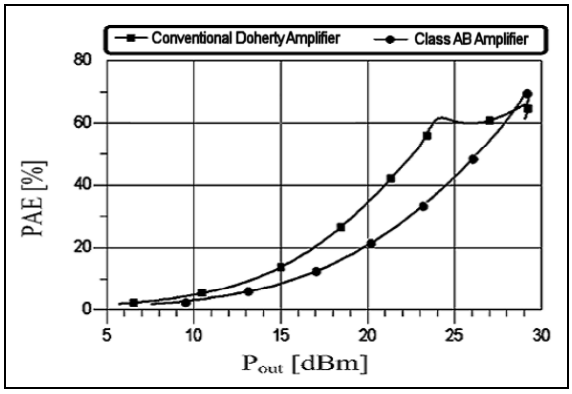


Fig. 7. Efficiency characteristic of Doherty amplifier and class AB amplifier.

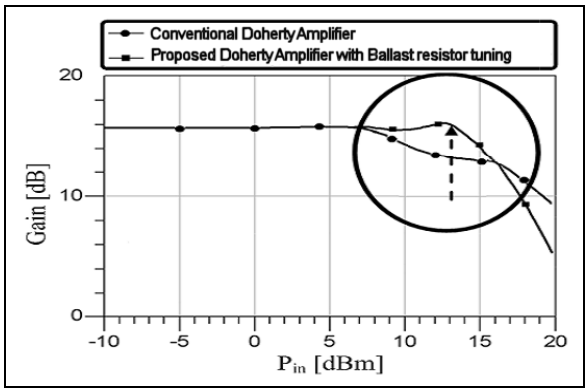
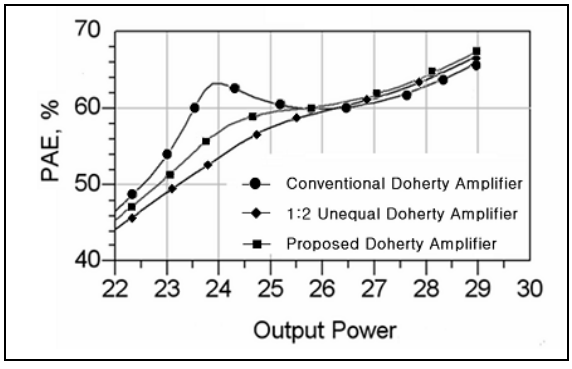


Fig. 8. Gain improvement of proposed Doherty amplifier with tuned peaking amplifier.

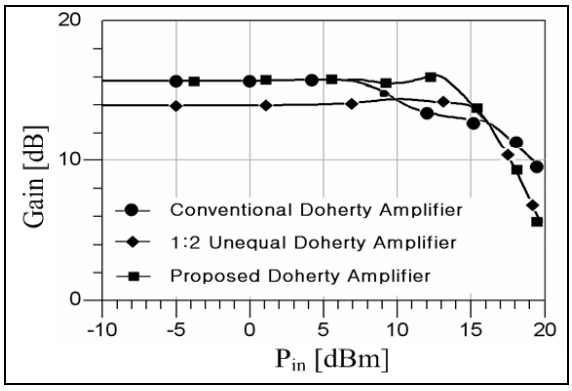
Fig. 8 shows increased gain characteristic of the proposed Doherty amplifier at high input power level. Without adding any additional elements on the proposed Doherty amplifier, we obtained gain improvements through the tuning of the ballast resistors which are essential for HBT amplifier design.

Comparison of three other cases of Doherty amplifier configurations is shown in Fig. 9. Conventional Doherty amplifier shows nearly ideal PAE characteristic, however, the gain at high power level drops abruptly. Although the unequal divide Doherty amplifier shows flat gain for overall power range, the gain is lower than that of the conventional one, and also the first peak of PAE is hardly visible. In contrast to those results, with the proposed design method of tuning ballast resistors, we achieved good gain flatness without dropping gain and without shrinking the first peak of PAE much.

The layout of the proposed Doherty amplifier is shown in Fig. 10 and the implemented overall chip size is 1050um× 2250um.



(a) Efficiency characteristic of Doherty amplifier



(b) Gain characteristic of Doherty amplifier

Fig. 9. Comparison of PAE and gain characteristic of three kinds Doherty Amplifier.

IV. CONCLUSION

In this paper, Doherty power amplifier is designed using the HBT process. And by using the Wilkinson power divider that has arbitrary termination impedance, this amplifier reduces matching elements and insertion loss than conventional Doherty power amplifier. Doherty amplifier is optimized by tuning the ballast resistor that is essentially needed for HBT process, so that the constant dynamic gain and the relatively high gain are achieved.

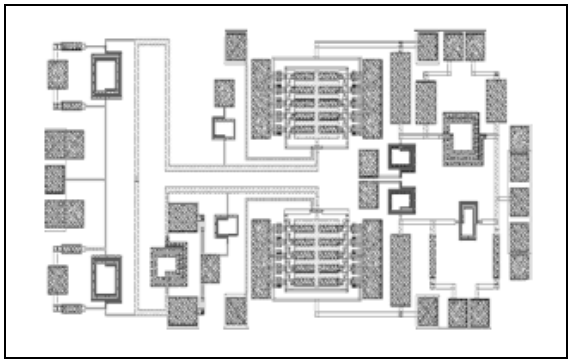


Fig. 10 1050um×2250um HBT layout.

REFERENCE

[1] W. H. Doherty, "A new high efficiency power amplifier for modulated wave.", *Proc. IRE*, vol. 24, pp. 1163-1182, Sep. 1936

[2] F. H. Raab "Efficiency of doherty RF power amplifier systems,", *IEEE Trans/ Broadcast*., vol. bc-33, pp. 77-83, Sep. 1987.

[3] Jeonghyeon Cha, "An adaptive bias controlled power amplifier with a load-modulated combining scheme,", *IEEE MTT-S Int. Microwave Symp. Dig*., pp. 81-84, 2003.

[4] C. F. Campbell, "A full integrated Ku-band Doherty amplifier MMIC," *IEEE Microwave Guided Wave Lett*., pp. 114-116, Sep. 1999.

[5] I. Masaya, et al., "An Extended Doherty Amplifier with High Efficiency over a Wide Power Range," *IEEE Trans. Microwave Theory Tech*., vol. 49 no. 12, Dec. 2001.