A Novel Design of Frequency Multiplier Using Feedforward Technique and Defected Ground Structure

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***Abstract* — A novel design of frequency multiplier using a feedforward technique and a defected ground structure (DGS) is proposed. The feedforward loop in the proposed frequency multiplier suppresses the fundamental component (f_0), the dumb-bell or spiral shaped DGS diminish unwanted harmonics such as second, third, fourth. Due to the combination of the feedforward structure and the DGS, only the multiplied frequency component ($2f_0$, $3f_0$, $4f_0$) appears at the output port and the other unwanted components are suppressed excellently. The frequency multipliers are designed at 1 GHz of f_0, by the proposed technique and measured. The measured output power of $2f_0$, $3f_0$, $4f_0$ is -2.59 dBm, -5.36 dBm, -4.57 dBm, respectively, when the input power is 0 dBm.**

I. INTRODUCTION

Recently, there is need of the signal source with high stability and low phase noise in microwave, millimeter-wave communication and radar systems. High frequency signal sources can be easily obtained by multiplying low frequency signal that has relatively high stability and low phase noise. However, in general, frequency multipliers include the unwanted fundamental and harmonic frequency components.

Serious problems may occur due to the undesirable frequency components, when a multiplier operates with other microwave circuits such as mixer, amplifier, and so on. In order to suppress the fundamental frequency component, quarter-wavelength open stub or balanced multiplier structure is adopted [1]–[3]. But these methods have the limitation of suppression only 20~25dB generally. A band pass filter is in common used to diminish the fundamental and unwanted harmonic components. But the insertion loss of the band pass filter causes multiplied signal to be less than the required signal level. In addition, it is not easy to make high Q factor band pass filter in monolithic microwave integrated circuit, fully monolithic frequency multiplier design is very difficult.

In this paper, a novel frequency multiplier that suppresses fundamental and unwanted harmonic components is proposed. The proposed multiplier is composed of the feedforward structure, which is widely used in linear power amplifiers, and defected ground structure (DGS) realized by etching a few dumb-bell or spiral shaped patterns on the ground plane of microstrip line [4]. Several applications using DGS to design a coupler, filter, and power amplifier have been already presented [5]–[7]. The feedforward loop suppresses f_0 signal and DGS cut down the other unwanted harmonic components effectively than previous method.

II. THEORY

The output current waveform to input voltage of transistors can be explained according to bias condition or conduction angle. The dc current consumption and harmonic signals to the bias are estimated by using averaging and correlation between a drain (or collector) current and the n^{th} harmonic as shown in (1), (2) and Fig. 1, where α is a conduction angle of input signal and I_{max} is the maximum allowable current [8]. The amplitude of the second harmonic, third harmonic and fourth harmonic is maximum when α is around 120°, 75° and 60°, respectively. Therefore, the bias point for frequency multiplier should be selected in the vicinity of pinch-off, between class B and C. Once the bias is determined, the input and output ports have to be matched for fundamental (f_0) and multiplied harmonic signal to maximize, respectively.

$$I_{dc} = \frac{1}{2\pi}\int_{-\alpha/2}^{\alpha/2} \frac{I_{\max}}{1-\cos(\alpha/2)}\left[\cos\theta - \cos(\alpha/2)\right]d\theta \quad (1)$$

$$I_n = \frac{1}{\pi}\int_{-\alpha/2}^{\alpha/2} \frac{I_{\max}}{1-\cos(\alpha/2)}\left[\cos\theta - \cos(\alpha/2)\right]\cos n\theta d\theta \quad (2)$$

Fig. 2 is the proposed frequency multiplier, which adopts the feedforward structure to suppress f_0 and DGS microstrip line to diminish the unwanted harmonics. f_0 can be more suppressed by adjusting attenuation of a variable attenuator("A") and phase of the variable phase shifter("Φ") [9]. To perfect cancellation, the magnitude and phase of f_0 are equal and out-of-phased at output coupler of the feedforward structure.

The DGS pattern under the microstrip line produces the additional equivalent inductance and increased characteristic impedance. In conventional microstrip lines, the line width is getting extremely narrower as the required line impedance increases. However, in the microstrip line with DGS, the line width is broader than that of the standard microstrip line for the same characteristic impedance because the additional inductance results in the highly increased characteristic impedance. The broadened width of the DGS microstrip line can be understood as the increased equivalent capacitance, which plays a great role in raising the phase constant and slow-wave effects [7].

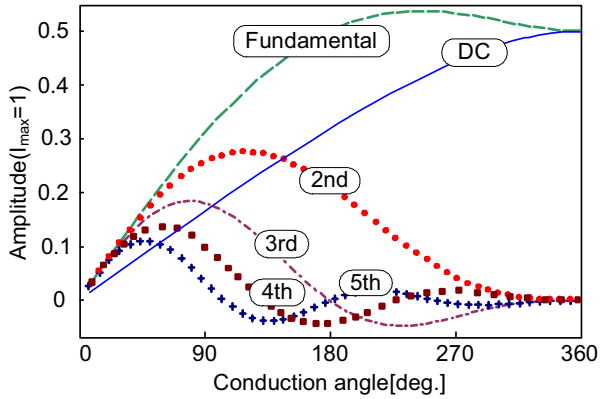

Fig. 1. Amplitude comparison of the fundamental and harmonic components versus conduction angle.

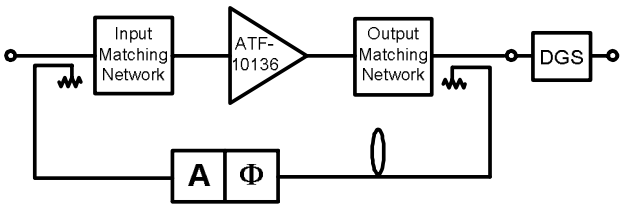

Fig.2. Block diagram of the proposed frequency multiplier.

The dumb-bell shaped DGS has a characteristic of low pass filter, and the spiral shaped DGS has a characteristic of band rejection filters. If we use the unequal spiral shaped DGS, we could obtain the characteristic of dual-band rejection, simultaneously. In this work, the dumb-bell shaped DGS microstrip line is used to diminish the higher-order harmonics over the third of doubler. The asymmetrical spiral shaped DGS is used to suppress the harmonics of $2f_0$, $4f_0$ of the tripler and the harmonics of $2f_0$, $3f_0$ of the quadrupler.

Fig. 3 shows the layouts of DGS of frequency multiplier. The substrate is RT/duroid 5880 with the dielectric constant of 2.2 and thickness of 31 mils. The DGS cell dimensions are; s=sw=0.2mm, gs=0.25mm, a=b=6mm, c=7.6mm, d=7.4m, w=2.4mm, wd=5.8mm, gd=0.3mm, d1=11mm, d2=14mm, and d3=12mm. By adjusting the DGS cell parameters, it is possible to control the electrical filtering characteristics.

Fig. 4 shows the simulated and measured S_{11} and S_{21} of dumb-bell and unequal spiral shaped DGS microstrip line. It is simulated on Ansoft HFSS 9.0. Fig. 4(a) is represented low pass filer characteristic of dumb-bell DGS, and asymmetrical spiral DGS at (b) and (c) has characteristics that are just like those of dual band rejection filters. Table I summarizes the suppression characteristics of the fundamental and harmonics in DGS microstrip line. The insertion loss of the harmonic multiplied is within -0.5dB, and the suppression of unwanted harmonics is more than 24.6dB.

III. Experiment and Measured Results

We have designed the frequency multiplier that multiplies 1GHz of fundamental signal to produce the frequency output at 2GHz, 3GHz, and 4GHz. The selected transistor is ATF10136 MESFET. The drain and gate bias voltages are set to 1.25 V and -1.3V for doubler, to 1.2V and -1.25V for tripler, to 1.3V and -1V for quadrupler, respectively. The transistors are

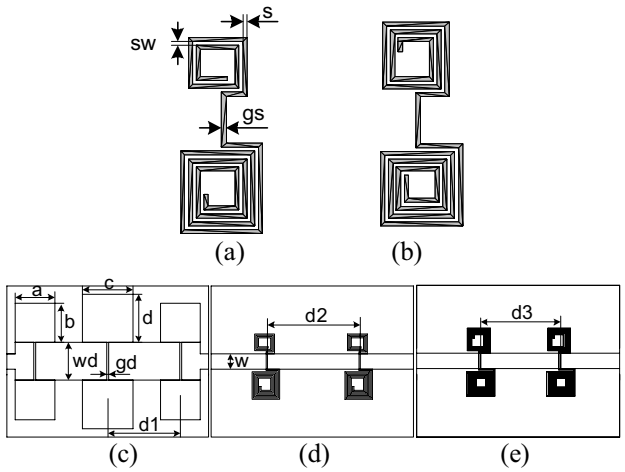

Fig. 3. Layout of DGS of frequency multiplier (a) spiral DGS unit for tripler, (b) spiral DGS unit for quadrupler, (c) for frequency doubler, (d) for frequency tripler, (e) for frequency quadrupler.

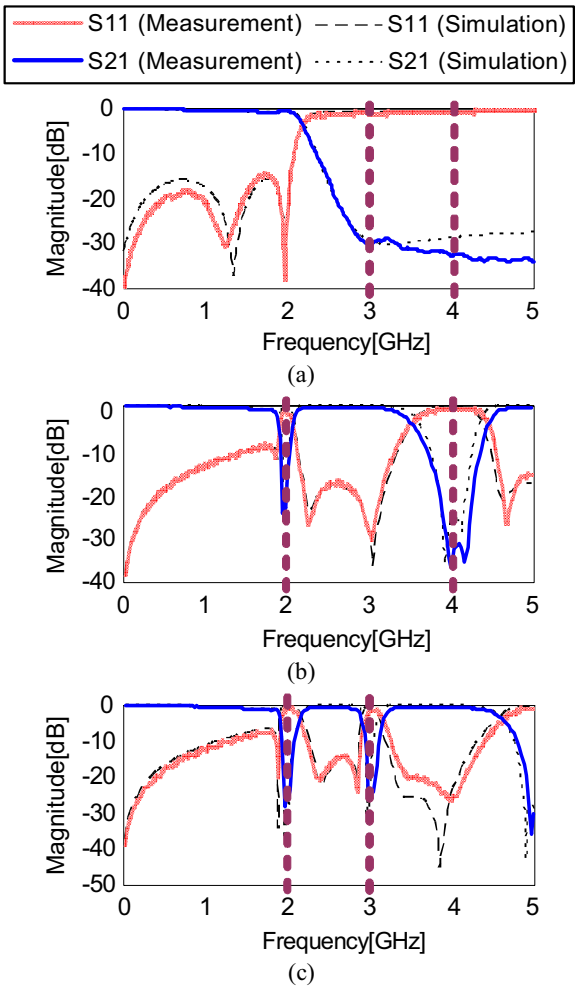

Fig. 4. Simulated and measured results of the DGS (a) for frequency doubler, (b) for frequency tripler, (c) for frequency quadrupler.

TABLE I
DGS Measurement Results

f_0=1GHz	S_{21}[dB]			
	f_0	$2f_0$	$3f_0$	$4f_0$
DGS(@doubler)	-0.41	-0.49	-30.17	-32.78
DGS(@tripler)	-0.41	-26.14	-0.36	-36.47
DGS(@quadrupler)	-0.30	-24.62	-25.19	-0.47

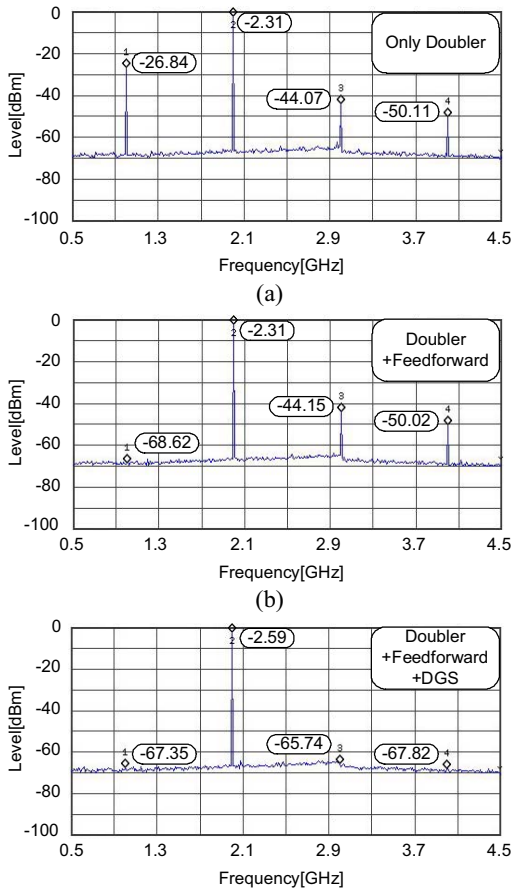

Fig.5. Measured spectrum of the frequency doubler.

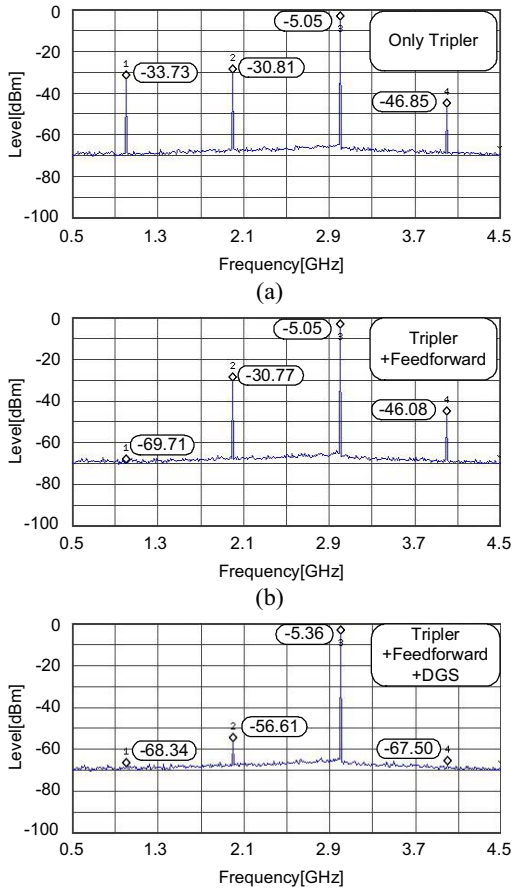

Fig. 6. Measured spectrum of the frequency tripler.

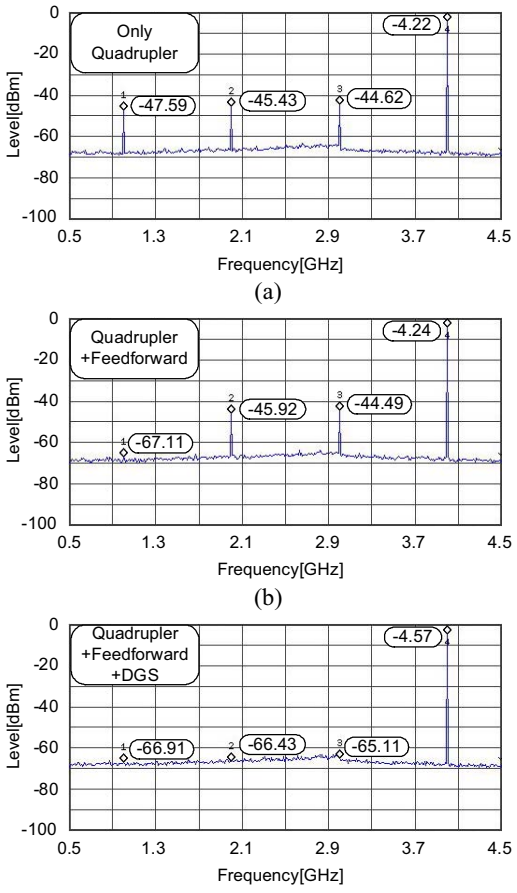

Fig. 7. Measured spectrum of the frequency quadrupler.

TABLE II
OUTPUT SIGNAL COMPARISON OF FREQUENCY MULTIPLIER STRUCTURES [dBm]

	P_{f0}	P_{2f0}	P_{3f0}	P_{4f0}
Only Doubler	-26.84	-2.31	-44.07	-50.11
Doubler+FF	-68.62	-2.31	-44.15	-50.02
Doubler+FF+DGS	-67.35	-2.59	-65.74	-67.82
Only Tripler	-33.73	-30.81	-5.05	-46.85
Tripler +FF	-69.71	-30.77	-5.05	-46.08
Tripler +FF+DGS	-68.34	-56.61	-5.36	-67.50
Only Quadrupler	-47.59	-45.43	-44.62	-4.22
Quadrupler +FF	-67.11	-45.92	-44.49	-4.24
Quadrupler +FF+DGS	-66.91	-66.43	-65.11	-4.57

biased near pinch-off voltage region between class B and C. The matching points for input and output networks were determined by using the source and load-pull method and implemented by simulation on Agilent ADS.

Fig. 6 ~ 8 shows the measured output spectrum of the frequency doubler, tripler and quadrupler. That is the conventional frequency multiplier, the frequency multiplier having the feedforward structure only and the proposed frequency multiplier having the feedforward structure and the DGS microstrip line. Table II summarizes output spectrum characteristics of several frequency multiplier structures.

The measured phase noise of the output signal ($2f_0$, $3f_0$ and $4f_0$) are -94.06dBc/Hz, -93.90 dBc/Hz and -92.2 dBc/Hz (at 10-KHz offset) for that of input signal -94.98

dBc/Hz, which is better than the theoretical phase degradation condition expressed by 20log(2)=6dB, 20log(3)=9.5dB and 20log(4)=12dB, by 5.08 dB, 8.42dB and 9.22dB, respectively. It is believed that this result is due to the clear elimination of the fundamental signal and unwanted harmonic signals. The DGS microstrip line is operated as harmonic short. So the phase noise of the proposed frequency multiplier is improved than the conventional.

V. Conclusion

The new design technique for frequency multiplier was proposed to obtain signal sources that have high stability and low phase noise. The fundamental frequency signal was excellently suppressed by using feedforward structure, and the unwanted harmonics were removed due to the DGS microstrip line. The measured suppressions of the fundamental, third, and fourth harmonic components were 40.51, 21.67, and 17.71 dB for the doubler, respectively. For the tripler, the amount of harmonic suppression is 34.61, 25.80, and 20.65 dB, respectively. For the quadrupler, the harmonic suppressions are 19.32, 21.00 and 20.49dB, respectively. It is believed that the proposed frequency multiplier can be integrated in monolithic integrated circuits form because the fabricated frequency multiplier consists of a transistor, diodes, and hybrid circuit elements. It is also expected that the proposed frequency multiplier have a great contribution to improve the quality of communication without high Q band pass filters.

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