Doherty Amplifier Using Load Modulation and Phase Compensation DGS Microstrip Line

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Abstract **— In this paper, a new Doherty power amplifier having the ideal harmonic termination condition that has been usually ignored is proposed. A defected ground structure (DGS) is adopted on the ground pattern of the output λ/4 impedance inverter of the carrier amplifier and output offset transmission line of the peaking amplifier that are essential for proper load modulation operation of a conventional Doherty amplifier. As a result of the second and third harmonic termination, excellent improvement in power added efficiency (PAE), gain, maximum output power as well as linearity is obtained. The acquired improvements in gain, maximum output power (P_{1dB}), PAE and adjacent channel leakage ratio (ACLR) to WCDMA 2FA signal are 0.42dB, 0.33dB, 12.7%, and 5.1dB, respectively. Moreover, physical length of microstrip line is shortened fairly by DGS, therefore the whole amplifier circuit size is considerably reduced.**

Index Terms **— Doherty Amplifier, DGS, PAE, linearity.**

I. INTRODUCTION

Doherty amplifier is one of the most representative ways of PAE enhancement, and extensive researches have been done on it. The key concept of Doherty amplifier is obtaining maximum efficiency over 6dB dynamic range using load modulation [1].

The design method for optimum output load-pull operation in conventional Doherty amplifiers (CDA) has been reported in [2] by simply assuming the ideal harmonic termination of an active load-pull operation, so that a fundamental component could be only concerned for PAE. Since the sub-amplifiers in CDA are usually operating in nonlinear bias conditions, a lot of harmonic components arise. So the harmonic termination must be considered for the improvement of PAE and linearity. In addition, some previous works showed that the termination of the harmonic components plays a positive role in improving the maximum output power, PAE and linearity [3][4].

In this work, we propose a new design method for DGS Doherty amplifier (DDA) having ideal harmonic termination. At first, we explain the design and measurement of a DGS microstrip line ("DGS line"). Secondly, we show the improved output powers of the carrier and the peaking amplifier due to the DGS line. Finally, the comparison between DDA and CDA are discussed in terms of power gain, P_{1dB}, PAE and ACLR characteristic.

II. DESIGN OF A DGS DOEHRTY AMPLIFIER

A. Active Load-pull Analysis with Ideal Harmonic Termination

Fig.1 shows an active load-pull circuit considering ideal harmonic termination. Active load-pull technique is a concept that the impedance of an RF load seen by the first signal source (*Gen*1) can be modified by applying the second signal source (*Gen*2). In other words, we can control the input resistance (R_1) seen by *Gen*1 by changing currents I_1 and I_2.

When performing an active loadpull analysis, an ideal harmonic termination condition should be satisfied, since only fundamental current component is taken into consideration. Previous studies assumed a weakly nonlinear case, higher order harmonics being not considered. However, the amount of higher order harmonic components is significant due to the fact that the peaking amplifier is usually operated deeply into class C.

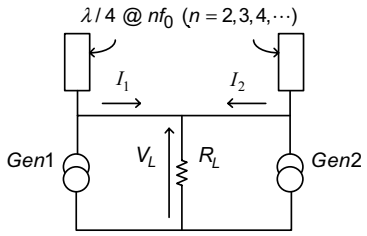


Fig. 1. Active load-pull circuit considering ideal harmonic termination.

Fig. 2 shows the block diagram of the CDA. CDA consists of carrier, peaking amplifier, λ/4 impedance transformer, offset transmission line, and input power divider. At higher output power range, both amplifiers operate and the load impedances are R_0, respectively. However, at lower output power range, only the carrier amplifier operates and peaking amplifier is in the off-state.

At this time, usually Z_{out} of the peaking amplifier is not open due to the parasitic components inside the amplifier. Therefore we need an offset transmission line (θ_{Pout}) to make Z_{out} of the peaking amplifier open at the output power combining point. Moreover, λ/4 impedance transformer with offset transmission line (θ_{Cout}) is essential for load impedance of the carrier amplifier to be $2R_0$ [5].

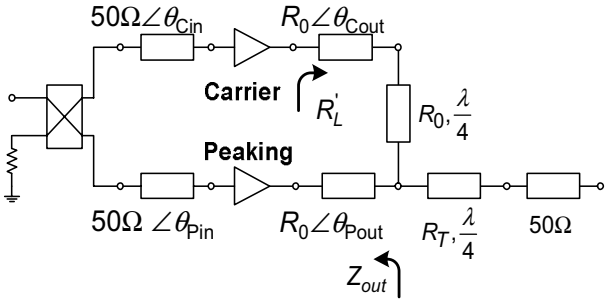


Fig. 2. Conventional Doherty amplifier.

B. DGS Low Pass Microstrip Line

We designed the DGS line using a dumbbell shaped DGS to obtain higher order harmonic termination condition [6]. The DGS line has to maintain low insertion loss and a good reflection characteristic at the fundamental frequency, since it should be placed at the output of the power amplifier.

Fig. 3 (a) shows the geometry of the proposed DGS line of which the characteristic impedance is 16Ω, implemented on the substrate with ε_r =2.2 and h=31mil (A=3.4mm,B=3.6mm, G=0.7mm, S=8mm, W=10.46mm). Fig. 3 (b) shows the electrical characteristic comparison of conventional and DGS line. Characteristic impedance 16Ω of the output microstrip line is derived from the optimum load-line of the carrier amplifier. Due to the characteristic impedance of 16Ω, additional 28.28Ω λ/4 transformers are used at the input and output of the 16Ω line for matching to the 50Ω measurement system.

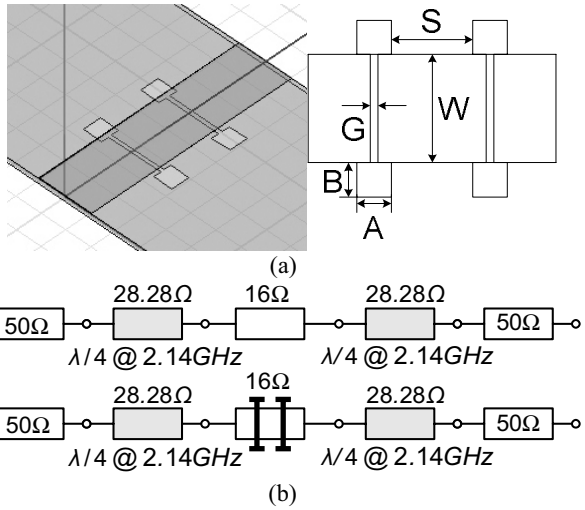


Fig. 3. (a) Geometry of the DGS line. (b) Transmission characteristic comparison between conventional and DGS line.

Fig. 4 (a) shows simulation and measurement of a DGS line. Fig.4 (b) represents transmission characteristic comparison. If 0.1dB insertion losses are excluded at the input and output λ/4 transformers, actual insertion loss of the 16Ω DGS line would be 0.13dB. It is noted that the measured suppression of the DGS line is more than 31dB at the second and third harmonic frequencies. Slow-wave effect is also shown in Fig. 4(c). The DGS line has electrical length of 89.5˚longer than that of the conventional microstrip line for the same physical length. That is why the whole circuit size can be reduced considerably.

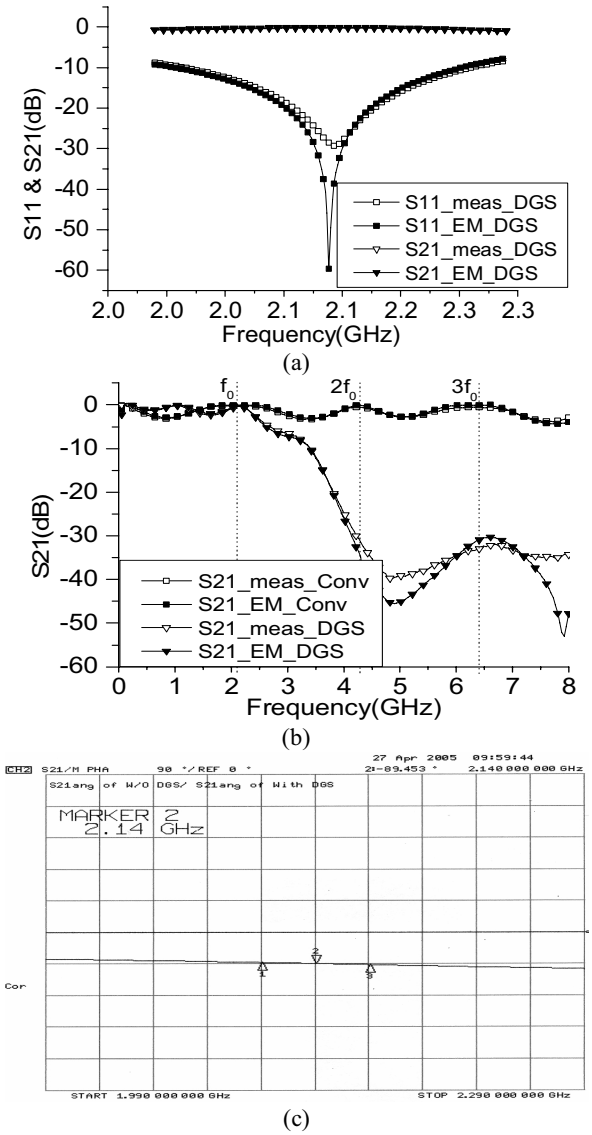


Fig. 4. (a) Simulation and measurement results of DGS line. (b) Comparison of transmission chatacteristic. (c) Comparison of electrical length.

C. DGS Doherty Amplifier

In order to verify the improved performances of a DGS Doherty amplifier, conventional and DGS Doherty amplifier is designed for IMT-2000 base-station using 4W GaAs FET device. Each of carrier amplifier and peaking amplifier has a bias condition of class A (I_{DS}=620mA) and class C (V_{GS}=-3.5V), respectively. The block diagram of the proposed DDA is shown in Fig. 5. We would call the inner part of the dashed line DGS carrier amplifier, the inner part of the solid line DGS peaking amplifier, and the whole part DGS Doherty amplifier.

The noteworthy point here is the fact that we did not insert additional transmission lines to apply DGS unit. We did apply DGS unit on the ground pattern of the λ/4 impedance inverter that is essential for proper active load-pull mechanism. At the same time, as we noted earlier, we need an offset transmission line at the output of the peaking amplifier. In other words, we applied DGS unit on the ground pattern of the output offset transmission line (θ_{Pout})of the peaking amplifier.

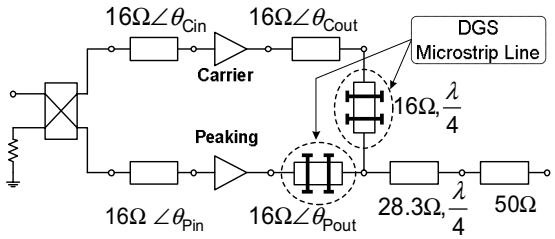
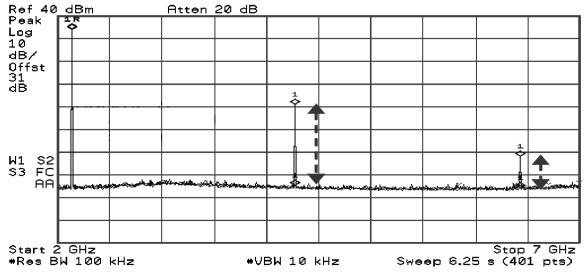


Fig. 5. Proposed DGS Doherty amplifier.

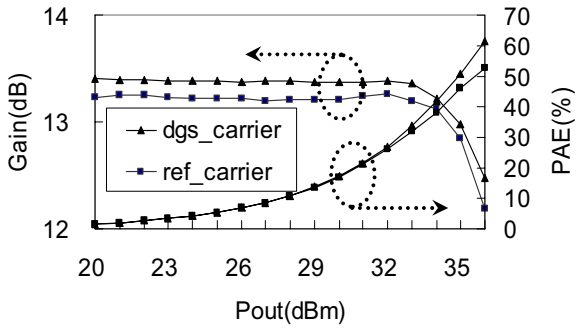
III. Implementation and Measurements

A. DGS Carrier Amplifier

Fig. 6 (a) shows the harmonic response of the conventional and the proposed DGS carrier amplifier. The second and third harmonics are suppressed about 35.62dB and 14.1dB (on the noise floor), respectively. As a result, gain and PAE improvement of the DGS carrier amplifier is shown in Fig. 6 (b) over 10dB output dynamic range. The energy of the suppressed higher order harmonics is expected to affect the fundamental signal. Gain, P_{1dB}, and PAE are increased about 0.2dB, 0.3dB and 9.1% at the maximum output power, respectively. Also, an ACLR is improved over dynamic range, especially 6dB at 29dBm as shown in Fig. 6 (c).



(a)



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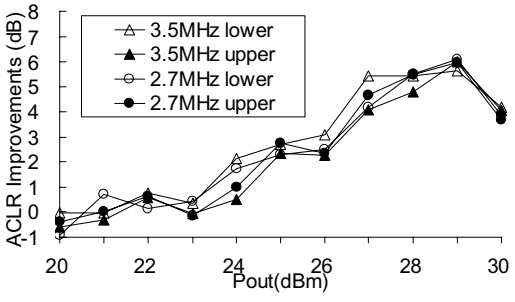
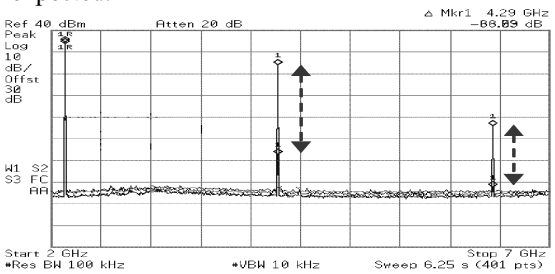


(c)

Fig. 6. DGS carrier amplifier. (a) Harmonic rejection. (b) Gain, P1dB and PAE improvement. (c) ACLR improvement for WCDMA 1FA signal.

B. DGS Peaking Amplifier

Fig. 7 (a) shows the harmonic rejection of the DGS peaking amplifier. The second and third harmonics are about 35dB and 25dB suppressed, respectively. Gain is barely changed, however the PAE at the maximum output power is 17.5% increased, as shown in Fig. 7 (b). The ACLR improvements of DGS peaking amplifier for WCDMA 1FA signal is shown at Fig. 7 (c). We obtained about 1.5dB improvement, somewhat smaller amount than expected.



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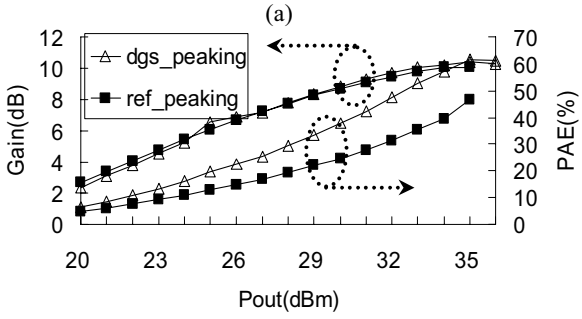

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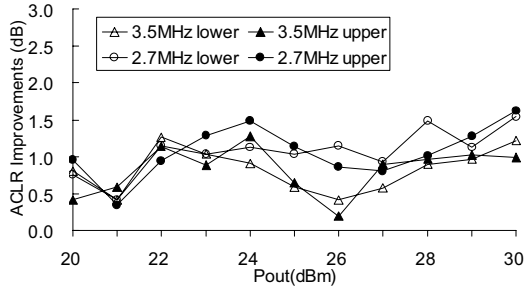


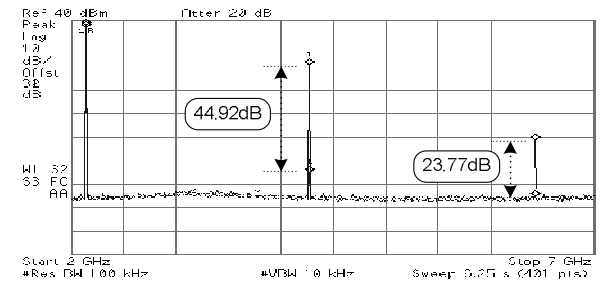
(c)

Fig. 7. DGS peaking amplifier. (a) Harmonic rejection. (b) Gain, P1dB and PAE improvement. (c) ACLR improvement for WCDMA 1FA signal.

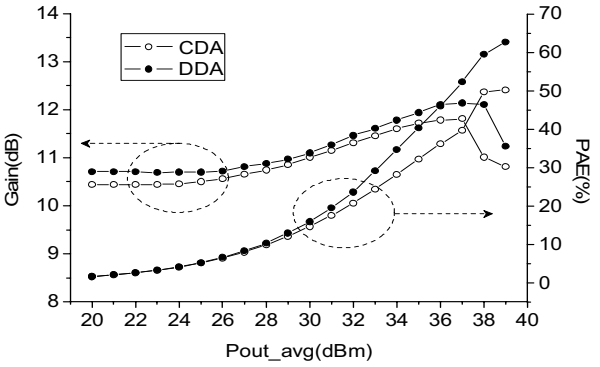
C. DGS Doherty Amplifier

The improved harmonic rejection characteristic of the DDA over the CDA is shown in Fig. 8 (a). The second and third harmonic rejections are 44.92dB and 23.77dB (on the noise floor), respectively. Higher order harmonic termination leads to increase in gain, output power and PAE.

Fig. 8 (b) shows the compared typical parameters between the CDA and DDA. Over the dynamic range, gain and P_{1dB} are increased about 0.33dB and 0.42dB, respectively. The maximum PAE improvement of the DDA over the CDA is 12.7%. Fig. 8 (c) and (d) shows the ACLR improvement and output spectrum for the WCDMA 2FA with the frequency spacing of 5MHz. We obtained normally 5dB ACLR characteristic over the output power dynamic range of 10dB. Output spectrum is shown at P_{out_avg}=28dBm.



(a)



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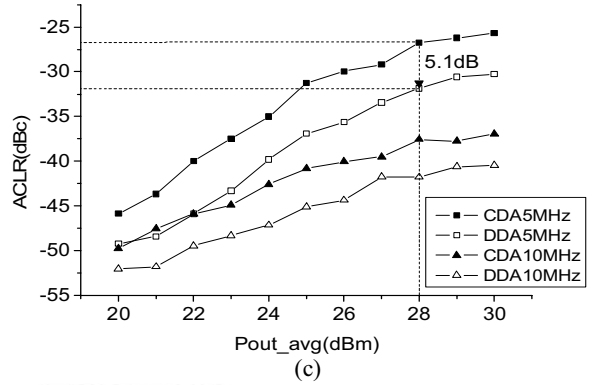

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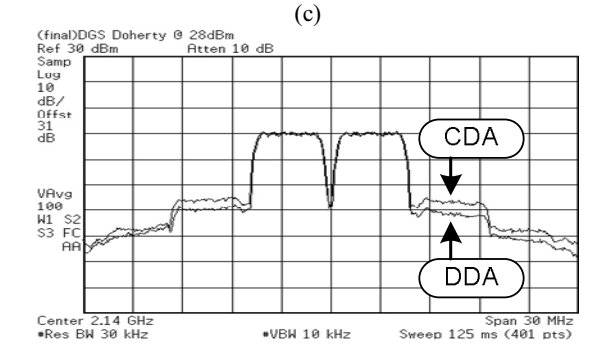

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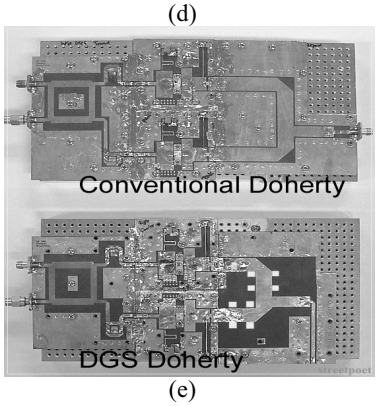

(e)

Fig. 8. DDA. (a) Harmonic rejection. (b) Gain, P_{1dB} and PAE improvement. (c) ACLR improvement for WCDMA 2FA signal. (d) Output spectrum (@Pout_avg=28Bm). (e) Comparison of the whole circuit size of CDA and DDA.

The size reduction of the implemented DDA over the CDA is shown in Fig. 8 (e). The ratios of the reduced lengths to the original ones are 71% (=69mm/96.96mm) at the carrier amplifier output, and 62% (=46.4mm/74.86mm) at the peaking amplifier output.

IV. Conclusion

In this paper, we proposed a new DGS Doherty amplifier having DGS microstrip line at the λ/4 impedance inverter of the carrier amplifier and output offset transmission line of the peaking amplifier. We could suppress higher order harmonics and reduce the circuit size effectively by the negligible insertion loss, excellent harmonic termination characteristic and slow-wave effect. As a result of harmonic termination, a considerable improvement in PAE, ACLR, gain and maximum output power have been achieved.

It is expected that the proposed design technique is well applicable to the conventional high power base-station Doherty amplifier to improve PAE, P1dB and linearity without any additional lumped elements or transmission lines, while the total circuit size is shortened at the same time.

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