Novel High-*Q* Inductor using Active Inductor Structure and Feedback Parallel Resonance Circuit

Sujin Seo, *Namsik Ryu, Heungjae Choi and Yongchae Jeong

Dept. of Information & Communication Engineering, Chonbuk National University,
664-14, Duckjin-Dong, Duckjin-Gu, Jeonju, 561-756, Korea
*XRONet Corporation, Sunae-dong 6-4, Bundang, Seongnam, Gyeonggi, 463-020, Korea

***Abstract* — This paper presents a novel high-*Q* inductor using conventional grounded active inductor and feedback parallel resonance circuit. The proposed high-*Q* inductor (HI) consists of the conventional active grounded inductor and feedback parallel resonance circuit which is composed of low-*Q* spiral inductor and capacitor. The novelty of the proposed structure is based on the increase of *Q*-factor by feeding parallel resonance circuit into gyrator structure. The high-*Q* inductor is fabricated by 0.18um Hynix CMOS technology. The fabricated inductor shows inductance of above 45 nH and *Q*-factor of over 250 around 5GHz.**

***Index Terms* — Active inductor, feedback parallel resonance circuit, *Q*-factor, spiral inductor.**

I. Introduction

One important issue related to the standard CMOS technology is low-resistivity silicon substrate that results in low *Q*-factor for the passive spiral inductor. Thus, in spite of the inherent drawbacks of the active inductor such as noise, linearity and power consumption, it have been studied and applied to many RF circuit designs because of its several advantages of low insertion loss, small size, and tunability of inductance.

The conventional grounded active inductor (GAI) is realized with basic gyrator-C structure [1]. The gyrator-C consists of two transistors, and generates inductive reactance from parasitic capacitance of those transistors. But the conventional GAI has limitation to increase the *Q*-factor and frequency tuning range with high *Q*-factor.

There have been some works by adding arbitrary circuit into the conventional GAI to enhance *Q*-factor [1][2]. Recently, GAI with cascode structure to enhance *Q*-factor was proposed in [3]. However, as the CMOS process becomes smaller with the development of CMOS process technology, it has a drawback of consuming much DC power by voltage headroom.

In this paper, we analyzed the conventional GAI mathematically by using RF small signal model of a transistor. Based on this analysis result, we proposed the optimum design method of tunable inductor with high *Q*-factor by feeding feedback parallel resonance circuit into the conventional GAI structure.

II. Conventional Grounded Active Inductor

Fig. 1 shows the conventional GAI and its equivalent circuit. From the equivalent circuit, we can derive current equations (i_1 and i_2) for each port, respectively. Input impedance Z_{in} seen from port 1 is obtained by the *Y*-parameter which derived from the current equations of i_1 and i_2. The input impedance is represented in Eq. (1) where $A=C_T(C_{gs1}+C_{gd2})+C_{gs1}C_{gd1}$, $B=C_T(1/r_{o1}+1/r_{o2}+g_{m1})+g_{m2}C_{gd2}+C_{gd1}/r_{o2}+C_{gs1}/r_{o1}$, $C=g_{m2}/r_{o1}+1/r_{o1}r_{o2}+g_{m1}g_{m2}$ and $C_T=C_{gs2}+C_{gd1}$.

$$Z_{\text{in}} = \frac{1/r_{o1} + s\left(C_T + C_{gd2}\right)}{A \cdot s^2 + B \cdot s + C} \tag{1}$$

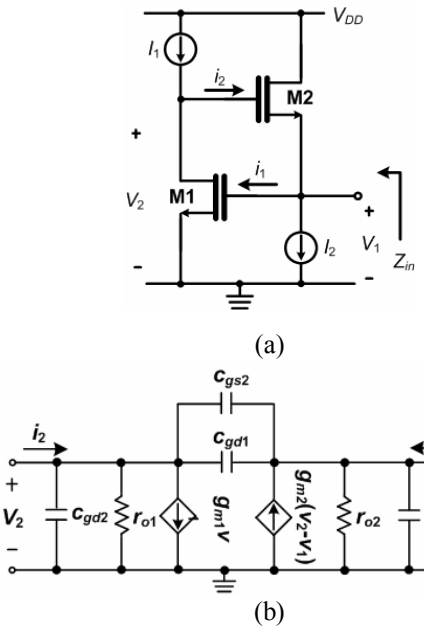


Fig. 1. The conventional (a) schematic of GAI, (b) two port equivalent circuit of GAI.

If we adopt an assumption, $s(C_T+C_{gd2}) > g_m >> 1/r_o$, Eq. (1) can be simplified the input impedance of GAI as Eq. (2). From Eq. (2), we can conclude intuitively that the inductance and Q-factor of the conventional GAI is determined by the typical parameters of transistor M1 and M2.

$$Z_{\text{in}} = \frac{s\left(C_T + C_{gd2}\right)}{g_{m1}g_{m2}} = sL \tag{2}$$

However, we cannot say that those parameters have an effect on Q-factor from Eq. (2). So, we can observe the variation of Q-factor through frequency by varying typical parameters in Eq. (3) from mathematical simulation.

$$Q = \frac{\omega L}{R} = \frac{\omega\left[\left(C_T + C_{ds2}\right)\left(C - \omega^2 A\right) - \left(B / r_{o1}\right)\right]}{\omega^2 B\left(C_T + C_{ds2}\right) + \left[\left(C - \omega^2 A\right) / r_{o1}\right]} \tag{3}$$

The simulation results are shown in Fig. 2. Fig. 2(a) shows that Q-factor can be enhanced by increasing r_o of transistor M1. Fig. 2(b) shows that Q-factor is proportional to g_{m1}, although the inductance value is inverse-proportional to g_{m1} as it is represented in Eq. (2). Fig. 2(c) and Fig. 2(d) shows that Q-factor can be decreased by increasing C_{gs2}. We can find that Q-factor is changed dynamically by the effect of parasitic capacitance of M2 at high frequency [3][5].

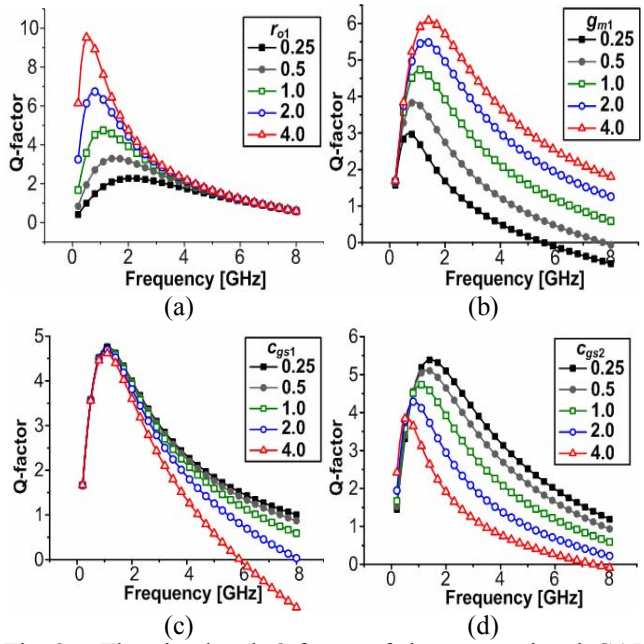


Fig. 2. The simulated Q-factor of the conventional GAI for (a) r_{o1} variation, (b) g_{m1} variation, (c) C_{gs1} variation and (d) C_{gs2} variation.

III. Proposed High-Q Inductor Design

A. Prototype inductor (PI) using feedback spiral inductor.

In this paper, we proposed a prototype inductor (PI) to improve Q-factor by adding the feedback spiral inductor (L_f) between the source of M2 and the gate of M1 of the conventional GAI. From Fig. 2(d), we can see that Q-factor is decreased by parasitic capacitance. If parasitic capacitance is reduced by adding the spiral inductor to the source of M2, we can compensate the degradation of Q-factor by parasitic capacitance. The spiral inductor can occupy an additional space, but we have a high Q-factor using only small inductance as a compensation for parasitic capacitance of M2 transistor in the conventional GAI. Moreover, a parasitic resistance of the spiral inductor is useful the improvement of Q-factor due to increasing inductance of GAI.

Fig. 3 shows PI using feedback spiral inductor and its small signal equivalent circuit. The spiral inductor represented by r_L and L. Fig. 4 is simulation results of the proposed PI according to increase L_f. When we used L_f of 2.3 nH, we can obtain very high Q-factor through frequency range from 4.3 GHz to 5.5 GHz. This result shows the possibility that PI can be realized with Q-factor above 50.

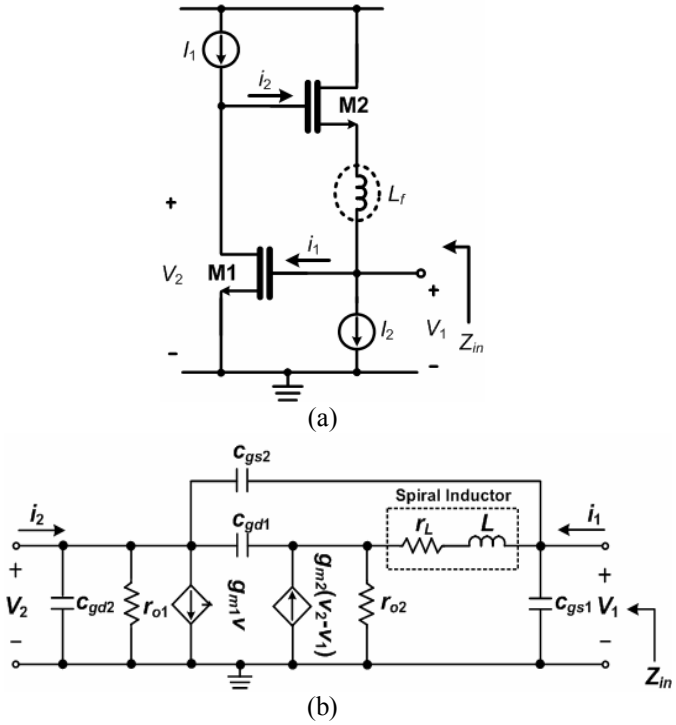


Fig. 3. Prototype inductor (PI) using feedback spiral inductor. (a) Schematic and (b) two port equivalent circuit.

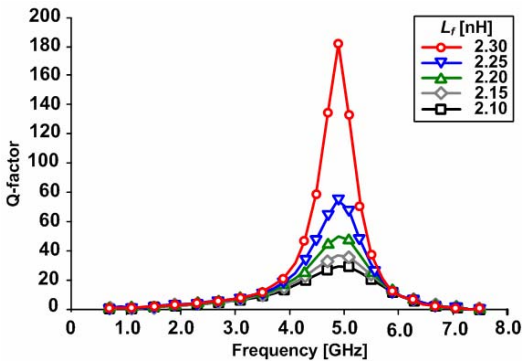
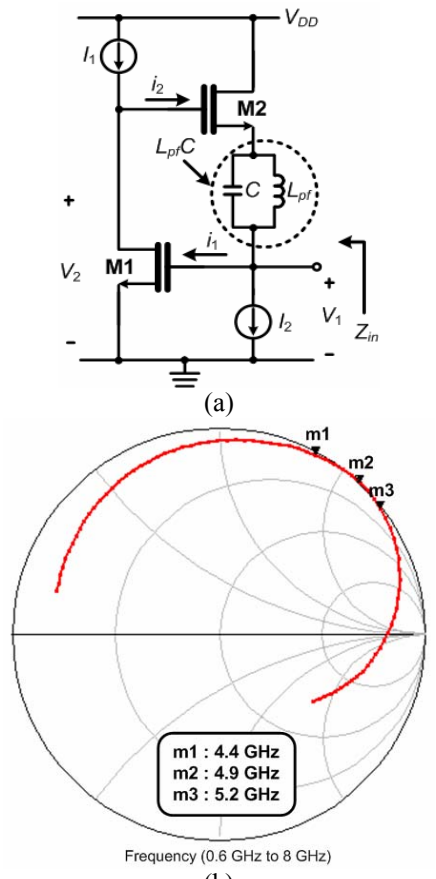


Fig. 4. Simulation result of PI by increasing the inductance of feedback inductor (L_f).



(a)

(b)

Fig. 5. High-Q inductor using feedback LC resonance circuit (a) Schematic and (b) smith chart. (C=0.1 pF, L_{pf} < L_f).

B. High-Q inductor using feedback LC resonance circuit.

The spiral inductor of over 2.3 nH occupies an extensive space and causes the size problem. To overcome this problem, we used LC parallel resonance circuit ($L_{pf}C$) instead of spiral inductor (L_f) as shown in Fig. 5.

The spiral inductor (L_{pf}) of the feedback resonance circuit is smaller than L_f of the PI. Fig. 5(a) presents a high inductor (HI) using parallel feedback LC resonance circuit. The impedance of parallel LC resonance circuit ($L_{pf}C$) can be explained and the equivalent inductance explained with Eq. (4). From Eq. (4), we will design resonator to exhibit large inductance value by small spiral inductor.

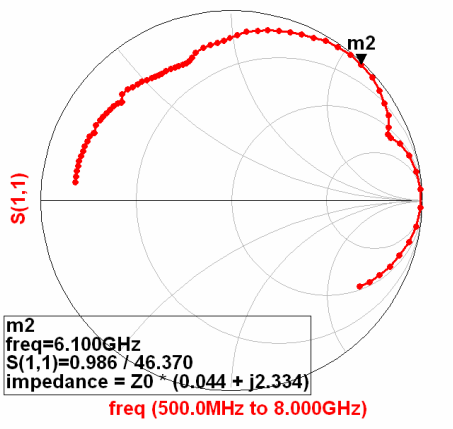
$$Z_{resonance} = sL_{resonance} = \frac{j\omega L_{pf}}{1-\omega^2 L_{pf} C_v} \tag{4}$$

Fig. 5 shows a schematic of HI and a simulation result. We used inductor (L_{pf}) of small size than L_f and capacitor with 0.1pF. The spiral inductor value used EM-simulation data. Thus we are obtained simulation result with high Q-factor in wide band, about 1GHz, as shown Fig. 5(b).

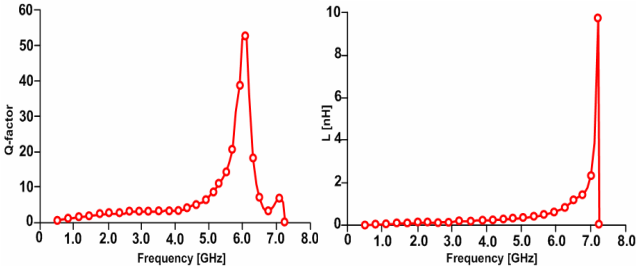
IV. Experimental Result of Tunable Inductor

A. Measurement result of PI.

To show the validity of the proposed PI and HI, we have fabricated by the standard 0.18 um Hynix CMOS process. Fig. 6 shows the measurement result of the fabricated PI. The PI power consumption is 12 mW for 1.8 V supply voltage. Also we have obtained that PI has Q-factor above 50 at 6 GHz, and the maximum inductance is over 18 nH. This result can be controlled by supplying the bias current into PI. Consequently, we can obtain higher Q-factor and inductance than the conventional GAI configuration. Actually, realization of the accurate PI using the feedback spiral inductor is difficult due to the additional parasitic components of the spiral inductor. Thus, we have analyzed that the maximum Q-factor frequency of the fabricated PI is deviated from the simulation result due to the additional parasitic components of the spiral inductor.



(a)



(b) (c)

Fig. 6. The measured (a) smith chart (b) *Q*-factor and (c) inductance of the fabricated PI.

B. Measurement result of HI

Fig. 7 is layout of the HI. The layout size of HI is 700 um × 700 um. Fig. 8 is the measurement result of the fabricated HI using feedback LC parallel resonator. HI power consumption is 12 mW for 1.8V supply voltage, the same value as PI. From Fig. 7, we know that HI has *Q*-factor of 250 around 5 GHz, and the maximum inductance is 45 nH. Through this result, we know that HI is obtained high *Q*-factor using smaller size spiral inductor than PI ($L_f > L_{pf}$).

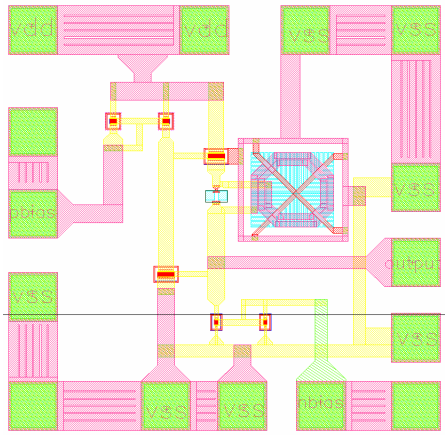
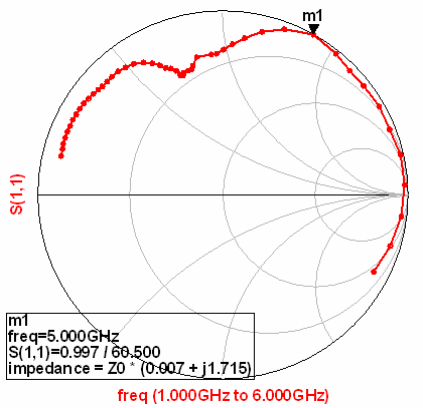
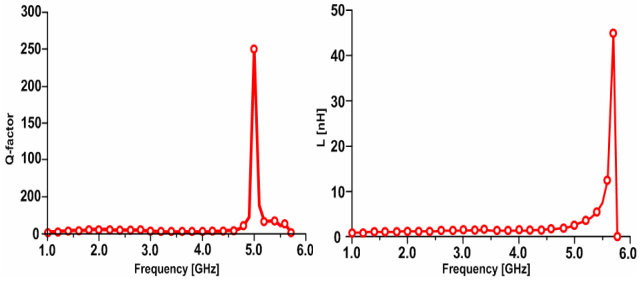


Fig. 7 Layout of high-*Q* inductor



(a)



(b) (c)

Fig. 8. The measured (a) smith chart (b) *Q*-factor and (c) inductance of the fabricated TI.

V. Conclusion

In this paper, we presented a novel high-*Q* inductor using active inductor structure and feedback parallel resonance circuit. The fabricated PI has *Q*-factor above 50 at 6 GHz, and the maximum inductance about 100 nH at 7 GHz, also HI has *Q*-factor of 250 around 5 GHz, and maximum inductance is 45 nH. In this result, the novel high-*Q* inductor provides high *Q*-factor and large inductance using the small value spiral inductor.

In this paper, we can achieve excellent result with the proposed HI. However, the proposed HI has two a drawbacks. Those problems are large power consumption and narrow frequency range of high *Q*-factor. In the near future, we will work out a way to solve those problems. We expect the proposed novel high-*Q* inductor can be applied to various circuits which require high *Q*-factor at high frequency.

References

[1] R. Mukhopadhyay, "Reconfigurable RFICs for Frequency-agile VCOs in Si-based Technology for Multi-standard Applications," *IEEE MTT-S International Microwave Symp. Diq.*, vol. 3, pp. 1489-1492, June 2004.

[2] C. C. Hsiao, "Improved Quality-Factor of 0.18-μm CMOS Active Inductor by a Feedback Resistance Design," *IEEE Microwave and Wireless Components Letters*, vol. 12, no. 12, pp. 467-469, Dec. 2002.

[3] A. Thanacbayanont and A. Payne, "VHF CMOS Integrated Active Inductor," *Electronic Letters*, vol. 32, no. 11, pp. 999-1000, May 1996.

[4] U. Yodprasit, and J. Ngarmnil, "Q-Enhancing Technique for RF CMOS Active Inductor," *ISCAS 2000 IEEE Int. Sym. on Circuits and Systems*, vol. 5, pp. 589-592, May 2000.

[5] H. Hayashi, M. Muraguchi, "A High-Q Broad-Band Active Inductor and Its Application to a Low-Loss Analog Phase Shifter," *IEEE Transactions on Microwave theory and techniques*, vol. 44, no 12, pp. 2369-2314, Dec. 1996.