High Efficiency Distributed Amplifier Using Optimum Transmission Line

Sigyun Jeong^{#1}, Heungjae Choi^{#2}, Yongchae Jeong^{#3}, J. Stevenson Kenney^{*4}, Chuldong Kim^{**5}

[#]Dept. of Information & Communication Engineering, Chonbuk National University, 664-14, Duckjin-Dong, Duckjin-Gu, Jeonju, 561-756, Republic of Korea

¹sg333.jeong@chonbuk.ac.kr

²streetpoet@chonbuk.ac.kr, ³ycjeong@chonbuk.ac.kr

* School of ECE, Georgia Institute of Technology, USA

⁴jskenney@ece.gatech.edu

** Sewon Teletech, Anyang, Republic of Korea

⁵chuldkim@sewon-teletech.co.kr

Abstract— In this paper, we performed numerical analysis on reversed current of distributed amplifier (DA) based on transmission line theory and proposed optimum transmission line (OTL) to cancel reversed currents. This OTL has improved electrical performances of DA. The distributed amplifier using optimum transmission line (DAOTL) has been implemented with pHEMT transistor. Due to high capacitance of pHEMT, cutoff frequency is decided to 3.6GHz. As a result of measurement, we could obtain maximum gain of 14.5dB and minimum gain of 12.8dB inner operation band. Moreover, we could PAE of 25.6% which is higher about 7.6% than the conventional DA (CDA) at 3GHz. The output power was obtained 10.9dBm which is higher about 1.7dB than the conventional at 3GHz.

I. INTRODUCTION

Recently, demand of communication system in microwave and millimeter wave bands is increasing according to an amount of information increases. Specially, the study about equipment which can be used in multi-band or broadband has been performed actively.

DA is known for most suitable topology in design of broadband amplifier. Up to now, there were many efforts to extend the cutoff frequency and implement with several type monolithic microwave integrated circuits [1]-[3]. But the conventional distributed amplifier (CDA) has low power added efficiency (PAE) characteristic which is typically less about 10% in high frequency, especially around cutoff frequency[4]-[6]. Even though there were many efforts to improve PAE, low efficiency characteristic which is generated by reversed current near the cutoff frequency is yet to be solved [7][8].

In this paper, we have analyzed reversed currents that are fed-backed to isolation resistor and proposed new topology to cancel reversed current each other. The cancellation of reversed current could be solved theoretically by evaluating the optimum electrical transmission line length. The proposed DAOTL provides flatter gain, higher efficiency and more output power than CDA near cutoff frequency.

II. DA THEORY USING TRANSMISSION LINE

The basic configuration of a microwave DA is shown in Fig. 1. The identical *N*-stage FETs are connected by transmission lines having characteristic impedance of Z_d and Z_g and length of l_d and l_g , respectively. And we assumed that the gate and drain ports are isolated except for the coupling through the transconductance (g_m) . Hence we can analyze by dividing into drain and gate stage, as shown Fig. 2(a) and (b).



Fig. 1 Basic schematic of DA using transmission line.



Fig. 2 The equivalent circuit (a) gate stage, (b) drain stage of DA.



Fig. 3 (a) The equivalent circuit of single unit cell of the gate line, (b) The equivalent circuit of single unit cell of the drain line.

Fig. 3(a) and 3(b) show the equivalent circuits for a single transistor unit cell from the gate and drain lines, respectively. In Fig. 3, L_g , L_d , C_g and C_d are inductance and capacitance per unit length of transmission line. And the parasitic components of FET are regarded as a part of transmission line. Therefore, characteristic impedances of gate line and drain line can be written as

$$Z_{g,d} = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{L_{g,d}}{C_{g,d} + C_{gs,ds} / l_{g,d}}}$$
(1)

And the propagation constants of gate line and drain lines can be written as

$$\gamma_g = \alpha_g + j\beta_g \approx \frac{\omega^2 R_i C_{gs}^2 Z_g}{2l_g} + j\omega \sqrt{L_g (C_g + C_{gs}/l_g)} \quad (2-a)$$

$$\gamma_d = \alpha_d + j\beta_d \approx \frac{Z_d}{2R_{ds}l_d} + j\omega\sqrt{L_d(C_d + C_{ds}/l_d)}$$
(2-b)

For an incident input voltage (V_i), the voltage on the C_{gs} of *n*-th FET can be written as

$$V_{cn} = V_i e^{-(n-1)\gamma_g l_g} \left(\frac{1}{1 + j\omega R_i C_{gs}} \right)$$
(3)

The final output current on drain line can be explained as $-1/2I_{dn}e^{\pm\gamma dz}$ by each transconductance in each direction. Therefore, total output current at the *N*-th output terminal can be written as

$$i_{o}^{+} = -\frac{g_{m}V_{i}}{2}e^{-N\gamma_{d}l_{d}}e^{\gamma_{g}l_{g}}\sum_{n=1}^{N}e^{-n(\gamma_{g}l_{g}-\gamma_{d}l_{d})}$$
(4)

The total output current at the drain line is added in phase only when $\beta_g l_g = \beta_d l_d$. So, (4) is simplified as (5).

$$i_{o}^{+} = -\frac{g_{m}V_{i}}{2} \frac{e^{N\gamma_{g}l_{g}} - e^{N\gamma_{d}l_{d}}}{e^{\gamma_{g}l_{g}} - e^{\gamma_{d}l_{d}}}$$
(5)

III. THEORETICAL ANALYSIS OF DAOTL

In the section II, we have analyzed the current toward output port by theory of traveling wave. However, there are also reversed currents by isolation port load resistor, R_D, existing in another direction of output port. And in order to obtain the higher efficiency, it is necessary to find the optimum transmission line length for canceling reversed currents. Fig. 4 shows reversed currents that are absorbed by R_D in the DA. The reversed currents flowing the n-th transistor toward R_D, i_n^- , are represented numerically in (6).



Fig. 4 The reversed currents by $R_{\rm D}$ in N-stage DA.

$$i_{n}^{-} = -\frac{1}{2} g_{m} V_{i} e^{-\gamma_{g} (n-\frac{1}{2})l_{g}} e^{-\gamma_{d} (n-\frac{1}{2})l_{d}}$$
$$= -\frac{g_{m} V_{i}}{2} e^{(\gamma_{g} l_{g} + \gamma_{d} l_{d})/2} e^{-n(\gamma_{g} l_{g} + \gamma_{d} l_{d})}, \text{ for } n=1,2,\cdots N$$
(6)

Transmission line of gate and drain leads the phase of reversed currents, as shown (6). And if propagation constant and line length of gate and drain line are equal each other $(\gamma_d l_d = \gamma_g l_g = \gamma l)$, (6) can be simplified as (7).

$$i_n^- = -\frac{g_m V_i}{2} e^{\gamma l(1-2n)}, \text{ for } n=1,2,3, \dots, N$$
(7)

Consequently, all of inverse current, i_0 , can be written as

$$i_{o}^{-} = i_{1}^{-} + i_{2}^{-} + i_{3}^{-} + \dots + i_{N}^{-} = -\frac{g_{m}V_{i}}{2} \sum_{n=1}^{N} e^{\gamma l(1-2n)}$$
(8)

If transmission line is lossless, (8) can be rewritten, as (9).

$$i_{o}^{-} = -\frac{g_{m}V_{i}}{2} \sum_{n=1}^{N} e^{j\beta l(1-2n)}$$
(9)

Fig. 5 shows phase deviation for cancellation of reversed currents. In case of 2-stage, the reversed currents can be canceled when phase deviation between i_1 and i_2 is π . And in case of *N*-stage, the cancellation condition is that the phase deviation between each reversed current has $2\pi/N$. Therefore, gate and drain line length must be set as (10) to satisfy cancellation condition of *N*-stage.

$$-\beta l - (-3\beta l) = \frac{2\pi}{N} \qquad \therefore \beta l = \frac{\pi}{N}$$
(10)

By substitution (2) in (10), we can find transmission line length for cancellation of the reversed currents, as (11).

$$l = \frac{\pi}{N} \cdot \frac{1}{\omega \sqrt{L_{g,d} (C_{g,d} + C_{gs,ds} / l_{g,d})}}$$
(11)

With this, we can eliminate absorbed power by RD of DA.



Fig. 5 The phase deviation for cancellation condition (a)2-stage, (b)3-stage, (c)4-stage, (d)N-stage

IV. FABRICATION AND MEASUREMENT OF DAOTL

To show validity of the proposed DAOTL, we simulated and implemented 4-stage DA by using pHEMT ATF-36077 on Teflon PCB. The circuit simulation was achieved using ADS of Agilent. Since input and output parasitic capacitance of transistor was fixed, the equivalent inductance of transmission line was fixed by (1) to obtain 50 Ω matching of input stage and output stage without matching network. Cutoff frequency (f_{3dB}) of the distributed amplifier is mainly determined by the cutoff frequencies of the artificial lines, which are given by [5]

$$f_{3dB} = \frac{1}{\pi \sqrt{L_{g,d} (C_{g,d} + C_{gs,ds} / l_g)}}$$
(12)

By (12), the designed DAOTL has operation frequency band of 400MHz~3.6GHz. And we select the frequency for cancellation of the reversed currents as 3.0GHz. So we designed that electrical length of DAOTL has 45° at 3.0GHz, otherwise that of CDA has typically 28° at 3.0GHz. In order to implement wanted inductance, characteristic impedance of transmission line should be 98 Ω in case of DAOTL. Otherwise, that should be 110 Ω in case of CDA. Fig. 6 shows simulation schematic of designed DA and Fig. 7 shows gain simulation results of CDA and DAOTL.

The fabricated DAOTL and CDA were biased through gate and drain line by means of external Bias-T. The bias point was selected at V_{ds} =1.5V, and V_{gs} =-0.35V corresponding to Id= 30mA.



Fig. 6 Simulation schematic of the designed DA.



Fig. 7 Simulation result of CDA and DAOTL.



Fig. 8 Gain measurement result of CDA and DAOTL.

The measured gain characteristics of DAOTL and CDA are shown in Fig. 8. In the operation band, the gain ripple characteristics of DAOTL and CDA were 1.8dB and 1.6dB, respectively. As like simulation result, the gain of DAOTL is higher than that of CDA in operating band and especially around 3GHz. Fig. 9 shows 1dB compression point (Pout) and PAE in the operating frequency. As like gain characteristic, those of DAOTL are better than CDA in the operating band.

The comparison of the measured results between of CDA and DAOTL is summarized in table I. Fig. 10 shows the fabricated DAOTL board.



Fig. 9 Measurement result (a) Pout of DAOTL and CDA, (b) PAE of DAOTL and CDA.

TABLE I COMPARISON OF CDA AND DAOTL

	CDA	DAOTL
Gain[dB]	12.1~13.7	12.7~14.5
Gain ripple[dB]	1.6	1.8
Minimum Pout[dBm]	8	8.2
Maximum Pout[dBm]	9.2	10.9
Minimum PAE[%]	14 (@2.2GHz)	14 (@1GHz)
Maximum PAE[%]	18 (@2.2GHz)	25.6 (@3GHz)



Fig. 10 The fabricated DAOTL. (57mm X 32mm)

V. CONCLUSIONS

CDA has generally low PAE characteristic near the cutoff frequency due to reversed current. In this paper, we presented the optimum transmission line length to cancel the reversed currents in isolation port. We simulated and fabricated new DA adopting the optimum transmission line length to provide high efficiency in the operating frequency band. The simulated and measurement results show better electrical performances than the conventional. Even though we present new DAOTL with discrete devices at now, we expect that the proposed DAOTL can be adopted RFIC and MMIC design so that the more broadband and high efficient DA would be obtained.

ACKNOWLEDGMENT

This work is supported by the second stage of Brain Korea 21 Project.

References

- B.M. Ballwebber, R. Gupta, D.J. Allstot, "A Fully integrated 0.5-5.5-GHz CMOS distributed Amplifier", *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 231-239, Feb. 2000.
- [2] J.B. Beyer, S.N. Prasad, R.C. Becker, J.E. Nordman, G.K. Hohenwarter, "MESFET Distributed Amplifier Design Guidelines", *IEEE Trans. on Microwave Theory Tech.*, vol. 32, no. 3, pp. 268-275, Mar. 1984.
- [3] R.C. Liu, K.L. Deng, and H. Wang, "A 0.6~22GHz broadband CMOS distributed amplifier," *IEEE Radio Frequency Integrated Circuits Symposium Digest*, pp. 103-106, Jun. 2003.
- [4] B. Karl et al., "On Theory and Performance of Solid-State Microwave Distributed Amplifiers" *IEEE Trans. on Microwave Theory Tech.*, vol. MTT-31, pp. 447-456, Jun. 1983.
- [5] David M. Pozar, *Microwave engineering*, Second Edition, John Wiley & Sons, N.Y., 1998.
- [6] K. B. Niclas, "On design and performance of lossy match GaAs MESFET amplifiers," *IEEE Trans. on Microwave Theory Tech.*, vol. MTT-30, pp. 1900-1907, Nov. 1982.
- [7] C.-C. Yen and H. -R. Chuang, "0.25um 20-dBm 2.4GHz CMOS power amplifier with an integrated diode linearizer.", *IEEE Microwave* and Guided Wave Letter, vol. 13, no. 11, pp. 1927-1937, Nov. 2004.
- [8] T. W, Kim, B. Kim, and K. Lee, "Highly linear receiver front-end adopting MOSFET transconductance linearization by multiple gated transistors," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 223-229, Jan. 2004.