A New DGS Unequal Power Divider

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***Abstract* — An unequal Wilkinson power divider having rectangular-shaped defected ground structure (DGS) is proposed. DGS microstrip line adopted for the divider is composed of double-layer substrate which removes the ground problem of the previous DGS structures in packaging. The first layer includes DGS on the bottom ground plane. The second substrate of which top metal plane has been removed is attached to the bottom plane of the first layer. At first, a conventional DGS unequal Wilkinsion power divider is designed according to the previous method on the first layer, and the second substrate is attached. The proposed DGS with double-layer substrate is described in detail and applied to 1:4 unequal dividers as an application example. The measured unequal Wilkinson power divider has an excellent agreement between prediction and measurement.**

***Index Terms* — unequal divider, Wilkinson power divider, defected ground structure, DGS.**

I. INTRODUCTION

Wilkinson power divider is one of the most widely used high frequency components since it has been introduced for the first time in [1]. The standard 2-way Wilkinson divider has the equal power dividing ratio, and can be used as a power combiner.

However, if N≥2 in 1:N unequal dividing ratio, a transmission line having very high characteristic impedance is required [2]. For instances, 132Ω and 158Ω transmission lines are required for N=3 and N=4, respectively. It is a serious problem that the generally accepted impedance limitation to realize is around 100Ω ~ 120Ω even though it depends on the substrate [3].

Defected ground structure (DGS) is one of good solution to solve this problem and design unequal Wilkinson power divider with highly unequal ratios [4,5]. DGS patterns give the increased equivalent inductance (L) and produce transmission lines having with high impedance [4-6].

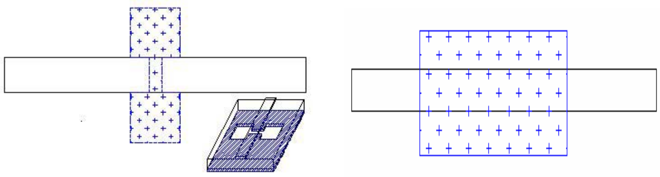
The advantages of DGS described in the previous research are; 1) It is easily performed to extract the equivalent circuit model [7], 2) It is well applied to RF/microwave circuits to reduce the size or improve performances [8], 3) DGS raises the realizable upper limit of characteristic impedance of microstrip line up to around 200Ω [4-6].

However there is a drawback, in the structure of DGS, that DGS patterns directly contact the ground surface when a DSG circuit is inserted into metal housing. If DGS pattern, in other words, the bottom plane of microstrip line having DGS patterns meets the bottom surface of metal housing, the advantageous effects of DGS disappear.

In this paper, a DGS structure with double-layer substrate is described and applied to design a 1:4 unequal Wilkinson power divider. Therefore, the goal to remove the ground problem of DGS in packaging is removed. The structure of DGS line, design of the 1:4 unequal, predicted and measured data of the unequal divider will be discussed in detail.

II. DGS LINE FOR REMOVING GROUND PROBLEM

Fig. 1 shows examples of previous DGS patterns and microstrip line. DGS patterns are realized on the bottom ground plane. Although a dumb-bell and rectangular shaped DGS are illustrated in Fig. 1, there exist many other DGS geometries such as meander, spiral, circular, triangle and so on [5,6,9]. Due to the DGS, the equivalent inductance highly increases, and consequently the characteristic line impedance jumps to high value.



(a) (b)

Fig. 1 DGS patterns on the ground plane of microstrip line (a) dumb-bell shape (b) rectangular shape

However, it has also a critical problem that it can not be inserted into metal housing/packaging. If the bottom plane contacts to the metal housing, the advantages of DGS disappear and it becomes just a standard microstrip line. It is definite that the bottom plane of DGS microstrip line should be separated from the metal housing in order to keep the advantages of DGS.

Fig. 2 shows the side view of double-layer substrate for DGS to remove the direct contact between DGS and metal housing. As has been described, conventional DGS has been realized on the ground bottom plane of the first substrate. However in this paper, the second substrate is attached to the first substrate so that DGS can not contact with the metal package directly. Area "A" in Fig. 2(a) should include DGS pattern completely. The bottom planes of the first and second

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substrates are connected through a number of via-holes in order for them to be the ground plane. The upper metal plane of the second substrate may be removed totally as shown in Fig. 2(b). The thickness of the second substrate should be as thin as possible.

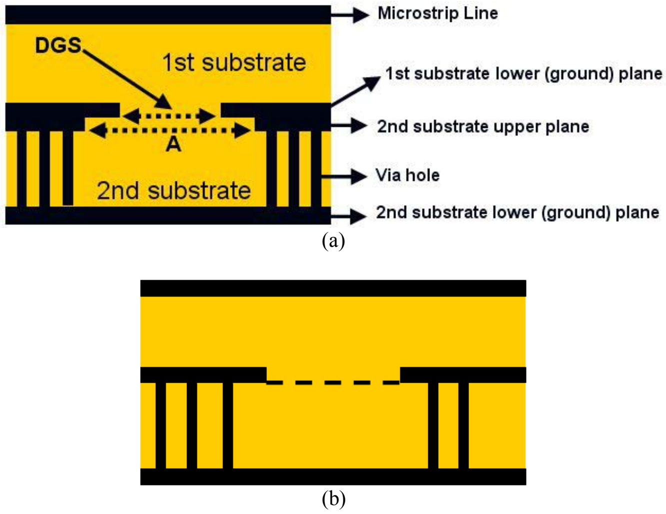

Fig. 2 Double-layer substrate for DGS not to contact metal housing directly. The upper metal plane of the second substrate remains in (a), while it has been removed in (b).

Fig. 3 shows the microstrip line having simple rectangular-shaped DGS on the bottom plane of the first substrate. W1 and W2 represent dimensions of DGS. WM is the width of the microstrip line on top plane of the first substrate.

When a rectangular-shaped DGS is realized on the ground plane of the first substrate, the effectively added inductance increases dominantly while the effective capacitance is extremely small. As the result, a very high line impedance value is obtained.

When the dielectric constant and thickness of the first substrate are 2.2 and 31mils, respectively, and, for convenience, the same substrate is attached as the second layer, the electromagnetically calculated S-parameter of the DGS line is presented in Fig. 4. The dimensions of W1, W2, and WM are 30mm, 5mm, and 0.26mm, respectively. It is noted that the calculated S11 is -1.74dB, which corresponds to 158Ω microstrip line.

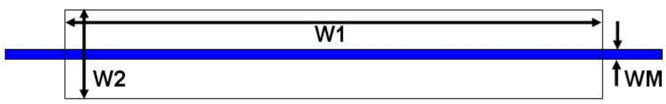

Fig. 3 Microstrip line with double-layer substrate and rectangular DGS. The second substrate is attached to the first layer even though it is not shown in thi s figure.

Fig. 5 shows the simplified transmission line model to determine the characteristic impedance (Z_{DGS}) of DGS line when port impedance is Zo. When θ=π/2 at center frequency (Fo), the magnitude of the reflection coefficient (Γ) is maximum, and it can be calculated from S_{11} by eq. (1). Once |Γ| is known, Z_{in} is calculated by eq. (2). Finally, Z_{DGS} is calculated from eq. (3). For example, S_{11} is -1.74dB in Fig. 4, and the calculated line impedance of DGS line shown in Fig. 3 is the 158Ω microstrip line.

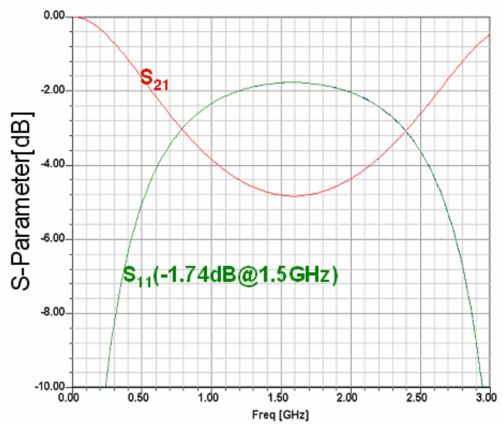

Fig. 4 Electromagnetically calculated S-parameter of the DGS line shown in Fig. 3

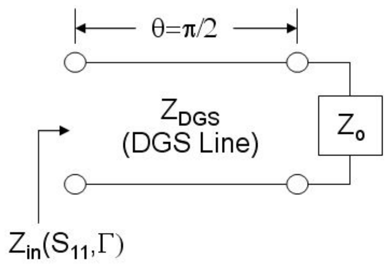

Fig. 5 Simplified model to determine the characteristic impedance (Z_3) of DGS line

$$|\Gamma| = 10^{\left(\frac{S11[dB]}{20}\right)} \tag{1}$$

$$Z_{in} = Z_o \frac{1+|\Gamma|}{1-|\Gamma|} \tag{2}$$

$$Z_{DGS} = \sqrt{Z_{in} Z_o} = Z_o \sqrt{\frac{1+|\Gamma|}{1-|\Gamma|}} \tag{3}$$

III. Unequal Wilkinson Divider using the Proposed DGS Structure

Fig. 6 shows the schematic of 2-way unequal Wilkinson power dividers. If the dividing ratio is 1:N and N≥2, Z_3 should be a very high impedance. Sometimes, for microstrip line case, it is too high to realize practically because the general limitation falls on 100Ω ~ 120Ω. When N is equal to 4, a 158Ω microstrip line should be provided. In the previous work [4], it was impossible to put the 1:4 unequal divider having DGS into the metal package because of ground problem of DGS.

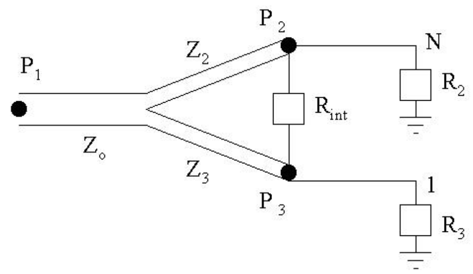

Fig. 6 Topology of 1:N unequal Wilkinson power divider. Rint is the isolation resistor, and R2 and R3 are termination impedance.

Fig. 7 shows layouts of the 1:4 unequal power divider with simple rectangular DGS and double-layer substrate. R2 and R3 in Fig. 6 have been transformed to 50Ω for practical measurement. Even though the exact R_{int} should be 125Ω for 1:4 Wilkinson divider, practically a 130Ω chip resistor has been adopted because it is available in commercial.

Fig. 8 shows the three-dimensional structure of the 1:4 divider for EM simulation, and Fig. 9 illustrates the photograph of the fabricated 1:4 unequal power divider. The unequal divider having DGS has been inserted in metal housing as shown in Fig. 9(c).

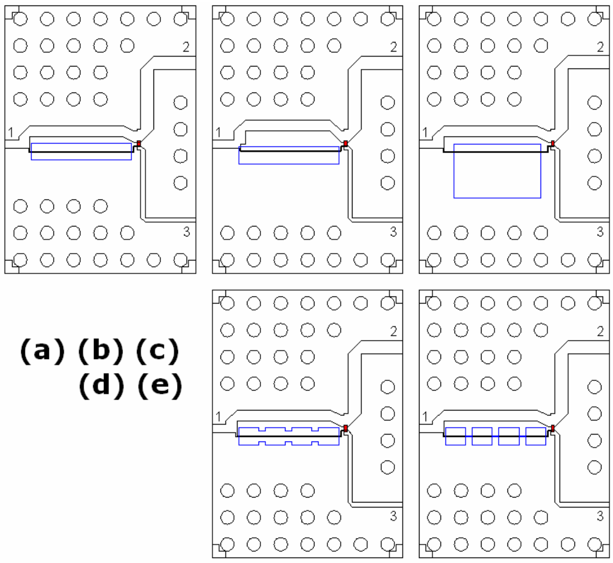

Fig. 7 Layouts of the 1:4 unequal power divider with DGS and double-layer substrate. (b)~(e) are modified layouts from (a).

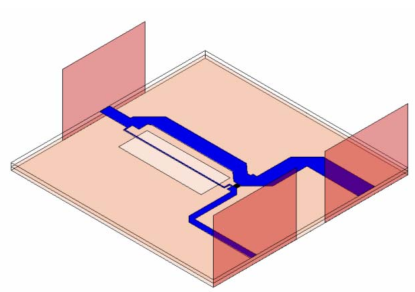

Fig. 8 Three-dimensional structure of the 1:4 divider for EM simulation

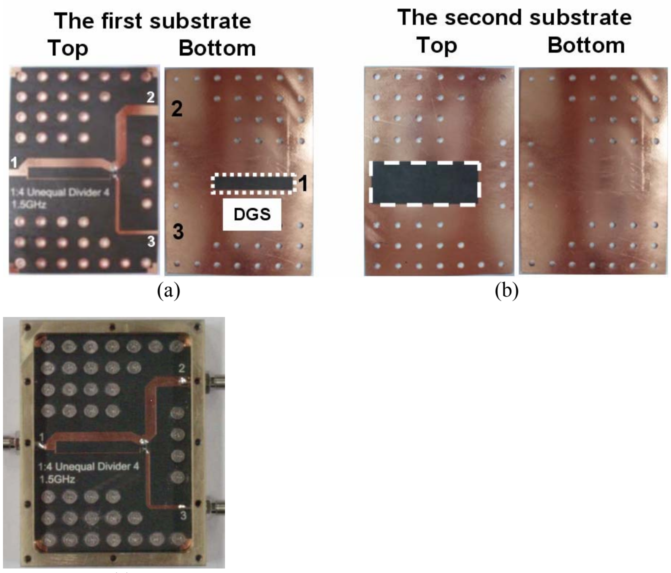

Fig. 9 Photograph of the fabricated 1:4 unequal power divider (a)1st substrate (b) 2nd substrate (c) packaged divider

Fig. 10 shows the predicted performances of the proposed 1:4 power divider. EM simulation has been performed using Ansoft HFSS. Fig. 11 presents the measured S-parameters, which have an excellent agreement with the predicted ones. The measured matching, power dividing ratio, and isolation characteristics are very good. The measured phase difference between output two paths is less than 1° in Fig. 12.

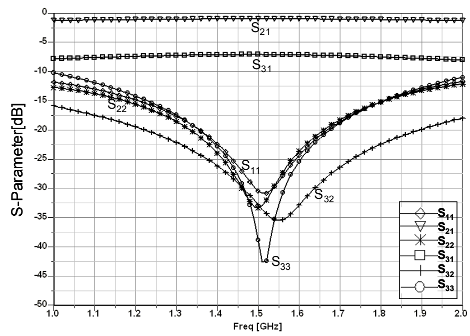

Fig. 10 EM Simulation data of the 1:4 unequal power divider

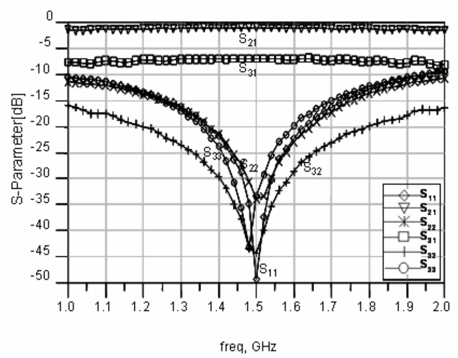

Fig. 11 Measured performances of the 1:4 unequal power divider

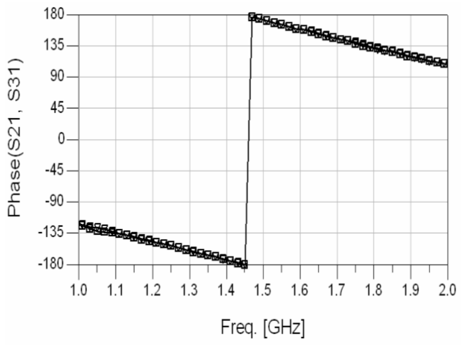

Fig. 12 Measured phase difference between S21 and S31

IV. CONCLUSION

A new DGS microstrip line with double-layer PCB structure has been proposed, and applied to a 1:4 unequal Wilkinson power divider. There is no ground problem due to the second substrate even after it has been packaged in metal housing. However, the advantages of DGS have not been degraded.

It is believed that the proposed DGS structure and is well applicable to other high frequency circuits with various DGS structure and other types of modified ground structures such as photonic bandgaps.

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