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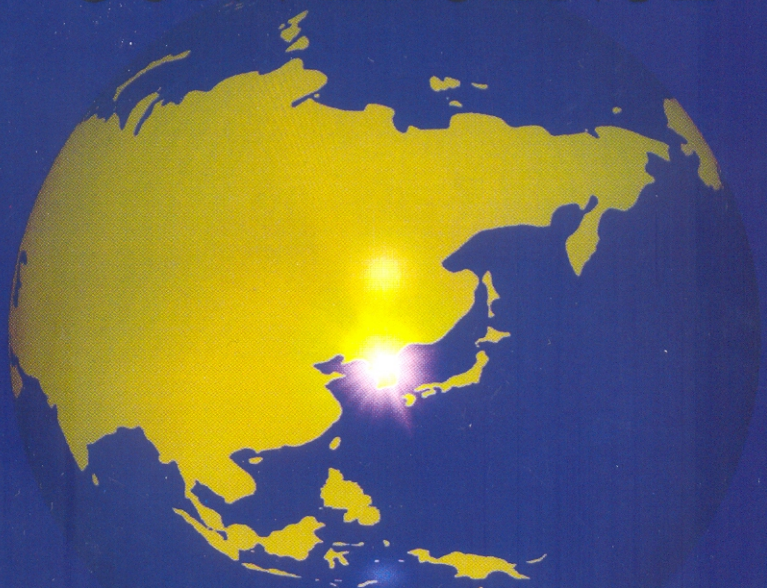

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A Modified CMOS Frequency Doubler Considering Delay Time Matching Condition

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Abstract

In this paper, a frequency doubler is designed that converts from 1.15GHz input signal to 2.3 GHz output signal using TSMC 0.18 CMOS Technology. The proposed doubler consist of a fully adjustable schmitt trigger (FAST), time-delay components, XOR gate and a voltage controlled delay line (VCDL). Time-delay components use RC integrator and comparator. Advantages of this topology include good fundamental frequency and harmonic frequency suppression, compact layout and low power consumption. The desired signal at 2.3 GHz is 0.871 dBm. The fundamental frequency at 1.15 GHz and third harmonic frequency at 3.45 GHz approximately 37 dBc below the 2.3 GHz signal. The fourth harmonic frequency at 4.6 GHz is approximately 24 dBc below the 2.3 GHz signal. The power consumption is 11.07 mW and the phase noise of the output signal is 100.5 dBc/Hz at 10 KHz offset.

1. Introduction

Modern communication systems require high frequency signal sources with high stability and low phase noise. High frequency signal sources can be obtained by multiplying the low frequency signal that has relatively high stability and low phase noise.

In general, frequency multiplier included the unwanted fundamental and harmonic components, and the spectral quality of the fundamental signal directly influences the multiplied frequency components. This method is to use the non-linearities of a transistor with large input signal [1]. Therefore, the phase noise in oscillators has been an important subject in theoretical and experimental papers [2][3].

When a multiplier operates with other microwave circuits --such as mixers, amplifiers, etc.-- serious problems may occur due to the undesirable frequency components and poor phase noise characteristics. Thus, input matching at the fundamental frequency is generally used, and matching for the doubled frequency. Also, band pass filters (BPF) are often used to diminish the fundamental and undesirable harmonic components, but the insertion loss of BPF's causes multiplied signal to be less than the required signal level. In addition, it is difficult to design BPF's with a high Q factor in monolithic microwave integrated circuits.

On the other hand, a frequency doubler was proposed using time delay technique [4][5]. Fig. 1 is a conventional frequency doubler block diagram. This topology is to delay the input signal by T/4, where T is the clock period, and the delayed signal is to feed in XOR gate. This technique, frequency doubler can be achieved with low power consumption, small chip area, and good fundamental and harmonic frequency suppression without filtering. Conventional frequency doubler can also be used as an analog multiplier by converting input sinusoid to a square wave. In practice, forth harmonic frequency suppression is low. The presence of this harmonic frequency is due to the uneven duty cycle of the output square wave which is caused by the two signals entering the XOR gate not being exactly 90? out of phase.

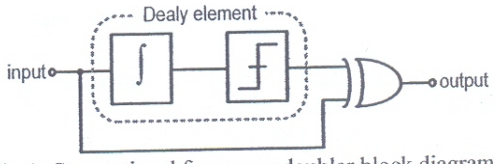

Fig.1. Conventional frequency doubler block diagram.

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In this paper, frequency doubler is presented based on the Fig.1. This circuit is converted from 1.15 GHz to 2.3 GHz. The designed frequency doubler added other circuits to solve existent problem. First circuit is a voltage controlled delay line (VCDL) to control delay time, and second circuit is a fully adjustable schmitt trigger (FAST) circuit to control duty cycle. The proposed frequency doubler circuit is designed by TSMC 0.18um technology.

2. Circuit design

A block diagram of the proposed frequency doubler is shown in Fig. 2. In conventional frequency doubler, the presence of fourth harmonic frequency is due to the uneven duty cycle of the output square wave which is the XOR gate not being exactly 90? out of phase. To solve this problem, proposed frequency doubler added the voltage controlled delay line (VCDL). The VCDL can regulate the delay time and phase difference of two XOR gate signals by 90? [6]. This topology can be used as an analog multiplier by inputting a sinusoid, converting it to a square wave. If the frequency is increased, duty cycle of converting square wave becomes irregular. The FAST can regulate the duty cycle of square wave by voltage control [7].

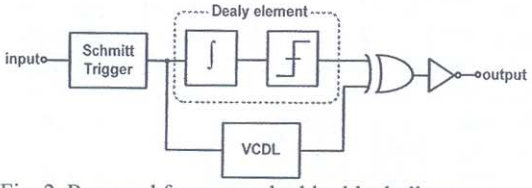

Fig. 2. Proposed frequency doubler block diagram.

2.1. Fully adjustable Schmitt trigger circuit

Input signal of the frequency doubler is sinusoid and the doubler circuit requires square wave. Thus, the first step is to make this conversion. If the frequency is increased, pulse width of square wave is narrow. Thus, rising time and falling time influence is increased. Thus, noise sensitivity of circuit is increased, and duty cycle of square wave is uneven.

The FAST can regulate the duty cycle of square wave by voltage control. The FAST has two independently adjustable threshold voltage levels such as lower threshold voltage ($V_{th,L}$) and higher threshold voltage ($V_{th,H}$). These components can be adjusted hysteresis by V_P and V_N. $V_{th,L}$ depends only on the control voltage V_N whereas $V_{th,H}$ depends only on the control voltage V_P. The schematic of FAST is as shown in Fig. 3.

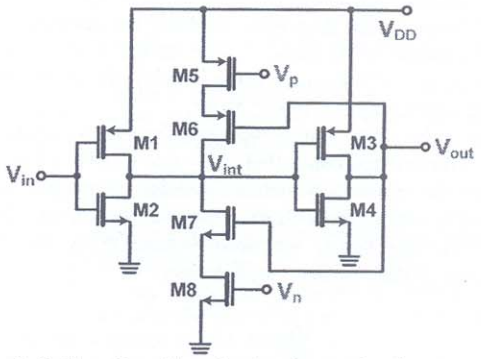

Fig. 3. Fully adjustable schmitt trigger circuit.

2.2. Delay elements

Delay elements consist of integrator and comparator using common-source amplifier (CS amp) and FAST as shown Fig. 4. The passive integrator consists of an RC integrator. We have assumed that the time constant τ is in the same range as the pulse width, and relation between time constant and frequency is $f0 = 1/\tau(\tau = RC)$. This equation sets a maximum tolerance between an ideal integrator and the passive integrator output. The RC integrator generates a triangular wave from a square wave when the $1/RC << f0$. The output signal of the RC integrator enters the comparator. However, amplitude of the triangular wave becomes smaller due to resistance components of RC integrator. This problem becomes more difficult for the comparator in the nest stage to determine the correct state. The comparator circuit is implemented by CS-amp and FAST. The CS-amp is used to amplify the triangular wave and the FAST can convert triangular wave to square wave.

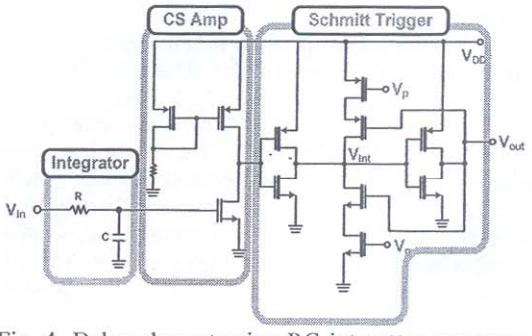

Fig. 4. Delay element using RC integrator, common-source amplifier and fully adjustable Schmitt trigger circuit.

2.3. Voltage controlled delay line (VCDL)

A conventional frequency doubler, the presence of fourth harmonic frequency is due to the uneven duty cycle of the output square wave which is the XOR gate not being exactly 90? out of phase.

To solve problem, proposed frequency doubler added the voltage controlled delay line (VCDL). Fig. 5 shows the circuit schematics for delay elements. This circuit is noting more than an inverter with a variable load. In this paper, we used 4-stage delay cell to increase adjustable delay time range.

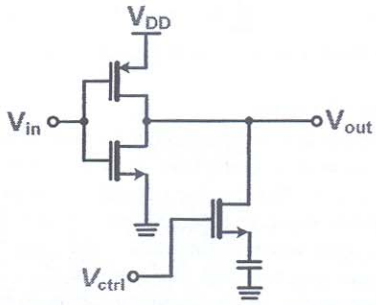

Fig. 5. Delay element of voltage controlled delay line.

2.3. XOR gate

The XOR gate is composed a transmission gates and two invertors as shown Fig. 6. The phase difference of input clock signals of the XOR gate is 90? and the output signal of this circuit becomes twice frequency of the input signal. The simulation of XOR gate is as shown Fig. 7.

3. Simulation result

We designed a frequency doubler using the time delay technique. An input sinusoidal signal at 1.15 GHz was used.

Fig. 8 is the output spectrum with an input power of 0 dBm. The desired signal at 2.3 GHz is 0.871 dBm. The fundamental frequency at 1.15 GHz and third harmonic frequency at 3.45 GHz approximately 37 dBc below the 2.3 GHz signal. The fourth harmonic frequency at 4.6 GHz is approximately 24 dBc below the 2.3 GHz signal. This result shows that the proposed frequency doubler improve the harmonic suppression characteristic through the time delay control. Table I summarizes the output spectrum of the simulated frequency doubler.

The phase noise of the output signal of designed frequency doubler is -100.5 dBc/Hz at 10 kHz offset. The DC supply voltage is 1.8 V and the circuit's DC current draw is 6.15 mA, resulting in a power consumption 11.07 mW for the circuit. The layout of designed frequency doubler shown in Fig. 9.

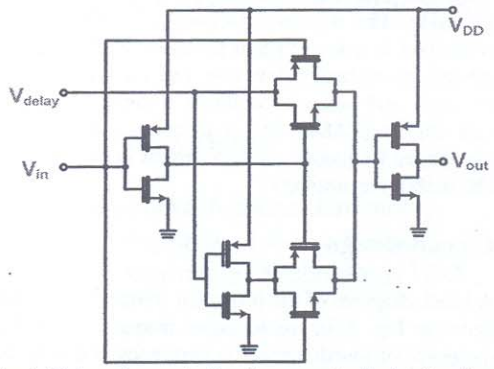

Fig. 6. Delay element of voltage controlled delay line.

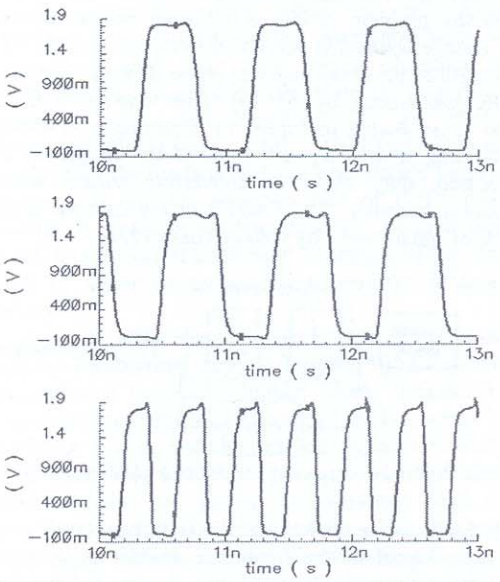

Fig. 7. Delay element of voltage controlled delay line.

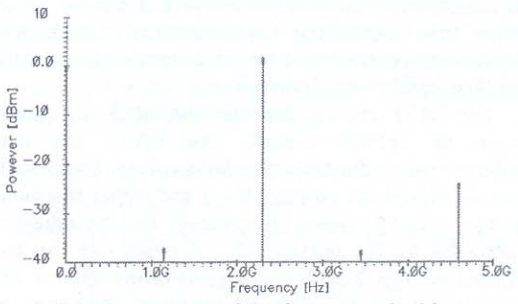

Fig. 8.Output spectrum of the frequency doubler.

TABLE I. OUTPUT SIGNAL OF THE FREQUENCY DOUBLER [dBm]

	P_{f0}	P_{2f0}	P_{3f0}	P_{4f0}
Doubler	-37.61	-0.871	-38.18	-24.69

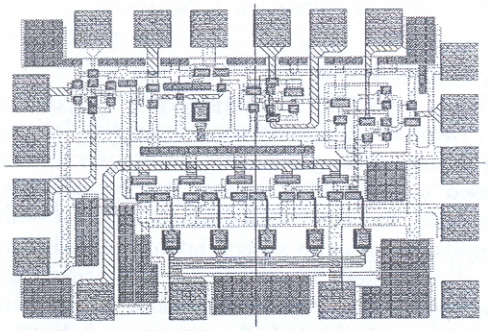

Fig. 9. Layout of the frequency doubler.

4. Conclusion

In this paper, a CMOS 0.18 um frequency doubler circuit has been designed and simulated. This circuit consists of time-delay elements, VCDL, FAST and XOR gate. This circuit converts 1.15 GHz input to 2.3 GHz output. The power consumption of the circuit is 11.07 mW and the circuit layout area is approximately 0.4 mm2. Simulation results show very good fundamental frequency, harmonic frequency suppression. Proposed frequency doubler improved the forth harmonic suppression value about 10 dBm than conventional frequency doubler. In the near future, this frequency doubler will be manufacture and measurement. We expect that the proposed frequency doubler design method is a great contribution to improving the quality of communication systems.

5. Acknowledgment

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