

A Novel Design of Frequency Multipliers Using Composite Right/Left Handed Transmission Line and Defected Ground Structure

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Abstract— A novel frequency multiplier using a composite right/left-handed transmission line and defected ground structure (DGS) is proposed. The left-handed transmission line (LH TL) in the proposed frequency multiplier suppresses the fundamental component (f_0), while the dumb-bell or spiral shaped DGS diminish unwanted harmonics such as second, third, and fourth harmonic. The frequency multipliers are designed at f_0 of 1 GHz by the proposed technique and measured results are presented. The measured output power at $2f_0$, $3f_0$, $4f_0$, is -3.77 dBm, -6.70 dBm, -6.58 dBm, respectively, when the fundamental input power is 0 dBm.

Keywords-Frequency multiplier, composite right/left handed transmission line, defected ground structure.

I. INTRODUCTION

Modern communication systems require high frequency signal sources with high stability and low phase noise. High frequency signal sources can be obtained by multiplying the low frequency signal that has relatively high stability and low phase noise. In general, frequency multipliers include the unwanted fundamental and harmonic components, and the spectral quality of the fundamental signal directly influences the multiplied frequency components. Therefore, the phase noise in oscillators has been an important subject in theoretical and experimental papers [1][2].

When a multiplier operates with other microwave circuits such as mixers, amplifiers, serious problems may occur due to the undesirable frequency components and poor phase noise characteristics. Band pass filters (BPF) are often used to reduce the fundamental and undesirable harmonic components, but the high insertion loss of BPF causes multiplied signal to be less than the required signal level. In addition, it is difficult to design BPF with a high Q factor in monolithic microwave

integrated circuits; a fully monolithic frequency multiplier design is very difficult.

On the other hand, it might be effective for feedforward structure to suppress the fundamental signal. However, the configuration has size problem due to the feedforward loop [3].

Artificial materials (metamaterials) with simultaneously negative permeability and permittivity are known as left-handed materials. LH materials often use arrays of metallic wires and split-ring resonators periodically loaded with series capacitors and shunt inductors [4]-[6]. A theoretical model and practical implementation of an artificial LH transmission line using interdigital capacitors and short circuit stub inductors was proposed [7].

In this paper, we propose a frequency multiplier with LH TL and DGS line. Since the LH TL is composed of several lumped elements, it is simpler and much smaller than feedforward structural multiplier.

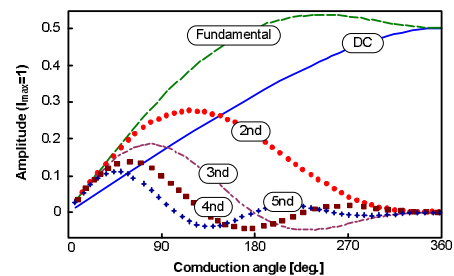


Figure 1. Amplitude comparison of the fundamental and harmonic components versus conduction angle.

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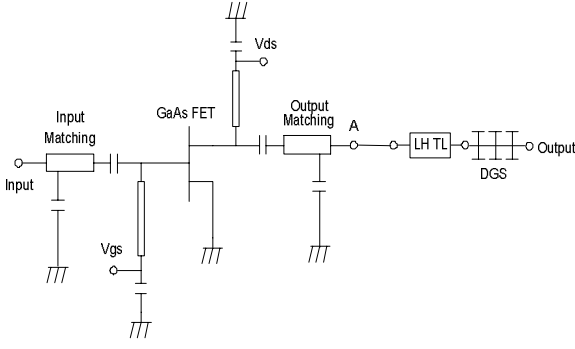


Figure 2. Block diagram of the proposed frequency multiplier.

II. FREQUENCY MULTIPLIER THEORY

The output current waveform to input voltage of transistors can be explained according to bias condition or conduction angle. The dc current consumption and harmonic signals to the bias are estimated by using averaging and correlation between a drain (or collector) current and the n th harmonic as shown in (1), (2) and Fig. 1, where α is a conduction angle of input signal and I_{max} is the maximum allowable current. The amplitude of the second harmonic, third harmonic and fourth harmonic is maximum when α is around 120° , 75° and 60° , respectively. Therefore, the bias point for frequency multiplier should be selected in the vicinity of pinch-off, between class B and C. Once the bias is determined, the input and output ports have to be matched for fundamental (f_0) and multiplied harmonic signal to maximize, respectively.

$$I_{dc} = \frac{1}{2\pi} \int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1 - \cos(\alpha/2)} [\cos \theta - \cos(\alpha/2)] d\theta \quad (1)$$

$$I_{dc} = \frac{1}{\pi} \int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1 - \cos(\alpha/2)} [\cos \theta - \cos(\alpha/2)] \cos n\theta d\theta \quad (2)$$

Fig. 2 shows the proposed frequency Multiplier. Even though the wanted harmonic component is larger than the unwanted signals at point "A", the magnitudes of unwanted components are not ignorable. However, they are suppressed totally by LH TL and DGS. Finally, the desirable harmonic component appears only at the output port.

III. CHARACTERISTIC OF THE LH TL AND DGS

A. Characteristic of the LH TL

The equivalent circuits of RH TL and LH TL are shown in Fig. 3. The phase responses of two unit cells are expressed by (3)

$$\phi_R = -\arctan \left[\frac{\omega}{2} \left(Z_{0R} C_R + \frac{L_R}{Z_{0R}} - \frac{\omega^2 L_R^2 C_R}{2Z_{0R}} \right) / (2 - \omega^2 L_R C_R) \right] < 0 \quad (3)$$

$$\phi_L = -\arctan \left[\frac{\omega}{2} \left(Z_{0L} C_L + \frac{L_L}{Z_{0L}} - \frac{1}{\omega^2 C_L Z_{0L}} \right) / (1 - 2\omega^2 L_L C_L) \right] > 0$$

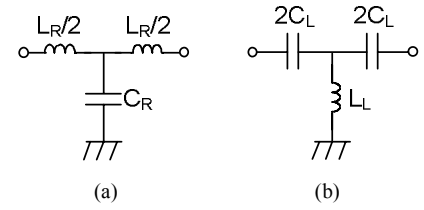


Figure 3. T-type unit cells. (a) RH TL. (b) LH TL.

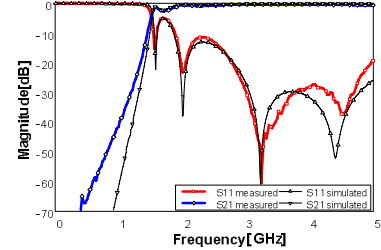


Figure 4. Simulated and measured results of the LH TL.

where Z_{0R} and Z_{0L} are characteristic impedances of the RH TL and LH TL, respectively, and expressed in (4).

$$Z_{0R} = \sqrt{\frac{L_R}{C_R}}, \quad Z_{0L} = \sqrt{\frac{L_L}{C_L}} \quad (4)$$

Since the electrical characteristic of the LH TL is similar to that of high pass filters, it is suitable to apply it to the output of the frequency multipliers for suppression of the fundamental component. The LH TL has been designed to have 4 unit cells, and the element values are $C_L=1.1\text{pF}$ and $L_L=2.8\text{nH}$, respectively. The characteristic impedance of the LH TL is about 50.5Ω . The RH TL with 50Ω characteristic impedance is implemented with a microstrip line. Fig. 4 shows the simulation and measurement result of the designed LH TL.

B. Defected ground structure (DGS)

The DGS pattern under the microstrip line produces the additional equivalent inductance and increased characteristic impedance. In conventional microstrip lines, the line width is getting extremely narrower as the required line impedance increases. However, in the microstrip line with DGS, the line width is broader than that of the standard microstrip line for the same characteristic impedance because the additional inductance results in the highly increased characteristic impedance. The broadened width of the DGS microstrip line can be understood as the increased equivalent capacitance, which plays a great role in raising the phase constant and slow-wave effects. The dumb-bell shaped DGS has a characteristic of low pass filter, and the spiral shaped DGS has a characteristic of band rejection filters. If we use the unequal spiral shaped DGS, we could obtain the characteristic of dual-band rejection, simultaneously. In this work, the dumb-bell shaped DGS microstrip line is used to diminish the higher-order harmonics over the third of doubler. The asymmetrical spiral shaped DGS is used to suppress the harmonics of $2f_0$, $4f_0$ of the tripler and the harmonics of $2f_0$, $3f_0$ of the quadrupler.

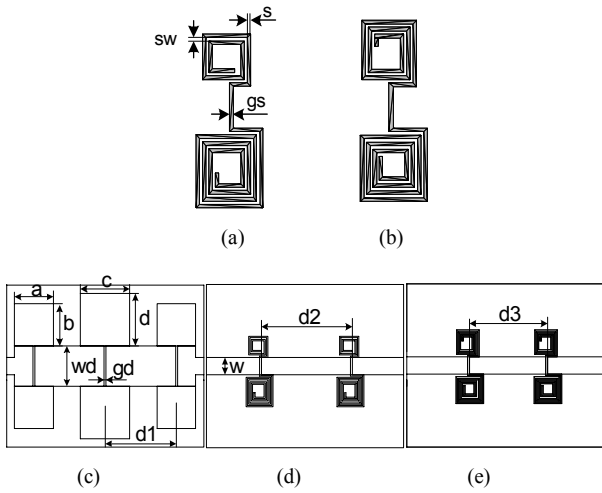


Figure 5. Layout of DGS of frequency multiplier. (a) spiral DGS unit for tripler, (b) spiral DGS unit for quadrupler, (c) for frequency doubler, (d) for frequency tripler, (e) for frequency quadrupler.

Fig. 5 shows the layouts of DGS of frequency multiplier and fig. 6 shows the simulated and measured results of the DGS [3].

IV. EXPERIMENT AND MEASURED RESULTS

We have designed a frequency multiplier using the proposed design method when the fundamental signal (f_0) is 1GHz. The adopted transistor is ATF10136 MESFET. The drain and gate bias voltages were set to 1.3V and -1.3 V. The transistor operated near the pinch-off region between class B and C. The matching points for input and output networks have been extracted using source-pull and load-pull methods, implemented in simulation using Agilent ADS. Fig. 7 through 9 shows the measured output spectrum of the frequency doubler, tripler and quadrupler. That is the conventional frequency multiplier, the frequency multiplier having the LH TL only and the proposed frequency multiplier having the LH TL and the DGS microstrip line. Table I summarizes output spectrum characteristics of several frequency multiplier structures.

The measured phase noise of the output signal ($2f_0$, $3f_0$, $4f_0$) are -97.17 dBc/Hz, -95.92 dBc/Hz and -94.57 dBc/Hz (at 10 - KHz offset) for that of input signal -101.5 dBc/Hz, which is better than the theoretical phase degradation condition expressed by $20\log(2)=6$ dB, $20\log(3)=9.5$ dB and $20\log(4)=12$ dB, by 1.67 dB, 3.92 dB and 5.07 dB, respectively.

V. CONCLUSION

A new design method for frequency multiplier has been proposed to obtain signal sources with high stability and low phase noise. The fundamental signal was suppressed using LH TL, and the unwanted harmonics were removed due to DGS microstrip line. The measured suppressions of the fundamental, third, and fourth harmonic components were 69.05, 66.57 and

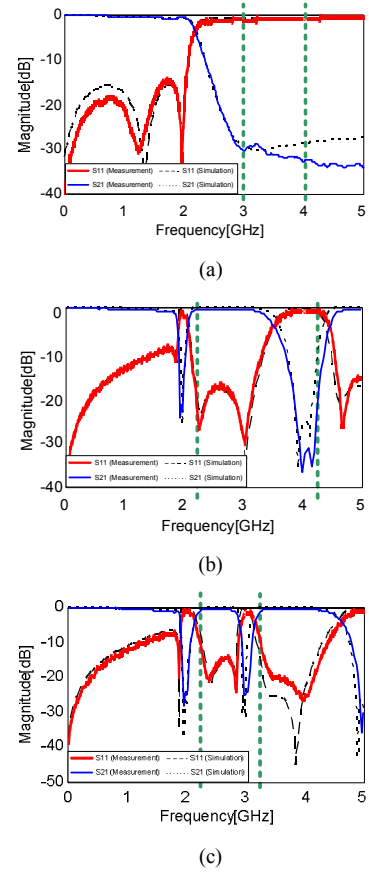


Figure 6. Simulated and measured results of the DGS. (a) for frequency doubler, (b) for frequency tripler, (c) for frequency quadrupler.

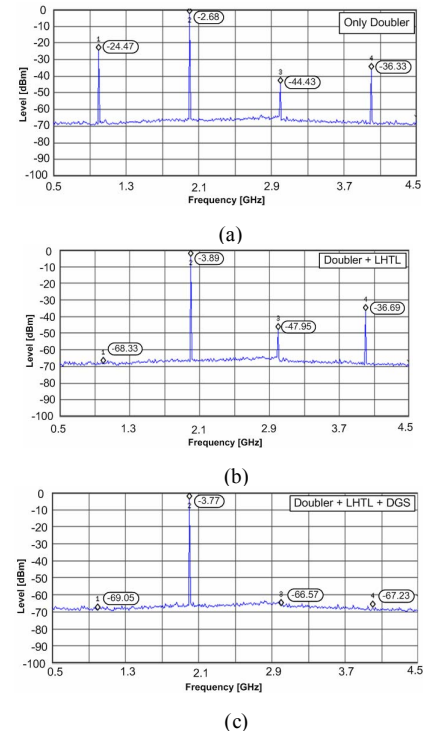


Figure 7. Measured spectrum of the frequency doubler.

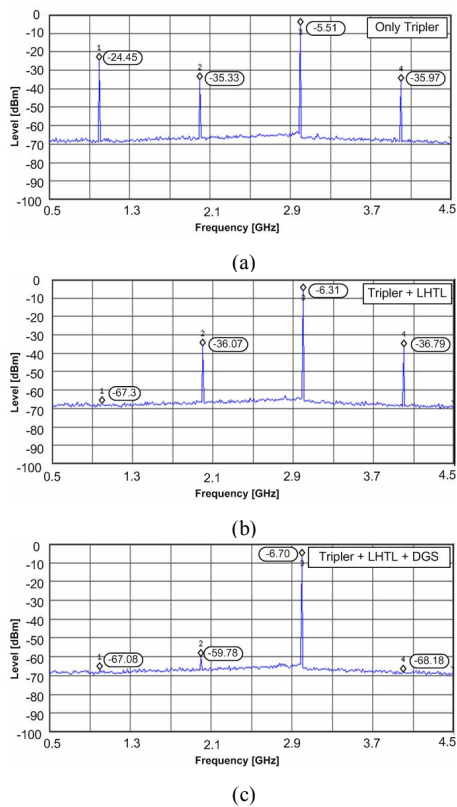


Figure 8. Measured spectrum of the frequency tripler.

69.23 dB for the doubler, respectively. For the tripler, the amount of harmonic suppression is 67.08, 59.78 and 68.18 dB,

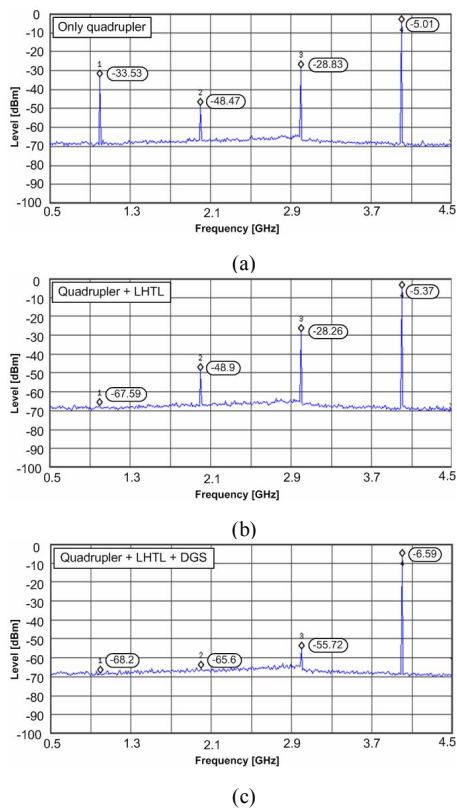


Figure 9. Measured spectrum of the frequency quadrupler.

TABLE I. COMPARISON OF HARMONIC OUTPUT POWER

$P_{n f_0}$ [dBm]	n=1	n=2	n=3	n=4
Only Doubler	-24.47	-2.68	-44.43	-36.33
Doubler+LH	-68.33	-3.89	-47.95	-36.69
Doubler+LH+DGS	-69.05	-3.77	-66.57	-67.23
Only Tripler	-24.35	-35.33	-5.51	-35.97
Tripler +LH	-67.3	-36.07	-6.30	-36.79
Tripler +LH+DGS	-67.08	-59.78	-6.70	-68.18
Only Quad	-33.53	-48.47	-28.83	-5.01
Quad +LH	-67.59	-48.9	-28.26	-5.37
Quad +LH+DGS	-68.2	-65.6	-55.72	-6.58

respectively. For the quadrupler, the harmonic suppressions are 68.2, 65.6 and 55.72 dB, respectively. It is believed that the proposed frequency multiplier can be integrated in monolithic integrated circuits by adopting microwave transmission line circuit because the fabricated frequency multiplier consists of resistor and lumped elements. It is also expected that the proposed frequency multiplier have a great contribution to improve the quality of communication without high Q band-pass filters.

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