Delay Matching Compensated CMOS Microwave Frequency Doubler

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***Abstract*—In this paper, a modified time-delay microwave frequency doubler is proposed. A voltage controlled delay line (VCDL) in the proposed frequency doubler compensates the time-delay mismatching between input and delayed signal. With the delay matching and waveform shaping using adjustable Schmitt triggers, the unwanted fundamental component (f_o) and the higher order harmonics such as third and fourth are diminished excellently. In result, only the doubled frequency component ($2f_o$) appears dominantly at the output port. The frequency doubler is designed at 1.15 GHz of f_o and fabricated with TSMC 0.18 µm CMOS process. The measured output power of $2f_o$ is 2.67 dBm when the input power is 0 dBm. The obtained suppression of f_o, $3f_o$, and $4f_o$ to $2f_o$ are 43.65, 38.65 and 35.59 dB, respectively.**

I. Introduction

Modern communication systems require high frequency signal sources with high stability and low phase noise for high speed data transmission technique. Traditionally, local oscillator with phase locked loop (PLL) has been used for microwave communication system. However, the stability of PLL is degraded as the operating frequency increases. Alternatively, high frequency signal can be obtained by multiplying the low frequency signal that has relatively high stability and low phase noise. Therefore, several design methods have been done on the frequency multiplier circuit [1]-[6].

The most widely used method is a frequency multiplier using the nonlinearity of a transistor [2]-[3]. Due to the periodic harmonic response of a transistor, the wanted frequency components at integer multiple frequencies of the fundamental component (f_o) can be obtained. By proper input and output matching, we can obtain the desired output component with maximum amplitude. However, additional harmonic termination circuit such as a band pass filter is required because the amount of unwanted harmonics including fundamental cannot be ignored.

Time-delay technique is another way of frequency multiplication and which is most likely to use in the digital circuit design [4]-[6]. An input square wave is delayed by T/4 with integrate and comparator circuit where T is the period of the input signal, and is fed into an XOR gate along with the input signal. Finally we can obtain the output with twice the input frequency. Fig. 1 shows a block diagram of the conventional frequency doubler using time-delay technique. As the operating frequency of the conventional frequency doubler using time-delay technique increases, we were confronted with two difficult problems to overcome. First, we cannot obtain an accurate square wave from a continuous wave (CW) using a simple inverter structure at higher frequency. Because the rising and falling time are considerably large and different for one period at high frequency, the logic performance of the XOR gate is degraded. We define this phenomenon as a duty cycle error. Second, assuming no duty cycle error, two inputs of the XOR gate may have a timing difference other than T/4 due to the propagation delay time of the delay element. This phenomenon is defined as a timing error. Timing error affects both the output power level of a desired multiplied signal and the unwanted harmonics suppression.

In this paper, we propose a modified time-delay technique based CMOS frequency doubler for higher frequency of operation with good f_o and the unwanted harmonics suppression. Schmitt trigger and voltage controlled delay line (VCDL) are adopted to diminish the duty cycle error and the timing error. The output power and unwanted harmonic suppression are much improved for higher frequency of operation.

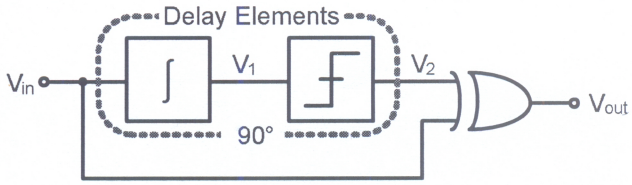


Fig. 1. Block diagram of the conventional frequency doubler using time-delay technique.

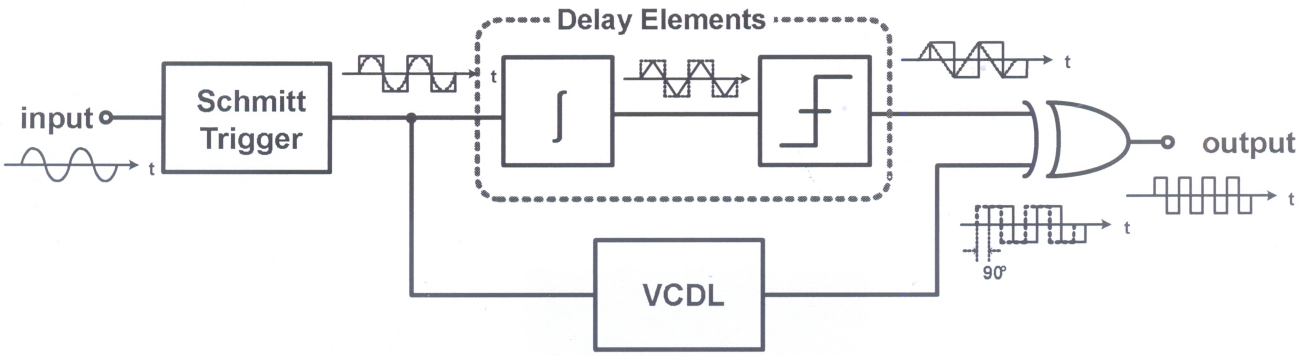


Fig. 2. Block diagram of the proposed microwave frequency doubler.

II. Circuit Design

Fig. 2 is the block diagram of the proposed microwave frequency doubler. The conventional simple inverter structure composed of PMOS and NMOS transistors can transforms the input sinusoidal wave to the square wave. However, as the frequency increases, duty cycle of a signal is uneven at the output of the inverter because rising and falling time of a square wave is comparable to the one period. This duty cycle error influences the performance of the circuit. This duty cycle error can be solved with Schmitt trigger instead of adoption inverter [7]-[9].

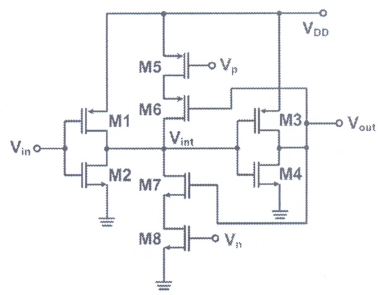
The transformed square wave is split into the delay element and the VCDL. And the delay element is composed of an integrator and a comparator. The integrator converts the square wave to a triangular wave and the comparator is then used to compare the triangular wave with a dc reference voltage. The resultant signal is a square wave which is delayed by 90° with respect to the input signal. Otherwise VCDL compensate the propagation delay time of the delay element to ensure the 90° phase difference at the input of an XOR gate. Finally the XOR gate can generate the wanted $2f_o$ with the exact 90° offset signals.

A. Schmitt Trigger

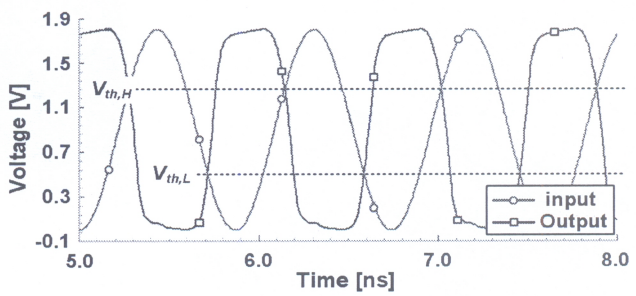
The input and output voltage of a Schmitt trigger has a hysteresis characteristics, as shown Fig. 3(a). The output goes to low when the input is higher than the higher threshold voltage, $V_{th,H}$, and the output goes to high when the input is lower than the lower threshold voltage, $V_{th,L}$. So the Schmitt trigger is a kind of a comparator with resistance to the noise with the amplitude between the two threshold voltages, $V_{th,H}$ - $V_{th,L}$. Therefore output waveform can generate the pure square wave with constant duty cycle. Fig. 3(b) is the schematic of the designed Schmitt trigger and consists of two inverters and four feedback transistors.

B. Voltage Controlled Delay Line

The phase (or timing) of a signal can be controlled by control voltage of the VCDL. Thus, the timing error between the reference input and the delayed signal can be optimized by VCDL [10]. The VCDL is circuit that adjusts the time delay of input signal according to the charging/discharging time of the load capacitance of an inverter. The average delay time of the inverter is expressed as Eq. (1).



(a)



(b)

Fig. 3. Schmitt trigger; (a) total schematic and (b) input/output voltage waveform characteristics.

$$t_d \approx \frac{2}{\mu C_{ox}(W/L)} \cdot \frac{C_L \cdot V_{DD}}{(V_{DD} - V_{th})^2} \quad (1)$$

Since the delay time is proportional to the load capacitor C_L, there is an additional transistor at the output stage to control this value, resulting in the change in the delay time. Fig. 4(a) is a schematic of the unit VCDL and Fig. 4(b) is a simulation result of 5-stage unit cell VCDL.

III. Measurement

In order to show the validity of the proposed doubler, we have designed a frequency doubler that multiplies 1.15 GHz

of the fundamental signal to produce the frequency output at 2.3 GHz. The proposed microwave frequency doubler is fabricated using CMOS TSMC 0.18 μm process. Fig. 5 is the microphotograph of the fabricated circuit. The core circuit layout area is approximately 0.8 x 0.5 mm^2, and the total chip area is 1.1 x 0.7 mm^2 including bonding pads. The supply voltage is 1.8.

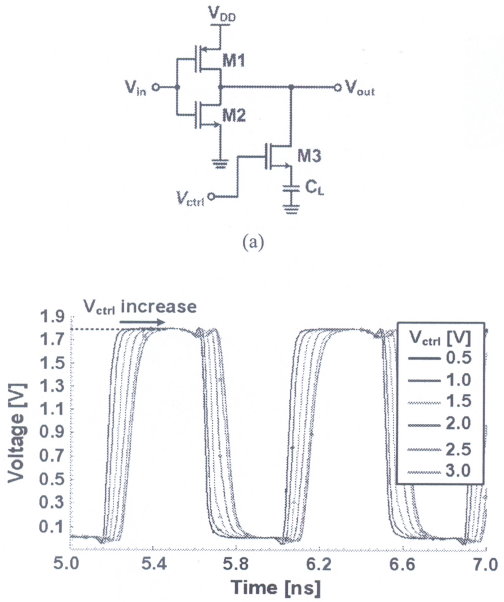


Fig. 4. Voltage controlled delay line (a) unit cell, (b) 5-stage VCDL output waveform through control voltage (V_{ctrl}).

Fig. 6 shows the simulated and the measured output spectrum of the fabricated microwave frequency doubler. The measured output power of $2f_o$ is 2.67 dBm, when the fundamental is fed with 0 dBm. The harmonic suppression of f_o, $3f_o$ and $4f_o$ compared to $2f_o$ are 43.65 dB, 38.65 dB, and 35.59 dB respectively. The measured phase noise characteristics of the output signal ($2f_o$) is -97.01 dBc/Hz (at 10 kHz offset), -109.7 dBc/Hz (at 100 kHz offset), and -115.5 dBc/Hz (at 500 kHz offset), respectively for that of input signal (f_0) is -102.2 dBc/Hz (at 10kHz offset), -118.5 dBc/Hz (at 100kHz offset), and -121.7 dBc/Hz (at 500kHz offset).

Table I is the performance comparison of the proposed circuit with the conventional frequency doublers in Ref. [4] And the compared Ref. [4] was most recently published measurement data which using time delay technique. However, by solving the duty cycle error and the timing error of a conventional circuit, we could achieve two times higher frequency of operation than the conventional circuit (Ref. [4]), showing excellent harmonic suppression performance. The improved harmonic suppression is 8.6 ~ 21.6 dB for all harmonic, and the 4th harmonic is improved by as much as 21.6 dB. Also, the proposed circuit has a conversion gain in contrast to the conventional circuit.

The total power consumption is 72 mW and this value is fairly high than the previous work. It is because the number of transistor of the proposed circuit increased due to the Schmitt trigger and VCDL. This is a cost for higher frequency of operation and excellent harmonic suppression.

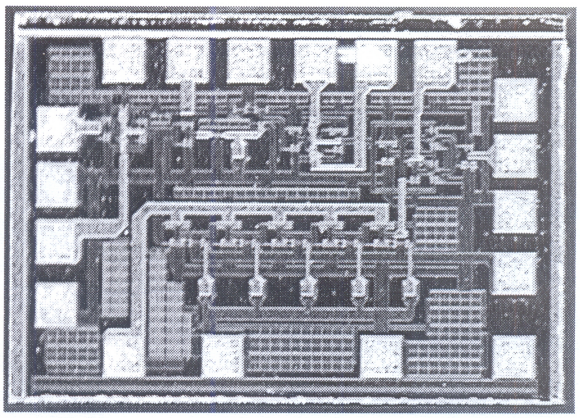


Fig. 5. Microphotograph of the fabricated microwave frequency doubler.

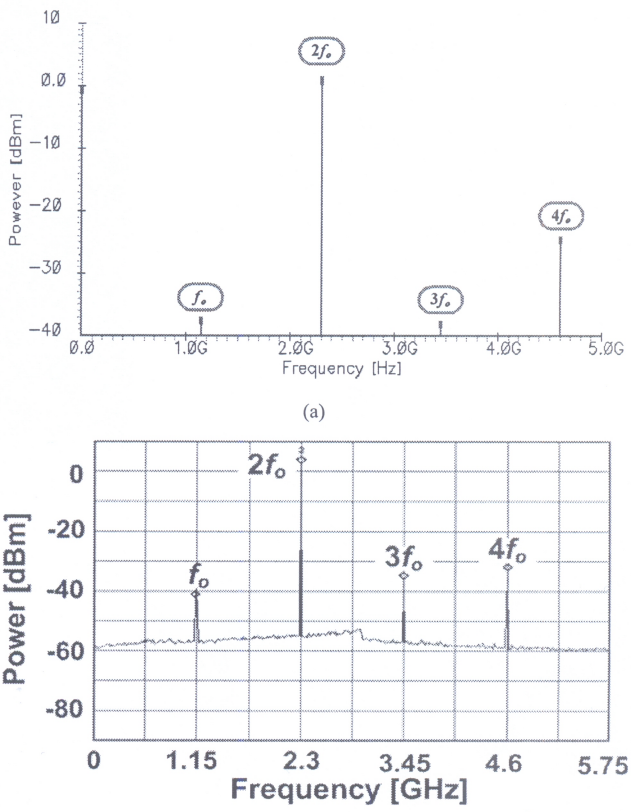


Fig. 6. Output spectrum with 0dBm input signal at 1.15 GHz. (a) simulation and (b) measurement.

IV. Conclusion

In this paper, the modified design method to increase the operating frequency and the unwanted frequency components

of the CMOS microwave frequency doubler using time-delay techniques is proposed. The conventional circuit cannot be used at higher frequency due to the limiting factors such as duty cycle error and timing error. The duty cycle error and the timing error are adjusted by the Schmitt trigger and the VCDL, respectively. It is expected that the proposed frequency doubling topology have a great contribution to increase in the operating frequency of various microwave and millimeter wave frequency multiplier circuit with RFIC. Even though good electrical performances, the power consumption of the fabricated frequency doubler consumes too much, we are redesigning to remove abundant circuits in the previous fabricated frequency doubler. Also we will design a new frequency multiplier such as tripler and quadrupler by the extension of the proposed frequency doubler.

TABLE I
PERFORMANCE COMPARISON

		Ref. [4]	This work	
			Sim.	Meas.
f_0 [GHz]		0.6	1.15	1.15
$2f_0$ [GHz]		1.2	2.3	2.3
P_{in} [dBm] at f_0		5	0	0
P_{out} [dBm] at $2f_0$		4	0.87	2.67
V_{DD} [V]		1.8	1.8	1.8
Current [mA]		5	40	40
P_{diss} [mW]		9	72	72
Harmonic suppression [dB]	f_o	30	36.74	46.6
	$3f_o$	30	37.31	38.6
	$4f_o$	14	23.82	35.6
Phase noise [dBc/Hz] (@100 kHz offset)		-109	-100.5	-109.7

ACKNOWLEDGMENT

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