A Compact DGS Load-Network for Highly Efficient Class-E Power Amplifier

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***Abstract*— A 20W class-E power amplifier (PA) with compact defected ground structure (DGS) load-network is presented for WCDMA base-station application. From the experiments, the proposed class-E PA achieves maximum power added efficiency (PAE) of 70.2 % at the output power of 43.05 dBm with the saturation gain of 12.7 dB. Harmonics are well below -46 dBc for 2nd harmonic and -52 dBc for 3rd, 4th, and 5th harmonics through the 8 dB output dynamic range. Comparing the complexity and the size, the proposed DGS load-network is much simpler and smaller than the conventional load-network with a number of open stubs, ensuring comparable harmonic load impedance and amplifier performance.**

I. INTRODUCTION

PA is the major source of heat and energy dissipation in the wireless communication system irrespective of mobile and stationary applications [1]-[2]. As the higher data rate signals exchange has become essential part of mobile communication (mp3, mega pixel digital photos and mobile games for iPhone of Apple Inc., for example), people's desire for longer batter life has been maximized nowadays. It implies the necessity of PAs with higher efficiency.

High-efficiency switching amplifier such as class-E is a promising solution for this situation with its relatively simple structure and experimentally achievable high-efficiency. Since its first introduction by N. O. Sokal and A. D. Sokal [3], significant research and experimental results have been published on the design equation [4] and load networks for class-E PA [5]-[6]. However, in case of considering up to 5th harmonic components, we should employ 4 open stubs with two series transmission line elements at least in addition to matching elements. Even though the electrical lengths (EL) of those components are relatively short because of its higher center frequency, they still occupy large space and increase the complexity of the circuit.

This paper presents a 20W class-E PA design with compact DGS load-network for WCDMA base-station application. To reduce the complexity of the conventional load-network and obtain comparable harmonics suppression, dumbbell shaped DGS /4 bias line and spiral shaped asymmetric DGS transmission line are designed for each target harmonic frequency. Experimental results such as gain, output power, PAE, and harmonic responses are presented according to output dynamic range and various input frequencies.

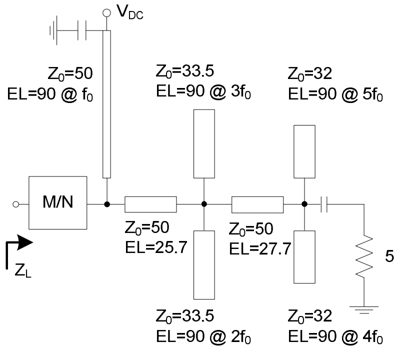


Fig. 1. Conventional transmission line load-network topology [6].

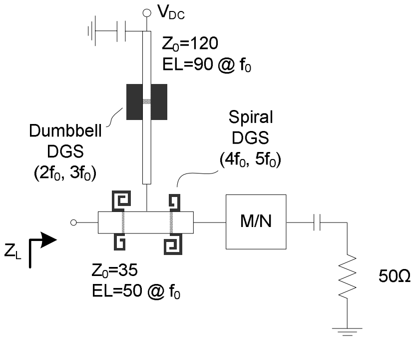


Fig. 2. Circuit schematic of the proposed DGS load-network for class-E power amplifier.

II. DGS LOAD-NETWORK AND CLASS-E AMPLIFIERS

Since the theories of Class-E PA have been well described in many previous articles, it is not mentioned here in detail.

Rather, main focus shall be the equivalent DGS load-network design procedure and performance analysis.

A. Conventional and DGS Load-Network Topologies

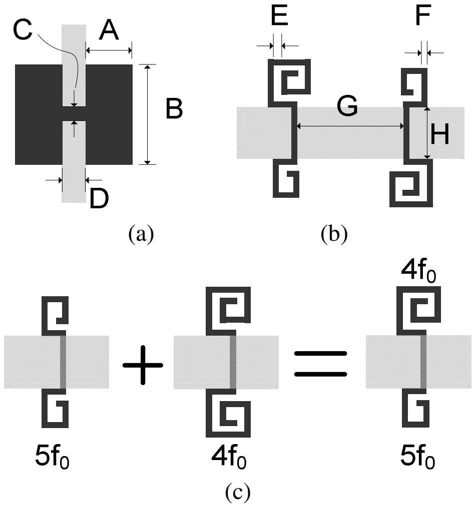
Circuit schematic of Fig. 1 shows the conventional transmission line load-network. As shown in the figure, transmission line load-network has several open stubs for each higher order harmonic to be suppressed of which EL are listed in the figure. Moreover, /4 bias line, which is only capable of rejecting 2nd harmonic, is typically used for most of the PAs instead of choke inductor due to power handling, higher order harmonic rejection, etc. Considering those transmission line elements, integration to a smaller size circuit can be a difficult problem. Even though harmonic suppression open stubs can be used also as a part of matching networks, achievable matching impedance area is fairly limited.

The DGS which is realized by etching a few specific (dumbbell or spiral shaped) patterns on the ground plane of the microstrip line produces the additional equivalent inductance for the conventional microstrip line. As a result, the line width is broader (0.41mm to 1.23 mm for 120Ω in this work) and the slow-wave effect is more increased than that of the conventional microstrip line for the same characteristic impedance [7][8]. The broadened width and the shortened line length of the bias line maintaining high characteristic impedance are very suitable features in PA design consuming large dc current. Also, DGS microstrip line has a frequency band rejection characteristic, of which passband and stop band can be controlled with physical shapes and sizes of DGS.

Fig. 2 shows the proposed DGS load-network. As an alternative to the several open stubs in Fig. 1, /4 bias line loaded with dumbbell shaped DGS, that suppresses 2nd and 3rd harmonics, and series transmission line (50° of electrical length in this case) loaded with asymmetrical spiral shaped DGS, which rejects 4th and 5th harmonics, are combined and included as a part of the output matching network. Comparing to the conventional circuit, /4 open stubs for 2nd and 3rd harmonics are merged into the /4 DGS bias line, while open stubs for 4th and 5th harmonics are integrated into the spiral DGS line. Additional line elements have never been inserted since we just utilized previously existing series lines and bias lines maintaining proper harmonic suppression effects without any stubs.

B. Class-E PA employing DGS load network

As explained, dumbbell DGS loaded /4 bias line rejects 2nd and 3rd harmonics simultaneously using slow-wave characteristics [8], while asymmetric spiral DGS transmission line suppresses 4th and 5th harmonics. Fig. 3 (a) and (b) shows the physical dimension of dumbbell and spiral shaped DGS optimized by 3D electro-magnetic (EM) simulation using Ansoft HFSS v11. As for an asymmetric spiral DGS, total perimeter and the number of turn of one symmetric unit cell is inversely proportional to the resonant frequency. Therefore, we first optimize the resonance frequency of the smaller unit symmetric spiral DGS to be equal to 5th harmonic frequency and the larger one to be tuned for 4th harmonic. By combining those two unit cells in one cell, we are able to obtain the desired dual-band suppression characteristic, as depicted in Fig. 3 (c). To broaden the cancellation bandwidth at 4th and 5th harmonic frequency, we inserted additional asymmetric unit cell with same perimeter as in Fig. 3 (b), and achieved the desired performance.



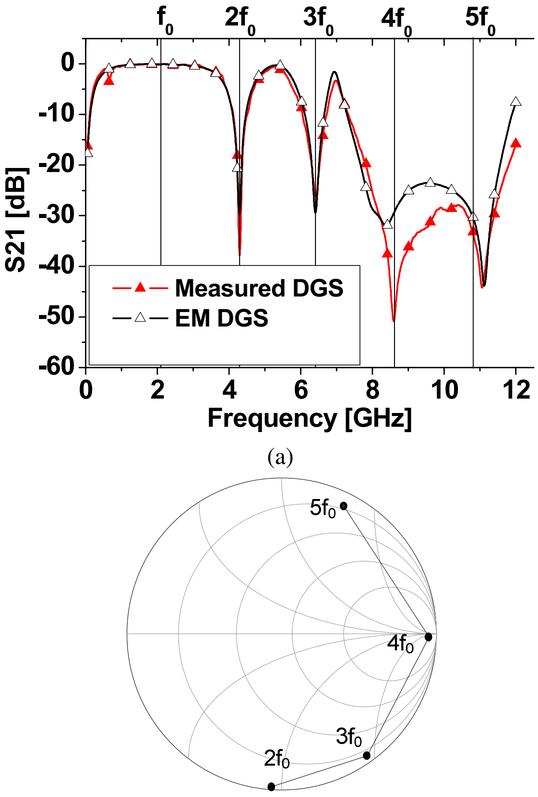
(a) (b)

(c)

Fig. 3. Physical dimension of DGS units: (a) dumbbell DGS (A=3mm, B=5.9mm, C=0.6mm, and D=1.2mm), (b) spiral DGS (E=0.4mm, F=0.4mm, G=6.4mm, and H=4mm) and (c) design procedure of asymmetric spiral DGS.

EM simulation and measurement result of the DGS load-network is shown in Fig. 4. In this work, fundamental frequency (f_0) is set to 2.14 GHz, center frequency of IMT-2000 base-station PA, and we considered up to 5th harmonic components. RT/Duroid 5880 (ε_r=2.2) laminate of Rogers Corp. is used for our work.

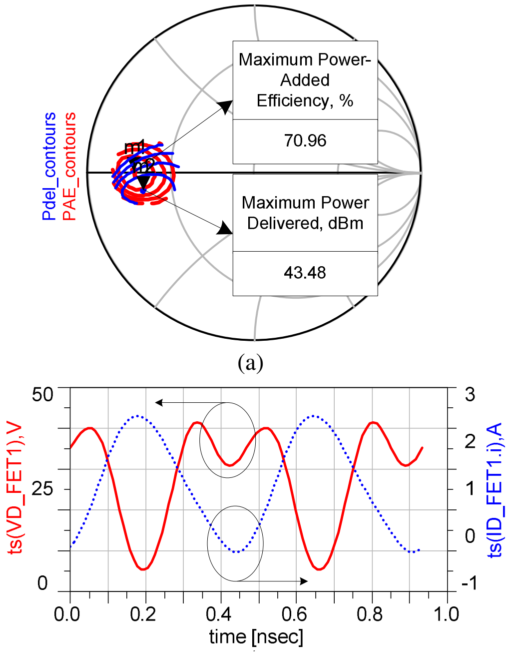
As shown in Fig. 4 (a), noteworthy advantage of the proposed DGS load-network is its extremely low loss, -0.05dB in this case, with comparable harmonic suppression of -37.2 dB, -26.7 dB, -49.5 dB, and -32.4 dB for 2nd, 3rd, 4th, and 5th harmonics, respectively. Low loss enables us to adopt the proposed concept to PA with higher output power. The reason of that measured result is better around 4th harmonic is due to the difference in the test condition whether there is a radiation boundary under the ground plate (simulation) or not (measurement). Fig. 4 (b) presents the measured input harmonic impedance of the DGS load-network. Although they are not ideally open, they are relatively open to the fundamental load impedance.



(a)

(b)

Fig. 4. (a) Simulated and measured transmission characteristics, and (b) measured input impedance of the proposed DGS load-network.



(a)

(b)

Fig. 5. Simulated (a) load pull contour with DGS load network for class E operation, (b) simulated voltage and current waveform.

Class-E PA is designed with gallium nitride high electron mobility transistor (GaN HEMT) NPTB00025 of Nitronex, which has a peak output power of 25W. Using the simulation model given by the company, we performed load-pull analysis with DGS load-network data imported from the EM simulation by Agilent ADS 2008a as shown in Fig. 5. Contours for the maximum power delivered to the load (0.5dB step) and the maximum PAE (4% step) is shown in Fig. 5 (a). Maximum achievable PAE is 70.96% with DGS load network at which the output power is 42.43 dBm. This result is obtained with the DC bias condition of V_{GS}=-2.2V (much lower than pinch-off) and V_{DS}=28V, and the switching capacitor is 0.68pF from the load-pull sweep for proper switching operation. Fig. 5 (b) presents switching voltage and current waveform. Although the waveform does not seem to be ideal switching function, voltage and current surely looks alternating with minimum crossing time, reducing dc power dissipation.

III. IMPLEMENTATION AND MEASUREMENTS

For comparison, reference class AB amplifier was also implemented with bias condition of V_{DS}=28V and I_{DS}=225mA with the same transistor. Optimum load impedance for class AB amplifier (Z_{Lopt}) was 7.65-j0.68 . Saturated output power and maximum PAE of class AB amplifier was 43.9 dBm and 58.5 % with saturated gain of 12.6 dB (linear gain = 13.6 dB). Experimental results are included in Fig. 6.

Based on the design of DGS load-network and the load-pull analysis results, class-E PA has been designed, implemented and measured. Saturated output power was 43.1 dBm with saturated gain of 12.7 dB and linear gain of 16.2 dB, as presented in Fig. 6. Maximum drain efficiency (DE) was 74.1 % and the maximum PAE was 70.2 % which shows good agreement with the simulation result.

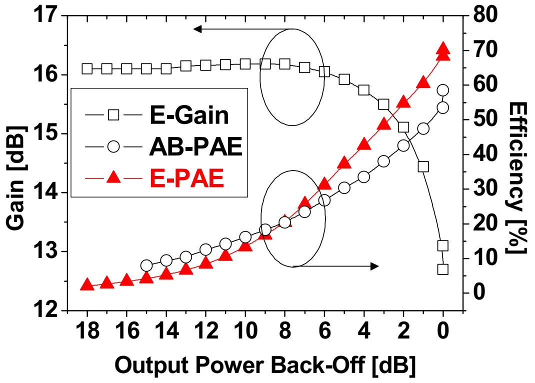


Fig. 6. Measured gain (E-Gain) and efficiency (E-PAE for class-E PA, AB-PAE for class-AB PA) according to output power back-off.

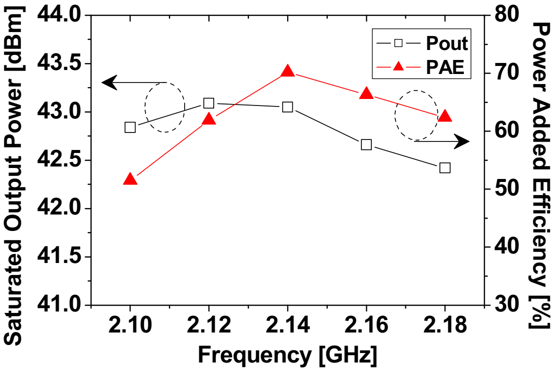


Fig. 7. Measured output power and PAE for various input CW frequency.

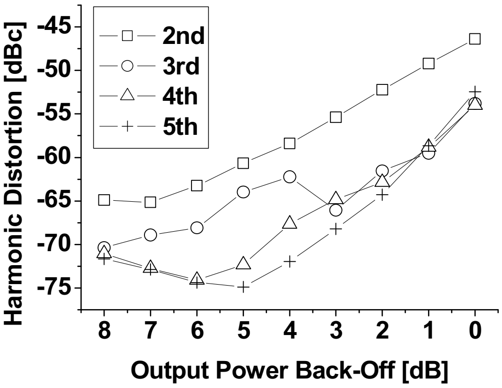
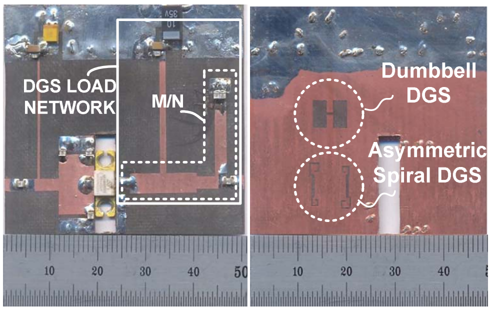


Fig. 8. Measured higher order harmonics level relative to fundamental.



(a) (b)

Fig. 9. Photographs of the fabricated Class-E PA with DGS load-network: (a) top and (b) bottom pattern.

Fig. 7 presents the measured output power and PAE over various input frequencies. For the entire bandwidth of IMT-2000 base-station (2.11~2.17 GHz), overall PAE is over 60%, achieving maximum PAE of 70.2% at the center frequency of 2.14 GHz with output power of 43.1 dBm. Measured higher order harmonic power levels are shown in Fig. 8. Harmonics are well below -46dBc for 2nd harmonic and -52dBc for 3rd, 4th, and 5th harmonics through the 8dB output dynamic range. Since the class-E PA is operated in a heavy saturation mode as 3dB gain saturation, harmonic levels are gradually increasing at higher output power, even though the relatively level to the fundamental output power is pretty low.

Photographs of the fabricated class-E PA with DGS load-network is presented in Fig. 9. Total size of the fabricated 20W class-E PA is 50 × 50 [mm^2], including the output matching network. If we limit our interest to the output-load network, the size reduction effect is much more evident.

IV. CONCLUSION

We have proposed compact DGS load-network for base-station 20W class-E PA, and illustrated design procedure with experimental results. Measured maximum PAE of 70.2% agreed well with the load-pull analysis using the proposed DGS load-network for class-E PA. It is expected that the extremely low insertion loss at the fundamental frequency and size reduction effect surely enables us to apply the proposed topology to the PA when higher output power and smaller size are required. Regarding the future works, applications of the proposed DGS transmission line and PA would be studied further of envelope tracking, envelope elimination and restoration transmitter systems.

ACKNOWLEDGMENT

This work is supported by the second stage of Brain Korea 21 Project.

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