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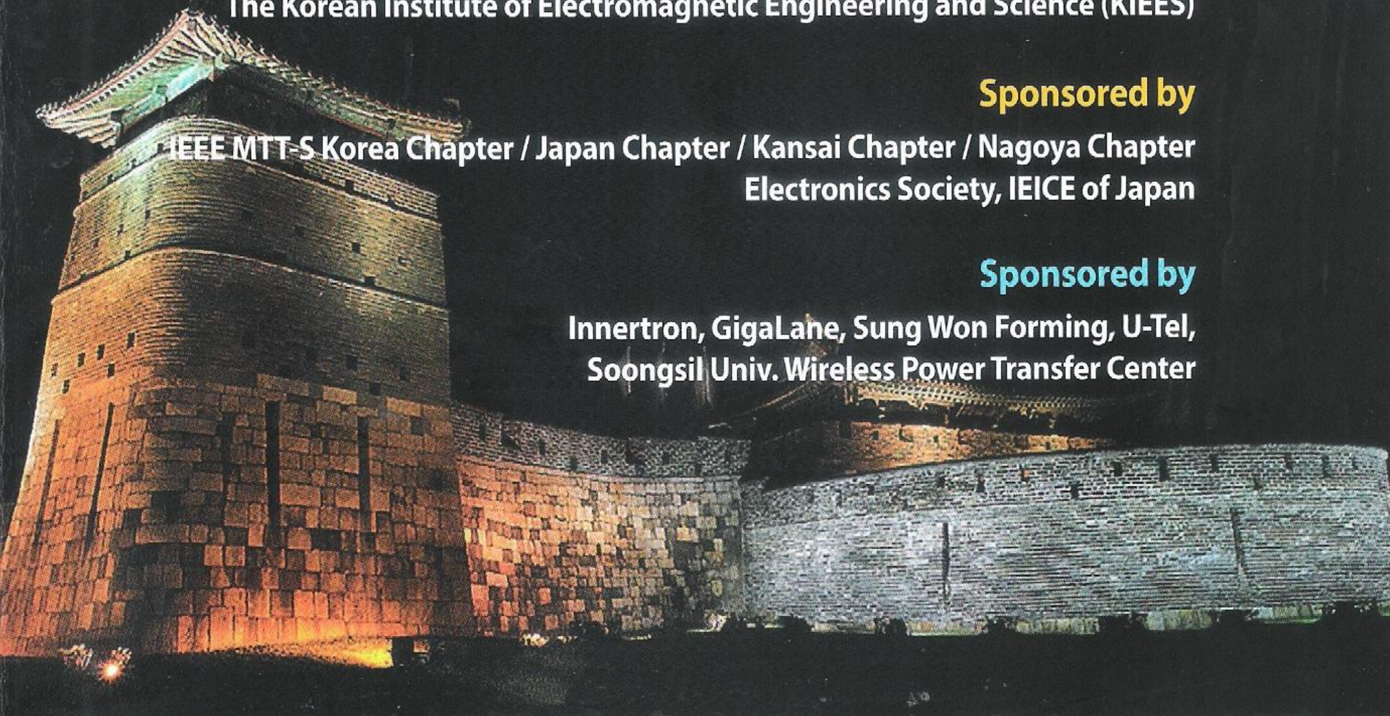

Session FR_1B (90 min): Filters and transmission lines

Session Chair: Prof. Jeong-Hae Lee (Hongik University, Korea)

Prof. Toshikazu Sekine (Gifu University, Japan)

Coffee Break 10:30 – 10:50

Transmission Line Negative Group Delay Circuit With Multiple-poles Characteristics

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***Abstract*—This paper presents a design of transmission line negative group delay (NGD) circuit with multiple-pole characteristics. By inserting an additional transmission line into conventional NGD circuit, the proposed circuit provides further design parameters to obtain wideband group delay (GD) and help to reduce the signal attenuation. The multiple-pole characteristics can provide the wider NGD bandwidth and can be obtained by connecting resonators with slightly different center frequencies separated by quarter-wavelength transmission lines. For experimental validation, two-poles in GD characteristics is designed, simulated, and measured.**

***Index Terms* — Distributed line, low signal attenuation, multiple-pole.**

I. Introduction

The negative group delay (NGD) phenomenon might yield the output of a wave packet preceding the input peak [1]. However, this does not violate the causality because the initial transient pulse is still limited to the front velocity, which will never exceed the speed of light [1].

In recent years, there has been an increasing amount of research on NGD circuits at microwave frequencies. The NGD occurs at certain range of frequencies where the absorption or the attenuation is maximum [1].Therefore, bandstop structures are used to realize NGD circuits. Based on either series or shunt *RLC* resonators, various kinds of microwave NGD circuits have been presented and demonstrated in literature [2]-[4]. To overcome the limited availability problem of lumped elements in RF and microwave, the NGD circuits using distributed elements are also presented [2]-[4]. However, the conventional NGD circuits presented in previous works exhibited excess signal attenuation (SA) up to 35 dB for -8 ns group delay (GD) which can cause serious stability issues when NGD circuit is integrated with systems such as the power amplifier linearization system. Therefore, for the same GD, the passband SA is expected to be as small as possible.

In this paper, a design of the transmission line NGD circuit with reduced SA and multiple-poles in GD characteristics is presented.

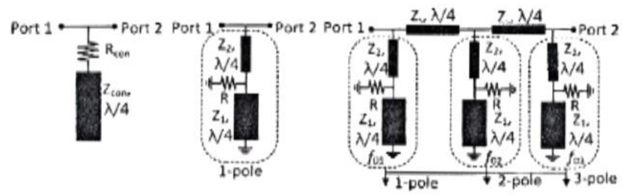

Fig. 1. Structure of transmission line NGDCs: (a) conventional, (b) proposed 1-pole circuit, and (c) proposed multiple-poles circuit.

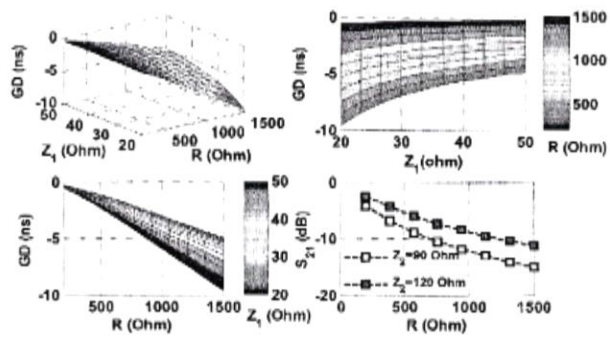

Fig. 2. Calculated group delay and signal attenuation of 1-pole NGD circuit according to R and Z_1 with Z_2=90Ω and f_0=1.96 GHz.

II. Design Theory

Fig. 1 shows structure of a conventional and proposed NGD circuit which consists of resistor R, transmission lines with characteristic impedances of Z_1 and Z_2 and electrical length of λ/4. The S-parameters and GD of circuit shown in Fig. 1(b) at center frequency (f_0) can be obtained as (1).

$$\left|S_{11}\right|_{f=f_0} = \left|S_{22}\right|_{f=f_0} = \frac{Z_0 R}{Z_0 R + 2Z_2^2} \quad (1)$$

$$\left|S_{21}\right|_{f=f_0} = \frac{2Z_2^2}{Z_0 R + 2Z_2^2} \quad (2)$$

$$\tau\big|_{f=f_0} = -\frac{d\angle S_{21}}{d\omega}\bigg|_{f=f_0} = -\frac{Z_0}{4f_0}\left\{\frac{(Z_1+Z_2)R^2 - Z_1 Z_2^2}{Z_1 Z_2\left(Z_0 R + 2Z_2^2\right)}\right\} \quad (3)$$

As seen from (3), the maximum achievable GD depends on Z_1, Z_2, and R. For better understanding of (2) and (3), the calculated maximum achievable GD and SA at f_0=1.96 GHz according to Z_1 and R are shown in Fig. 2.

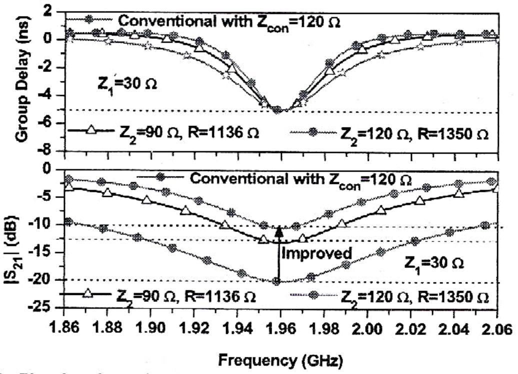

Fig. 3. Simulated results of 1-pole NGD circuit with different values of Z_2.

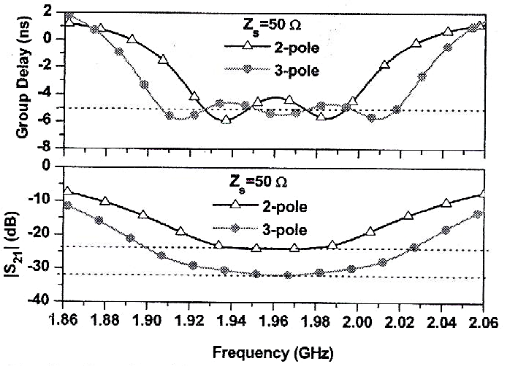

Fig. 4. Simulated results of 2-pole and 3-pole NGD circuit.

As seen from this figure, the SA is improved when value of Z_2 is high. Therefore, high Z_2 and low Z_1 are necessary for reduced SA.

Fig. 3 show simulation results of 1-pole NGD circuit. In this simulation, maximum achievable GD at f_0=1.96 GHz is assumed as -5 ns. As seen from this figure, the proposed circuit provides the reduced SA as compared to conventional one [3]. The SA in the proposed circuit is further reduced by making value Z_2 is high. However, the NGD bandwidth is also reduced.

The NGD bandwidth can be enhanced by connecting 1-pole NGD circuits with slightly different center frequencies separated by λ/4 transmission line of characteristics impedance Z_s=50 Ω as shown in Fig. 1(c). Due to different resonant frequencies of each 1-pole NGD circuits, the multiple-poles in GD characteristics can be obtained.

Fig. 4 show the simulated result of 2-poles and 3-poles NGD circuits. In case of 2-poles NGD circuit, two NGD circuit with center frequencies f_{01} = 1.935 GHz and f_{02} = 1.975 GHz are used. Similarly, for 3-poles NGD circuit, the center frequencies are given as f_{01} = 1.912 GHz, f_{02} = 1.963 GHz and f_{03} = 2.03 GHz. In both cases, the circuit element values of 1-pole NGD circuits are given as Z_1=30 Ω, Z_2=90 Ω and R=1139 Ω.

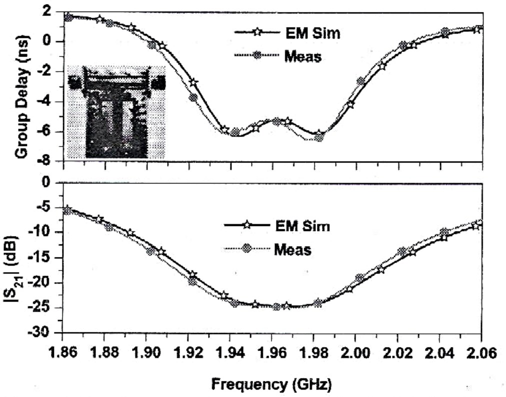

Fig. 5. Simulated and measured results of 2-poles NGD circuit.

III. Simulation And Measurement Results

For experimental validation of proposed circuit, the goal was to obtain GD of -6 ns at f_0 = 1.96 GHz. For this purpose, 2-poles NGD circuits was designed and fabricated. The circuit element values and center frequencies are same as 2-poles NGD circuit presented in section II. The circuit was fabricated in RT/Duroid 5880 of Rogers Inc. with dielectric constant (ε_r) of 2.2 and thickness (h) of 31 mils.

Fig. 5 shows the simulation and measured results of 2-poles NGD circuit. From the measurement, GD is determined as -5.80±0.45 ns over bandwidth of 80 MHz. The maximum SA at f_0=1.962 GHz is 24.67 dB.

IV. Conclusion

This paper demonstrates the design of negative group delay circuit with multiple-poles group delay characteristic and reduced signal attenuation. The multiple-poles negative group delay circuit is obtained by cascade connection of 1-pole circuit having slightly different frequencies. For experimental verification, 2-poles negative group delay circuit is designed, fabricated, and measured.

References

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