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Session Chairs:

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Fully On-Chip CMOS Active Negative Group Delay Circuit

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***Abstract*—This paper presents a design of CMOS active negative group delay (NGD) circuit with wideband characteristics. The proposed circuit consists of MOSFETs and the parallel RLC circuits connected to the source of MOSFETs. The simulation results show that the NGD is -0.97 ns and its NGD bandwidth is 152 MHz with $|S_{21}|$ of 8.44 dB at the center frequency of 2.4 GHz. The proposed circuit is designed in standard 65nm RF CMOS process and designed fully on-chip to adapt other applications.**

Keywords—CMOS, Common-source amplifier, Negative group delay, RLC resonator.

I. INTRODUCTION

Recently, some interesting researches of the negative group delay (NGD) concept have led to its experimental and application validation through the realization in electronic circuit [1]-[8]. The NGD occurs at range of frequencies where the absorption or signal attenuation (SA) is maximum. Therefore, a low SA NGD circuit is essential in wireless communication. In [2]-[4], a various design of passive microwave NGD circuits using RLC resonators are presented. The main drawback of passive NGD networks is their inherent SA. This can overcome by using a general purpose gain amplifier, however, it can decrease overall NGD. Therefore, a design of the active NGD circuits are essential for compensating the SA as well as preventing in decrease in group delay [5], [6]. Similarly, the conventional active/passive NGD circuits were implemented in microstrip technology which have bulky size. Since RFIC CMOS technology is a good candidate of circuit miniaturization, a research on implementing active NGD circuits in such technology are essential to reduce circuit size, and compensation the SA [7].

In this paper, an active NGD circuit implemented in CMOS is proposed. The proposed circuit provides NGD, reduced size, and improved the SA in passband.

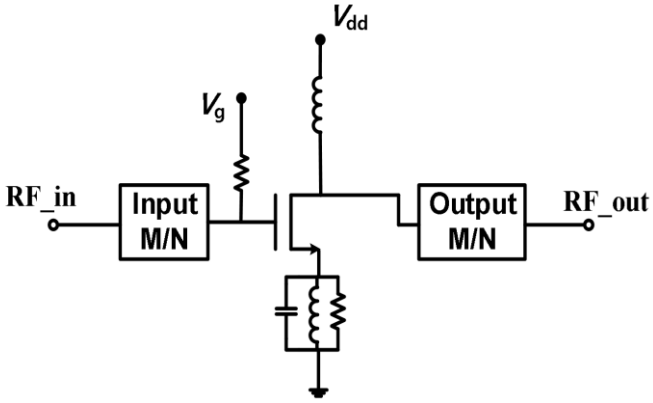

Fig. 1. Proposed CMOS active NGD circuit

II. DESIGN METHOD

Fig. 1 shows a block diagram of proposed CMOS active negative group delay circuit (NGDC). The proposed circuit consists MOSFETs and series-shunt RLC resonators attached to the source of MOSFETs.

Group delay (GD) times is defined as (1) [1].

$$GD = -\frac{d\phi}{d\omega} \tag{1}$$

where $\phi(\omega)$ are the frequency-dependent phase shift of S_{21}.

Fig. 2. (a) shows the schematic NGD circuit. For the group delay analysis, we used Z-matrix.

First, we found the input admittance of NGD network.

$$Y_{in,NGD} = \frac{1}{R} + \frac{1}{j\omega L} + j\omega C = \frac{\omega L + jR\left(\omega^2 LC - 1\right)}{\omega LR} \tag{2}$$

With Eq. (2), we can find the *ABCD*-matrix of passive network and *ABCD*-matrix was transformed to *Z*-matrix a shown in (3).

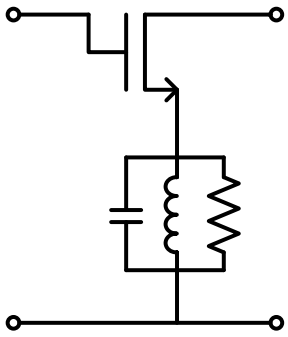

Fig. 2. basic structure of the proposed circuit and

$$Z_{NGD\_network} = \begin{bmatrix} \dfrac{\omega LR}{\omega L + jR\left(\omega^2 LC - 1\right)} & \dfrac{\omega LR}{\omega L + jR\left(\omega^2 LC - 1\right)} \\ \dfrac{\omega LR}{\omega L + jR\left(\omega^2 LC - 1\right)} & \dfrac{\omega LR}{\omega L + jR\left(\omega^2 LC - 1\right)} \end{bmatrix} \quad (3)$$

To find the *Z*-matrix of MOSFET, we used a Spectre of Cadence to extract the parameters of MOSFET. And with the *Z*-matrix calculation, we can get overall *Z*-matrix of the proposed circuit.

To find GD, *Z*-matrix should be transformed to *S*-matrix. For the transformation, we used conversion method from *Z*-matrix to *S*-matrix as shown in (4).

$$S = \begin{bmatrix} \dfrac{(Z_{11}-Z_0)(Z_{22}+Z_0)-Z_{12}Z_{21}}{(Z_{11}+Z_0)(Z_{22}-Z_0)-Z_{12}Z_{21}} & \dfrac{2Z_{12}Z_0}{(Z_{11}+Z_0)(Z_{22}-Z_0)-Z_{12}Z_{21}} \\ \dfrac{2Z_{12}Z_0}{(Z_{11}+Z_0)(Z_{22}-Z_0)-Z_{12}Z_{21}} & \dfrac{(Z_{11}+Z_0)(Z_{22}-Z_0)-Z_{12}Z_{21}}{(Z_{11}+Z_0)(Z_{22}-Z_0)-Z_{12}Z_{21}} \end{bmatrix} \quad (4)$$

We can get the *S*-matrix of overall circuit with matrix conversion method from the *Z*-matrix to *S*-matrix.

$$S_{21} = \frac{2Z_0\left(R_{21} + jX_{21} + \dfrac{\omega LR}{\omega L + jR\left(\omega^2 LC - 1\right)}\right)}{\left(R_{11} + jX_{11} + \dfrac{\omega LR}{\omega L + jR\left(\omega^2 LC - 1\right)} + Z_0\right)\left(R_{22} + jX_{22} + \dfrac{\omega LR}{\omega L + jR\left(\omega^2 LC - 1\right)} + Z_0\right) - \left(R_{12} + jX_{12} + \dfrac{\omega LR}{\omega L + jR\left(\omega^2 LC - 1\right)}\right)\left(R_{21} + jX_{21} + \dfrac{\omega LR}{\omega L + jR\left(\omega^2 LC - 1\right)}\right)} \quad (5)$$

Ultimately we can get GD with derivation of the phase of S_{21}. Since the GD equation was too complex and long to write down directly in this paper, we had performed in circuit simulation.

III. Chip Implementation

For an electrical verification, the proposed active NGD circuit was designed and implemented in CMOS technology.

The operating center frequency is chosen as 2.4 GHz. The chip was implemented in standard 65nm RF CMOS process. Fig. 3 shows the layout of proposed circuit. The circuit size is 1200 x 1000 μm^2 including the wire bonding pads. A Spectre of Cadence was used for the simulation.

Fig. 4 shows the simulated *S*-parameters characteristic of the proposed circuit. The simulated $|S_{11}|$, $|S_{21}|$, and $|S_{22}|$ at the center frequency are -29 dB, 8.45 dB, and -11.6 dB, respectively. As can see in Fig. 4(or Table I), the proposed circuit provides gain of 8.45 dB at the operating frequency. Similarly, Fig. 5 shows the simulation result of GD of the proposed circuit. From the simulation, a GD of -0.97 ns is obtained at the center frequency and bandwidth of NGD is 152 MHz. The simulation results are summarized in Table I.

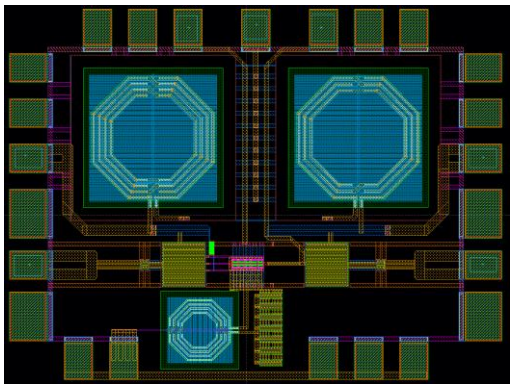

Fig. 3. Layout of proposed circuit.

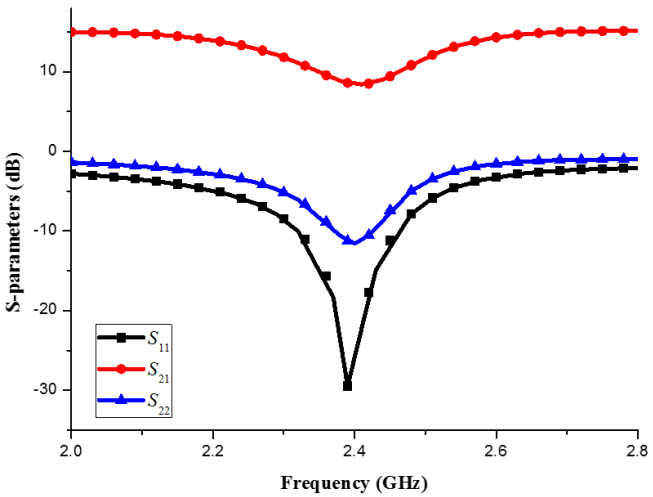

Fig. 4. Simulated S-parameter results.

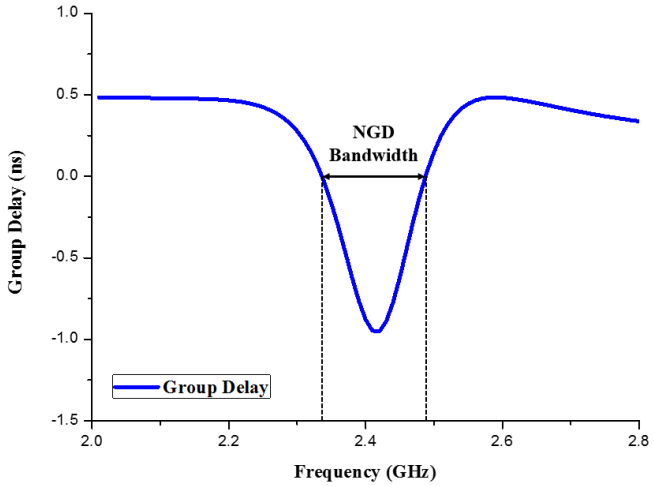

Fig. 5. Simulated group delay time

TABLE I. SIMULATION RESULT OF S-PARAMETERS.

S_{21}	S_{11}	S_{22}	*NGD at* f_0	*NGD bandwidth*
8.45 dB	-29 dB	-11.6 dB	-0.97 ns	152 MHz

IV. CONCLUSION

This paper presents the design of CMOS active negative group delay circuit using common-source amplifier structure with RLC shunt-series resonators. Generally passive NGD circuit cause the high insertion loss. To compensate the high insertion loss, we used parallel RLC NGD circuit with common-source amplifier. Because of this, the proposed circuit can provided NGD with gain at the operating frequency. With the proposed circuit, the NGD characteristic can be realized with small circuit size and applicable CMOS circuits to obtain another electrical performances.

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