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Session 3：Data and Web

14:45 - 17:50, October 20, 2017.   Location: Classroom 206, No1
Teaching Building, STDU.   Session Chairs:
  Prof. Zhaohui Qi (Shijiahzuang Tiedao University, China)
  Dr. Jianzheng Liu (Tianjin University of Science and Technology, China)

ID.3.   Joint Design of Interference Spin and Linear Transceivers for Two-Way Multi-Link Interference Networks
Junbeom Kim, Changyun Lee, Daesung Yu, Seok-Hwan Park and Yongchae Jeong
Chonbuk National University

ID.29.   Design of a Wideband Amplifier Using a Cascode Structure and Feedback Network
Jongsik Lim[1], Heeyoun Choi[1], Dal Ahn[1], Yongchae Jeong[2], Sang-Min Han[1] and Won-Sang Yoon[3]
[1]Soonchunhyang University
[2]Chonbuk National University, Rep. of KOREA
[3]Hoseo University, Rep. of KOREA

ID.51.   Enh-Code: An Enhanced Erasure Code Algorithm in Distributed Storage Systems
Chao Yin, Tongfang Li, Xiaoping Qu, Zhi Wang, Sihao Yuan and Qin Zhan
Jiujiang University, Jiangxi Province, Jiujiang City, China

ID.96.   Design and Realization of SHM Data Release System Based on Web
Yuhong Liu and Mubiao Su
Shijiazhuang Tiedao University

ID.104.   A Pheromone-Heuristic Artificial Bee Colony Algorithm for Web Service Instantiation
Lei Huo and Yuhong Liu
Shijiazhuang Tiedao University

ID.54.   Data Arrangement Algorithm for CAN Compression
Yeon-Jin Kim, Yang Zou and Jin-Gyun Chung
Chonbuk national university

ID.55.   Additional Zero-Byte Data-Reduction Algorithm for CAN
Yang Zou, Yeon-Jin Kim and Jin-Gyun Chung
Chonbuk national university

ID.103.   A Planetary Data System (PDS) in Data Management for Deep Space Exploration
Lijing Ren, Zhengxu Zhao, Denghui Zhang and Weihua Zhao
Shijiazhuang Tiedao University

ID.50.   Improving Network Lifetime with the Load Balancing Routing Metrics

Design of a Wideband Amplifier Using a Cascode Structure and Feedback Network

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Abstract—This paper describes the design of a cascade amplifier with a wideband gain and flatness. The well-known cascode structure is combined by a feedback network to suppress the increase of Miller capacitance. This produces a few advantages such as an extended cutoff frequency, mitigated degradation of gain at the mid-range in the targeted bandwidth, reduced ripple in gain, and improved matching performances. The designed amplifier, as a design example, has the bandwidth of 1 *GHz* or more when the center frequency is 1.8 *GHz*. The simulated and measured data show that the bandwidth, where the gain is higher than 8 *dB*, is wider than 1 *GHz* bandwidth. Even a minor frequency shift is observed in the measured S-parameters, the simple structure of the discussed cascade amplifier is believed to be applied for various wireless systems for the broadband operation.

Keywords— Cascode amplifiers, feedback amplifiers, broadband amplifiers

I. INTRODUCTION

Lots of wireless systems for communication, broadcasting, data service, and many other applications recently require much broader bandwidth and higher data rate because of the enormously increased practical data and information. This trend inevitably requires the broadband operation to RF and microwave systems and components to meet the unexpected bandwidth requirement for the future. If a wireless circuit has a considerable capability of wideband operation, it may be welcomed because it has a good applicability and one does not need to worry about the available operating frequency. Even though there is a limitation of gain because the gain-bandwidth product is almost constant, and it is not easy to get an excellent matching over the wide bandwidth, however the obtainable gain over the fairly broad operating band is one of key attracting factors if it is to be applied popularly.

It is well known that cascade structures decrease the effect of Miller capacitances and mitigate the degradation of mid-band gain [1-3]. Therefore this leads to the increase of cutoff frequency, and helps us to design wide band amplifiers. A cascade amplifier is discussed as one of solutions for wide band microwave amplifiers in this work. A feedback network is combined to the cascade structure to improve the matching and reduce in-band ripple [4].

II. DESIGN OF THE PROPOSED CASCODE AMPLIFIER

Fig. 1 shows the concept of Miller capacitance of transistors [5,6]. When there is a feedback phenomenon between input and output ports, even it is very small, the unwanted feedback capacitor, C_{io}, exists. In addition, the input impedance of Fig. 1(a) is well known as (1), so the Miller capacitor C_M, is $j\omega C_{io}(1+A_v)$, where I_{in} and A_v mean the input current and voltage gain of the transistor, respectively.

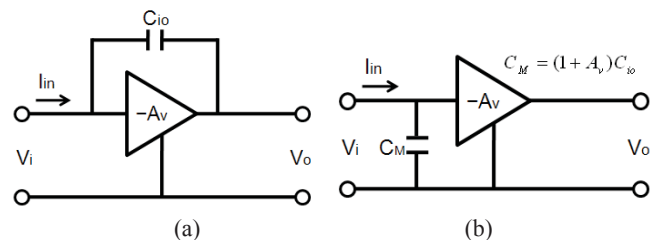$$Z_{in} = \frac{V_i}{I_{in}} = \frac{1}{j\omega C_{io}(1+A_v)} \tag{1}$$

Fig. 1. Increased input capacitance by the Miller effect (a)feedback capacitor between input-output ports (b)equivalent input capacitance due to the Miller effect

The Miller capacitance has negative effects such as decreased gain and limited cutoff frequency in the frequency responses, and ultimately the contribution to narrow bandwidth. [1-3]. One of good solutions to mitigate the Miller effect is the cascode structure. Because there is no feedback capacitance in common-gate transistors, the upper cutoff frequency tends to move to higher frequency, the total gain response is improved, especially in the point of view of operating bandwidth.

Fig. 2 shows a basic cascode structure with the connection of common-source (Q_1) and common-gate (Q_2) transistors [6]. In this structure, the load impedance of Q_1 becomes the input impedance of Q_2, or vice versa. The gain of Q_1 is simply defined as "$g_{m1}Z_{in2}=g_{m1}/g_{m2}$". If this structure is to be realized as an integrated circuit, the condition of "$g_{m1}=g_{m2}$" is recommended. So the same two transistors are adopted generally at the same time. In the cascode structure, the unwanted feedback capacitance of the common-source stage, if

any, is preserved to the originally low value which is quite smaller than C_M.

In addition, combining the RC feedback network to the cascode structure, it is possible to obtain the improved stability and gain-flatness of amplifiers [5].
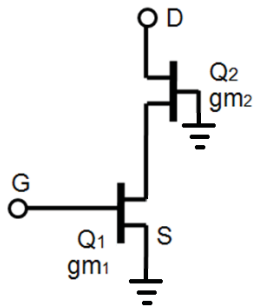

Fig. 2. Basic cascode structure with the conjunction of common-source and common-gate.

III. SIMULATION AND MEASUREMENT

Fig. 3 shows the schematic of the designed cascode amplifier. The center frequency is 1.8 *GHz* and the required design bandwidth is 1 *GHz* at least for the gain higher than 8 *dB*. The adopted FETs are FHX35LG small signal microwave transistors. The ADS (advanced design system) S/W from Keysight Technologies has been adopted to design and simulate the amplifier. In order to improve the reliability of design, electromagnetic simulations for discontinuity elements have been performed and reflected to the final schematic.
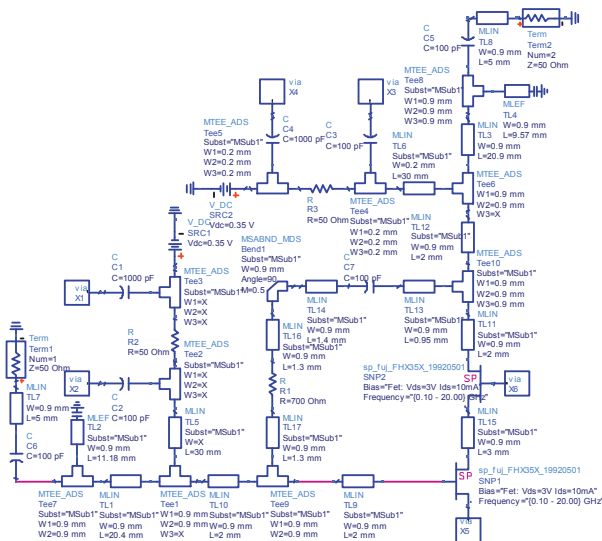

Fig. 3. Schematic of the designed cascode amplifier

Fig. 4 illustrates the predicted S-parameters of the amplifier from ADS. Focusing on the gain (S21), the frequency band where the gain is greater than 10 *dB* lies over 1 *GHz* to 2.6 *GHz*. Considering the bandwidth with the condition of matching less than -5 *dB*, the reasonable bandwidth is around 1.3 *GHz* to 2.3 *GHz* from Fig. 4.
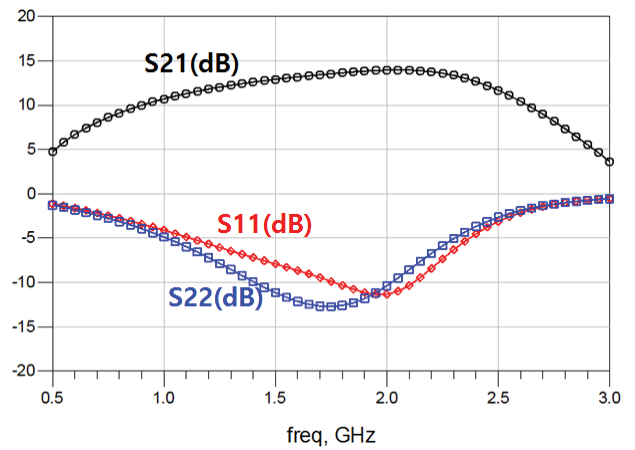

Fig. 4. Simulated S-parameters of the designed amplifier

The photo of the fabricated amplifier is presented in Fig. 5. The dielectric constant (ε_r) and thickness of the substrate are 2.2 and 31 *mils*, respectively. There was no trial to reduce the circuit size because this is the first prototype to evaluate the proposed design.
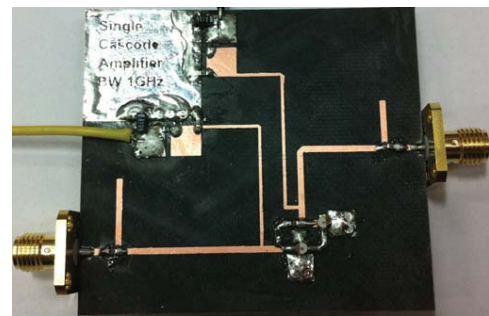

Fig. 5. Photo of the fabricated amplifier

Fig. 6 shows the measured S-parameters of the amplifier. Although there are some discrepancies between Fig. 4 and Fig. 6, a broad gain curve is observed. The measured gain flatness is ±1.5 *dB* over 1 *GHz* to 2 *GHz*, so this means a very broad band amplifier has been designed with a good flatness over 1,000 *MHz* of bandwidth.
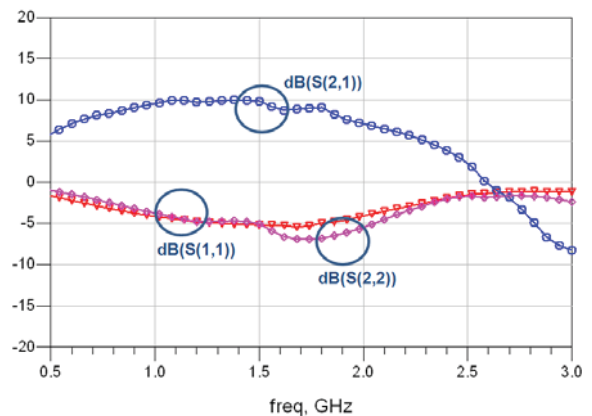

Fig. 6. Measured performances of the amplifier

IV. CONCLUSION

A broadband cascode amplifier with the bandwidth of more than 1,000 *MHz* has been designed and measured. A well-known cascode structure has been adopted to mitigate the Miller effect of transistors. In addition, a RC feedback network has been connected to guarantee the stable amplification and improve matching. The fabricated amplifier showed some discrepancies from the simulation such as low gain and frequency shift. It is noted that the fabricated amplifier is the first prototype built by an in-house facility. So it is expected that the performances would be improved by adopting a more refined matching network, exact analysis and design of the feedback network, and fabrication using a precise facility in the future.

REFERENCES

[1] B. Heydari, P. Reynaert, E. Adabi, M. Bohsali, B. Afshar, M. A. Arbabian and A. M. Niknejad, "A 60-GHz 90-nm CMOS Cascode Amplifier with Interstage Matching," *Proceedings of the 2nd European Microwave Integrated Circuits Conference*, pp. 88-91, Oct. 2007. Munich Germany.

[2] A. Tessmann, W. H. Haydl, A. Hulsmann, and M. Schlechtweg, "High-Gain Cascode MMIC's in Coplanar Technology at W-band Frequencies," *IEEE Microwave and Guided Wave Letters*, vol. 8, no. 12, pp. 430-431, Dec. 1998.

[3] A. Sedra and K. Smith, *Microelectronic Circuits* 5/e, Ch. 6, Oxford University Press, 2004.

[4] G. Gonzalez, *Microwave Transistor Amplifiers Analysis and Design 2/e*, Ch. 2 and Ch. 4, Prentice-Hall, 1997.

[5] T. Floyd, *Electronic Devices* 7/e, Ch. 10, Prentice-Hall, 2005.

[6] A. Sedra and K. Smith, *Microelectronic Circuits* 5/e, Ch. 5, Oxford University Press, 2004.