Microwaves Bridging Smart Cities

2019 Asia-Pacific Microwave Conference

APMC 2019 Singapore

10 - 13 December 2019 | Marina Bay Sands, Singapore | www.apmc2019.org

Program Book

Technical Sponsors

IEEE Advancing Technology for Humanity

IEEE Singapore Section

MTT-S

APS

IEEE Singapore MTT/AP Joint Chapter

EMC Society

Nanyang Technological University Singapore

NUS National University of Singapore

EuMA

Supported by

Singapore Exhibition & Convention Bureau

Held in

Singapore Passion Made Possible

Managed by

ace:daytons direct

14:00 A Compact Low-Pass Filter Based on Spoof Surface Plasmon Polaritons Using Defected Ground Structure
Dawei Zhang (Harbin Engineering University, P.R. China); Kuang Zhang, Ruiwei Dai and Wu Qun (Harbin Institute of Technology, P.R. China); Tao Jiang (Harbin Engineering University, P.R. China)

14:15 Design of Bi-Level-Microstrip Quadrature Directional Couplers with Indirectly Coupled Lines
Slawomir Gruszczynski, Krzysztof Wincza and Robert Smolarz (AGH University of Science and Technology, Poland)

14:30 A Wideband Balanced-to-Unbalanced Out-of-Phase Power Divider Based on Hybrid Microstrip/Slotline Structure
Yu Zhu, Kaijun Song, Maoyu Fan and Yong Fan (University of Electronic Science and Technology of China, P.R. China)

14:45 Two-Bit Chipless RFID for Temperature and Humidity Sensing
Wazie Mohammed Abdulkawi (King Saud University, Saudi Arabia); Abdel Fattah Sheta (King Saud University, College of Engineering, Saudi Arabia)

15:00 Wideband Bandpass Power Divider Using Slot-coupled Diamond-shape Microstrip Lines
Jie Lu, Haojie Chang, Weixing Sheng and Jie Cui (Nanjing University of Science and Technology, P.R. China)

15:15 X-band 12-way Dual Transition Radial Combiner
Su-Hyun Lee (R&D Lab, Korea)

15:30 Bandwidth and Gain Enhancement of CPW-Fed Slot Antenna Using A Partially Reflective Surface Formed by Two-Step Tapered Dipole Unit Cells
Hsiu-Ping Liao and Shih-Yuan Chen (National Taiwan University, Taiwan)

Session	**[F3-6] Reconfigurable Circuits**
Time / Date	Friday, December 13, 2019 / 13:30 – 15:30 hrs
Venue	Orchid 4311
Chair(s)	Wang Ling Goh (Nanyang Technological University, Singapore); Yongchae Jeong (Chonbuk National University, Korea)

13:30 Frequency Reconfigurable Shorting-Pin Loaded Rectenna for Smart Living
Hanis Amirah Ja'ffar (University of Malaya, Malaysia); Mohd Yazed Ahmad (University of Malaya & Faculty of Engineering, University of Malaya, Malaysia)

13:45 Reconfigurable Series Negative Capacitor Using Coupled Line Negative Group Delay Circuit and Varactor Diode
Girdhari Chaudhary, Phanam Pech, Junhyung Jeong and Yongchae Jeong (Chonbuk National University, Korea)

14:00 Switched-band Amplifier Using Switched Matching Network with Transmission Zeros
Ming-Lin Chuang, Ming-Tien Wu and Kuan-Chieh Chiu (National Penghu University of Science and Technology, Taiwan)

14:15 Broadband MMIC Phase Shifters Based on CRLH Circuit
Masatake Hangai, Ryota Komaru and Shintaro Shinjo (Mitsubishi Electric Corporation, Japan)

14:30 Automated Reconfigurable Antenna Impedance for Optimum Power Transfer
Mohammad Alibakhshikenari (Universitàdegli Studi di Roma "Tor Vergata", Roma, Italy); Bal Virdee (London Metropolitan University, United Kingdom); Chan H. Hwang See (Edinburgh Napier University, United Kingdom); Raed A Abd-Alhameed (University of Bradford, United Kingdom); Francisco Falcone (Universidad Publica de Navarra, Spain); Ernesto Limiti (University of Rome Tor Vergata, Italy)

14:45 Antenna Aperture Tuning with High-Voltage Bulk-CMOS Switch-Based RF Capacitor
Oguzhan Oezdamar (University of Erlangen-Nuremberg, Germany); Valentyn Solomko, Anthony Thomas, Kun Wang and Nadine Pfuhl (Infineon Technologies, Germany); Robert Weigel (Friedrich-Alexander Universität Erlangen-Nürnberg, Germany); Amelie Hagelauer (University of Bayreuth, Germany)

15:00 A Fully Integrated Switched Capacitor Using Low Temperature and Wet Release Process for Reconfigurable CMOS Triple-band Power Amplifier
Hyunok Cho (Kwangwoon University, Korea); Milim Lee and Changkun Park (Soongsil University, Korea); Jae Yeong Park (Kwangwoon University, Korea)

15:15 Tunable Bandpass Graphene Frequency Selective Surface with Quasi-Elliptic Response
Hai-Long Kong, Lin-Sheng Wu and Liang-Feng Qiu (Shanghai Jiao Tong University, P.R. China)

Reconfigurable Series Negative Capacitor Using Coupled Line Negative Group Delay Circuit and Varactor Diode

Girdhari Chaudhary
Division of Electronics and Information Engineering
Chonbuk National University
Jeonju, Korea
girdharic@jbnu.ac.kr

Phanam Pech
Division of Electronics and Information Engineering
Chonbuk National University
Jeonju, Republic of Korea
jes2phanam@jbnu.ac.kr

Junhyung Jeong
Division of Electronics and Information Engineering
Chonbuk National University
Jeonju, Republic of Korea
jjunh05@jbnu.ac.kr

Yongchae Jeong
Division of Electronics and Information Engineering
Chonbuk National University
Jeonju, Republic of Korea
ycjeong@jbnu.ac.kr

***Abstract*—This paper presents a reconfigurable microwave non-Foster negative capacitor using low loss negative group delay circuit and varactor diode. The proposed circuit consists of series transmission line, shunt short-circuited resistor connected coupled lines, and varactor diode. The negative capacitor is reconfigured by changing bias voltage of varactor diode. For the experimental demonstration, the proposed reconfigurable negative capacitor is designed, simulated, and measured. The measurement results show that the negative capacitor can be reconfigured from -0.72 pF to -0.85 pF by changing bias voltage of 2.5 V to 18 V.**

Keywords— Coupled line, low insertion loss negative group delay circuit, tunable negative capacitor.

I. Introduction

Non-Foster negative capacitor and inductors have wide range of applications in fields of electronic and microwave circuit design [1]. In addition, non-Foster elements based matching circuit can exceed the Bode-Fano limit on the maximum achievable matching bandwidth using passive networks [2]. For designing the non-Foster reactive elements, the Foster reactance theorem should be violated. Therefore, conventional methods for designing non-Foster elements are based on active device negative impedance converters (NICs) and negative impedance inverters (NIIs) [3]-[4]. However, active devices based non-Foster circuits suffer from stability problems.

Recently, intimate relation between non-Foster reactive elements and negative group delay (NGD) circuits have been introduced [5]. Therefore, non-Foster negative capacitor and inductors without stability issue have been realized at microwave frequencies by using NGD circuits [6]-[7]. In recent research, tunable negative capacitor and inductor have been realized using distributed amplifier-based reconfigurable NGD and varactor diode [8]-[9]. However, these requires several varactor diodes and distributed gain amplifiers.

In this paper, we propose the reconfigurable series negative capacitor based on low loss NGD circuit and single varactor diode. Analytical design equations have been presented for selecting circuit parameters. From the analytical analysis, it is shown that the series negative capacitor can be reconfigured by changing the bias voltage of varactor diode.

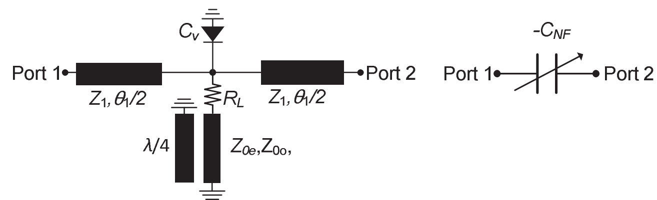


Fig. 1. Schematic of proposed reconfigurable non-Foster negative capacitor using negative group delay circuit and varactor diode.

II. Proposed Structure

Fig. 1 shows the proposed structure of the reconfigurable non-Foster series negative capacitor. The proposed structure consists of transmission lines (Z_1, θ_1), shunt resistor (R_L) connected short-circuited coupled line (Z_{0e}, Z_{0o}), and varactor diode (C_v). Using circuit theory, the overall S-parameters of the proposed circuit are derived as (1)

$$S_{11} = \frac{B - CZ_0^2}{2AZ_0 + B + CZ_0^2} \tag{1a}$$

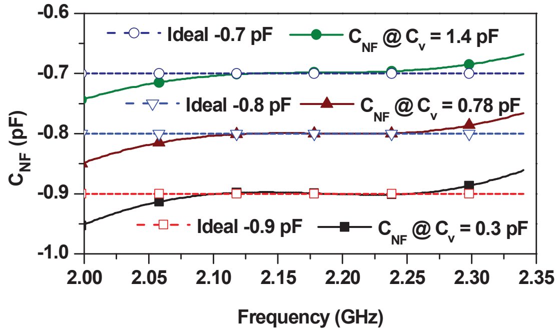
$$S_{21} = \frac{2Z_0}{2AZ_0 + B + CZ_0^2}, \tag{1b}$$

where

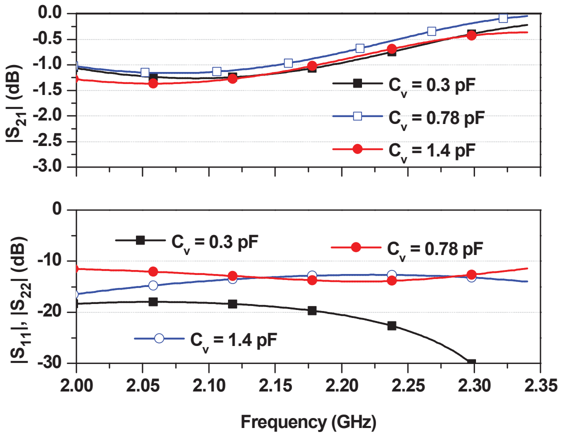
$$A = \cos\frac{\theta_1 f}{f_0} + \frac{j}{2} Z_1 Y_{in} \sin\frac{\theta_1 f}{f_0} \tag{2a}$$

$$B = jZ_1 \sin\frac{\theta_1 f}{f_0} - Z_1^2 Y_{in} \sin^2\frac{\theta_1 f}{2f_0} \tag{2b}$$

$$C = jY_1 \sin\frac{\theta_1 f}{f_0} + Y_{in} \cos^2\frac{\theta_1 f}{2f_0} \tag{2c}$$



(a)



(b)

Fig. 2. Simulated responses of (a) ideal series negative capacitances and proposed non-Foster negative capacitor with $\theta_1 = 38^o$, $Z_1 = 78\ \Omega$, $C_{eff} = -12.6$ dB, $Z_c = 310\ \Omega$, and $R_L = 200\ \Omega$ and (b) *S*-parameters of proposed circuit.

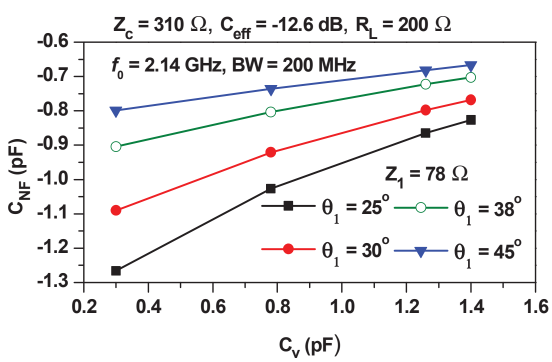


Fig. 3. Series non-Foster negative capacitance variations according to series transmission line electrical length (θ_1).

$$Y_{in} = j2\pi f C_v + \frac{x_1}{R_L x_1 + j x_2} \tag{2d}$$

$$x_1 = \cot^2 \frac{\pi f}{2 f_0} - C_{eff}^2 \csc^2 \frac{\pi f}{2 f_0} \tag{2e}$$

$$x_2 = C_{eff} Z_c \cot \frac{\pi f}{2 f_0} \tag{2f}$$

$$Z_c = \frac{2 Z_{0e} Z_{0o}}{Z_{0e} - Z_{0o}} \tag{2g}$$

$$C_{eff} = \frac{Z_{0e} - Z_{0o}}{Z_{0e} + Z_{0o}} \tag{2h}$$

Similarly, f and f_0 are operating and design center frequencies, respectively.

Furthermore, the relationship between S_{21} and non-Foster impedance Z_{NF} is written as (3) for non-Foster two-port network [9].

$$Z_{NF} = \frac{2 Z_0 (1 - S_{21})}{S_{21}} \tag{3a}$$

$$C_{NF} = -\frac{1}{im(Z_{NF}) \times 2\pi f} \tag{3b}$$

As noted from (3), if the S_{21} of the proposed circuit is same with ideal series negative capacitor network, the proposed circuit works as equivalently non-Foster negative capacitor.

To validate the proposed circuit, Fig. 2 shows the simulation results of the proposed circuit and compares with ideal series negative capacitances around 2.175 GHz. As seen from the Fig. 2(a), the proposed non-Foster series negative capacitor (C_{NF}) is reconfigured from -0.7 pF to -0.9 pF when C_v is varied from 1.4 pF to 0.3 pF, respectively. In addition, the C_{NF} is flat over the bandwidth of 200 MHz as like ideal negative capacitor.

Similarly, Fig. 2(b) shows the *S*-parameters of the proposed circuit. As observed from this figure, the maximum insertion loss varies from 1.26 dB to 1.36 dB when C_v is changed from 0.3 pF to 1.4 pF, respectively. In addition, the input/output return losses remain higher than 12 dB within bandwidth of 200 MHz for overall tuning range of C_{NF}.

Fig. 3 shows the calculated C_{NF} according to the electrical length (θ_1) of the series transmission line. In these calculations, input/output return losses are maintained higher than 12 dB within flat C_{NF} bandwidth of 200 MHz at f_0 = 2.175 GHz. As seen from this figure, the tunable range of C_{NF} is increased as θ_1 decreases. However, small θ_1 makes difficult to connect the SMA connector and biasing circuits of varactor diode.

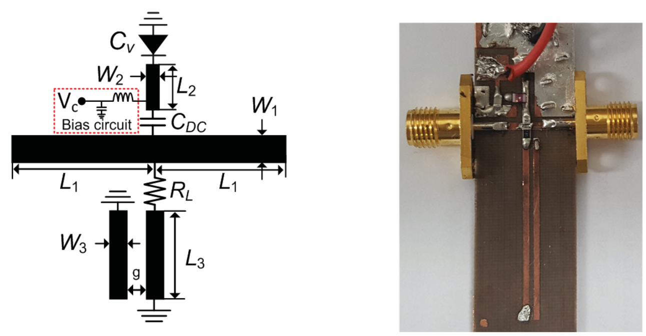
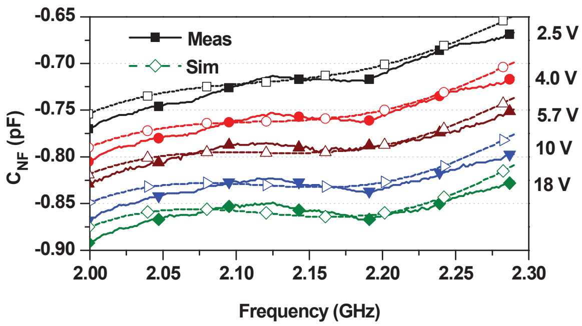
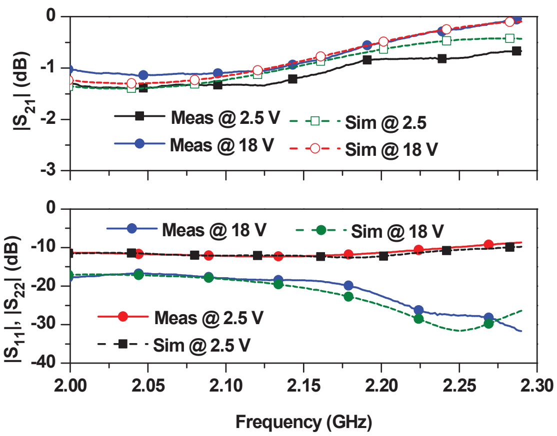


Fig. 4. (a) Physical layout with physical dimensions with R_L = 180 Ω and C_{DC} = 1.5 pF, and (b) photograph of fabricated circuit. Physical dimensions: L_1 = 8, L_2 = 6, L_3 = 27, W_1 = 1.20, W_2 = 1.10, W_3 = 1, g = 0.6. (Units: millimeter).



(a)



(b)

Fig. 5. Simulation and measured results of reconfigurable non-Foster circuit: (a) series non-Foster negative capacitances and (b) *S*-parameters.

III. Simulation and Measurement Results

For the experimental validation, the circuit was designed and fabricated using Taconic PCB substrate (ε_r = 2.2 and h = 0.787 mm). The design goal was to obtain series non-Foster negative capacitor of -0.7 pF to -0.9 pF. In this work, varactor diode SMV-1231 from Skyworks was used. The physical layout and photograph of fabricated circuit are shown in Fig. 4.

Fig. 5(a) shows the simulation and measured results of series non-Foster negative capacitor. The measurement results are well agreed with simulation. From the measurement, non-Foster negative capacitance is varied from -0.71 pF to -0.85 pF within 200 MHz bandwidth when a bias voltage is varied from 2.5 V to 18 V. Similarly, the insertion loss and input/output return losses are shown in Fig. 5(b). As seen from this figures, maximum insertion loss is varied from 1.15 dB to 1.406 dB and minimum input/output return losses are varied from 17.5 dB to 12.2 dB within bandwidth of 200 MHz when bias voltage varies from 18 V to 2.5 V, respectively.

IV. Conclusion

In this paper, we demonstrated the reconfigurable series non-Foster negative capacitor based on a negative group delay circuit and varactor diode. The proposed circuit provides the low insertion loss and negative capacitances by changing the bias voltage of varactor diode. Because of simple design and implementation, the proposed circuit is expected to further apply in reconfigurable non-Foster circuitries to enhance the functionalities of microwave circuits and systems.

Acknowledgment

This research was supported by the Basic Science Research Program through the National Research Foundation (NRF) of Korea, funded by Ministry of Education, Science and Technology (2016R1D1A1A09918818), in part by the Basic Science Research Program through NRF of Korea funded by Ministry of Education (2019R1A6A1A09031717) and in part by the Korean Research Fellowship Program through NRF of Korea, funded by Ministry of Science and ICT (2016H1D3A1938065).

References

[1] M. C. Tang, T. Shi, and R. W. Ziolkowski, “Electrically small broadside radiating huygens source antenna augmented with internal non-Foster elements to increase its bandwidth,” *IEEE Antennas Wirless Propag. Lett.*, vol. 16, pp . 712-715, Aug. 2016.

[2] A. Poggio and M. Mayes, “A unieque brodband dipole antenna design utilizing conjugate reactance loading,” *Proc. Propag. Soc. Int. Symp*, vol.7, pp . 250-258, Dec. 1969.

[3] S. Kolev, B. Delacressonniere, and J. L. Gautier, “Using a negative capacitance to increase the tuning range of a varactor diode in MMIC technology,” *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 12, pp. 2425–2430, Dec. 2001.

[4] J. Linvill, “Transistor negative-impedance converters,” *Proc. IRE*, vol. 41, no. 6, pp. 725–729, Jun. 1953.

[5] H. Mirzaei and G. V. Eleftheriades, “Realizing non-Foster reactive elements using negative group delay networks,” *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4322–4332, Dec. 2013.

[6] N. Au and C. Seo, “Novel design of a 2.1-2.9 GHz negative capacitance using a passive non-Foster circuit,” *IEICE Electron. Express* ***1*** (2017) 20160955.

[7] T. Zhang, R. Xu, and C. T. Michael Wu, “Unconditionally stable non-Foster element using active transversal-filter-based negative group delay circuit,” *IEEE Microwave Wireless Component Letters*, vol. 27, no. 10, pp. 921-923, Oct. 2017.

[8] M. Zhu and C. T. Michael Wu, “A tunable series negative capacitor using distributed amplifer-based reconfigurable negative group delay circuit,” *Proc. of 48th European Microwave Conference*, pp. 616-619, 2018.

[9] M. Zhu and C. T. Michael Wu, “A tunable non-Foster T-network loaded transmission line using distributed amplifier based reconfigurable negative group delay circuit,” *Proc. of Asia Pacific Microwave Conference*, pp. 720-722, 2018.