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S1-10 - Power Dividers and Diplexers

1. **Three-Way Substrate-Integrated Waveguide Filtering Power Divider With In-Phase and Anti-Phase Outputs**

15:00 - 15:20 Hong-Wen Qian[1], Yi-Hsin Pang[1], 1 - National University of Kaohsiung

2. **600-GHz-Band Frequency-Division Multiplexing Communication With Silicon Unclad Diplexer**

15:20 - 15:40 Norihiko Shibata[1], Yuta Uemura[1], Yuma Kawamoto[1], Li Yi[1], Masayuki Fujita[1], Tadao Nagatsuma[1], 1 - Osaka University

3. **Design of Semi-Lumped-Element Power Divider With Arbitrary Three Matching Frequencies**

15:40 - 16:00 Ayumu Tsuchiya[1], Tadashi Kawai[1], Akira Enokihara[1], 1 - University of Hyogo

4. **Design of a Four-Frequency Channel Power Division Multiplexer**

16:00 - 16:20 Kuo-Lun Sun[1], Kai-Jie Xu[1], Pu-Hua Deng[1], 1 - National University of Kaohsiung

5. **Group Delay Analysis Approach for Quasi-Reflectionless Power Divider With Flat Phase Difference**

16:20 - 16:40 Girdhari Chaudhary[1], Daehan Lee[1], Yongchae Jeong[2], 1 - Jeonbuk National University, 2 - Chonbuk National University

Group Delay Analysis Approach for Quasi-Reflectionless Power Divider With Flat Phase Difference

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***Abstract*— In this paper, we present a group delay (GD) analysis approach for designing a quasi-reflectionless filtering power divider with arbitrary prescribed flat phase difference. The proposed quasi-reflectionless filtering power divider consists of Wilkinson divider, coupled lines and series resistor connected open-circuited stubs. To achieve flat phase difference, GD should be same through both output ports of power divider. In addition, arbitrarily prescribed GD flatness and phase difference flatness are controlled by series connected resistors. The proposed design method is validated through experimental results by fabricating quasi-reflectionless power divider with 90° phase difference at center frequency of 3.50 GHz. The measurement results are consistent with simulation and theoretical predicted results.**

Keywords—Coupled line, flat phase difference, group delay approach, phased array, quasi-reflectionless.

I. Introduction

Power dividers with arbitrary flat phase difference are indispensable components for phased array antennas, beamforming networks, and antenna feeding networks for modern wireless communication [1]. Conventional filtering power dividers have a reflective nature in stopband, which means all signals at stopband are reflected at input terminal [2]. In recent years, reflectionless filtering power dividers have become attractive to prevent interblock signal interference from unwanted RF signal power reflections and improve the stability of adjacent RF active circuits in RF front-end [3]- [6]. In [5], quasi-reflectionless filtering power divider was designed by using a resistively bandstop branch at input terminal. Similarly, a reflectionless filtering power divider was designed by combining two signals in two paths without producing signals reflected back to both paths [6]. Despite of significant research, conventional reflection-less filtering power dividers have in-phase (0°) difference between output ports. Nevertheless, previously reported reflectionless power dividers were lacking analysis of arbitrary prescribed flat phase difference and group delay (GD), which is crucial for phased array antenna systems [7], [8].

In this paper, we propose a quasi-reflectionless filtering power divider with arbitrary prescribed flat phase difference and GD. An analytical design method has been developed by using GD analysis approach. The quasi-reflectionless filtering response is achieved by controlling coupled line sections and series resistor connected stubs.

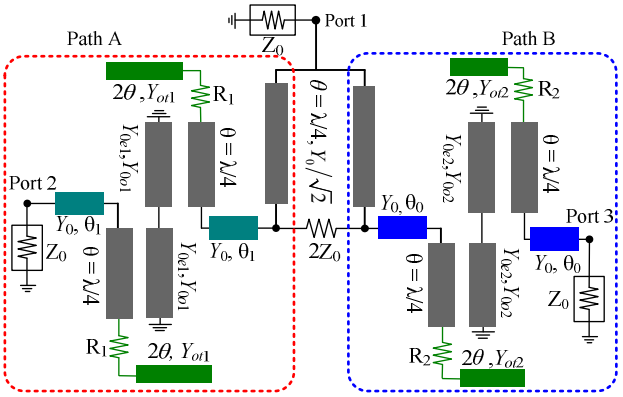


Fig. 1. Proposed structure of quasi-reflectionless filtering power divider with arbitrary prescribed flat phase difference.

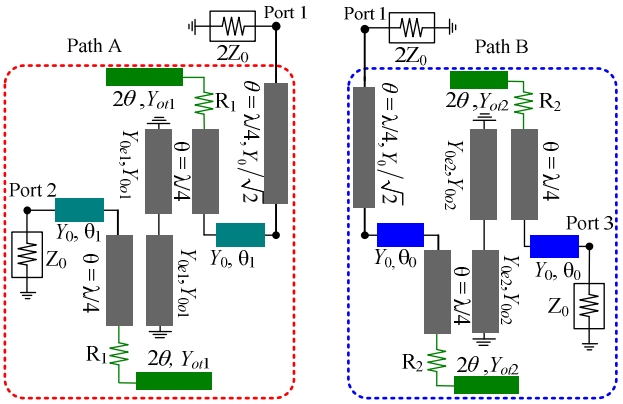


Fig. 2. Equivalent circuit under even-mode excitation between :(a) port 1 and 2 and (b) port 1 and 3.

II. Analytical Analysis

Fig. 1 shows the proposed structure of quasi-reflectionless filtering power divider, which consists of Wilkinson divider and $\lambda/4$ coupled lines terminated with series resistor connected $\lambda/2$ open-circuited stubs. Since the structure is symmetrical, even- and odd-mode analysis can be applied to derive *S*-parameters [8]. Fig. 2 shows the equivalent sub-networks path A and path B during signal transmission between port 1 and 2 and port 1 and 3. The phase difference between path A (port 1 and 2) and path B (port 1 and 3) is expressed as (1).

$$\Delta\varphi = \angle S_{21} - \angle S_{31} = 2\left(\theta_1 - \theta_0\right) \tag{1}$$

Using phase of S_{21} and S_{31}, the GDs between path A and path B at center frequency (f_0) are derived as (2).

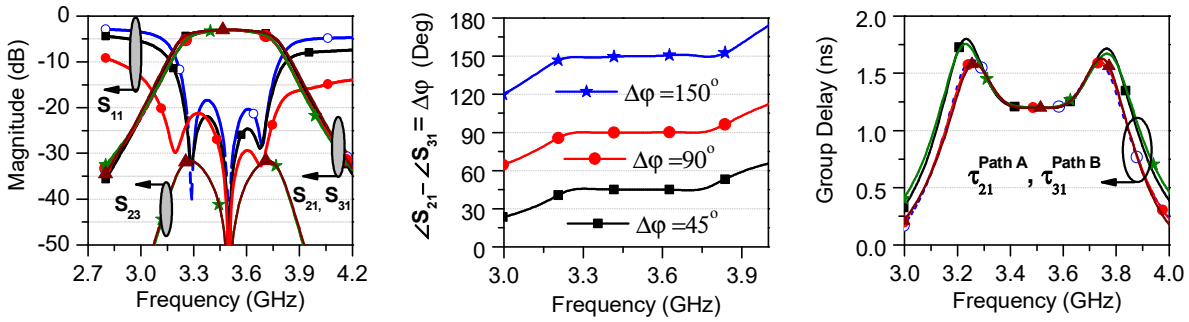


Fig. 3. Simulated results of quasi-reflectionless power divider with flat phase difference and group delay of 1.20 ns at f_0 = 3.50 GHz.

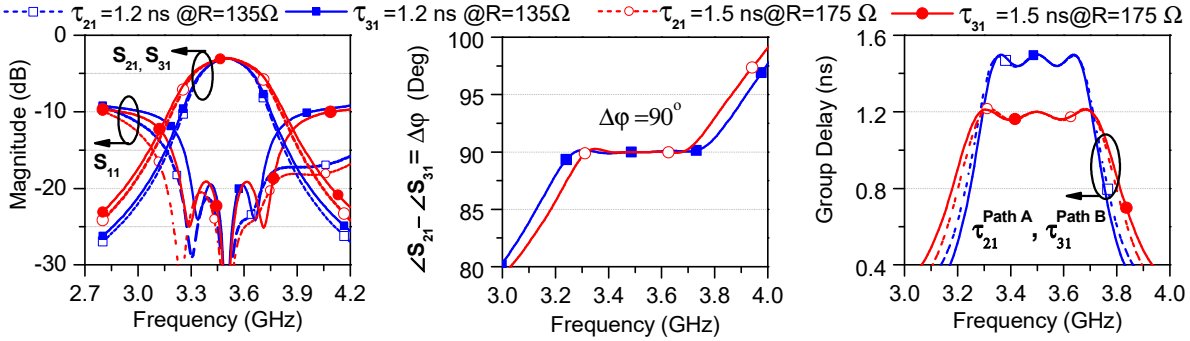


Fig. 4. Simulated results of quasi-reflectionless differential phase shifter with a phase difference of 90° and different arbitrarily prescribed group delays.

Table I: Circuit parameters for different phase difference (Refer to Fig. 3)

$Z_{ot1} = Z_{ot2}$ = 50 Ω and GD = 1.2 ns at f_0 = 3.50 GHz					
Branch	$\Delta\varphi$	Z_{0ei} (Ω)	Z_{0oi} (Ω)	R_i (Ω)	θ_i
Path A		133.65	73.28	30	45°
Path B	150°	117.05	62.75	75	120°
	90°	129.16	68.98	30	90°
	45°	134.54	72.13	30	67.5°

$$\tau\big|_{f=f_0}^{\text{Path A}} = \frac{a_1 Y_{0o1}^3 + Y_{0o1}c_1 + d_1}{4 f_0 b_1 Y_{0o1}^2} + \frac{\theta_1}{\pi f_0} + \frac{3}{8\sqrt{2} f_0} \quad (2a)$$

$$\tau\big|_{f=f_0}^{\text{Path B}} = \frac{a_2 Y_{0o2}^3 + Y_{0o2}c_2 + d_2}{4 f_0 b_2 Y_{0o2}^2} + \frac{\theta_0}{\pi f_0} + \frac{3}{8\sqrt{2} f_0}, \quad (2b)$$

where

$$a_1 = \frac{1-k_1^2}{Y_0^2(1+k_1)^3},\ b_1 = \frac{k_1^2}{Y_0(1+k_1)^2} \quad (3a)$$

$$c_1 = \frac{k_1^2}{1+k_1}, d_1 = 2k_1^2 Y_{ot1}, Y_{0e1} = \frac{1-k_1}{1+k_1} Y_{0o1} \quad (3b)$$

$$a_2 = \frac{1-k_2^2}{Y_0^2(1+k_2)^3},\ b_2 = \frac{k_2^2}{Y_0(1+k_2)^2} \quad (3c)$$

$$c_2 = \frac{k_2^2}{1+k_2}, d_2 = 2k_2^2 Y_{ot2}, Y_{0e2} = \frac{1-k_2}{1+k_2} Y_{0o2} \quad (3d)$$

Using equations (2), the Y_{0o1} and Y_{0o2} in terms of specified GD at f_0 can be derived as (4).

$$a_1 Y_{0o1}^3 - 4 f_0 b_1 \left(\tau\big|_{f=f_0}^{\text{Path A}} - \frac{\theta_1}{\pi f_0} - \frac{3}{8\sqrt{2} f_0} \right) Y_{0o1}^2 + Y_{0o1}c_1 + d_1 = 0 \quad (4a)$$

$$a_2 Y_{0o2}^3 - 4 f_0 b_2 \left(\tau\big|_{f=f_0}^{\text{Path B}} - \frac{\theta_0}{\pi f_0} - \frac{3}{8\sqrt{2} f_0} \right) Y_{0o2}^2 + Y_{0o2}c_2 + d_2 = 0 \quad (4b)$$

Table II: Circuit parameters for flat group delay (Refer to Fig. 4)

$Z_{ot1} = Z_{ot2}$ = 50 Ω, f_0 = 3.50 GHz					
Branch	$\Delta\varphi/\tau$ (ns)	Z_{0ei} (Ω)	Z_{0oi} (Ω)	R_i (Ω)	θ_i
Path A	90°/1.2	133.65	73.28	135	45°
Path B		129.16	68.98		90°
Path A	90°/1.5	143.12	87.22	175	45°
Path B		139.65	83.57		90°

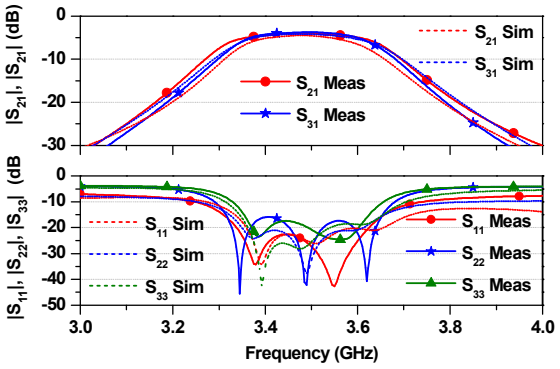
To achieve flat phase difference, the GDs of path A and path B should be chosen identical. The optimum circuit parameters of proposed circuit can be obtained by solving 4(a) and 4(b). As noted from 4(a) and 4(b), Y_{0o1} and Y_{0o2} have three roots and one of these roots is the optimum circuit parameter.

For validation of the analytical design equations, Fig. 3 depicts the simulation of proposed quasi-reflectionless filtering power divider with arbitrary prescribed flat phase difference. The circuit parameters are shown in Table I. In this design example, GDs of path A and path B are selected as 1.20 ns at f_0 =3.50 GHz. The flat phase difference of 45°, 90° and 150° are achieved within passband frequency. In addition, GD at f_0 remains same although phase difference is changed from 45° to 150°.

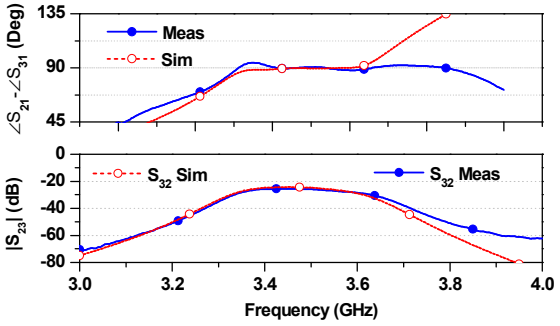
Fig. 4 depicts the simulation results demonstrating the arbitrary prescribed flat GD. The GD flatness and phase difference flatness are controlled by series connected resistor. In addition, flat phase difference bandwidth is slightly enhanced if GD is chosen smaller value.

III. Simulation And Measurement Results

For experimental validation, a $\Delta\varphi$ = 90° quasi-reflectionless filtering power divider with GD of 2 ns at f_0 = 3.5 GHz was designed and fabricated on Taconic substrate with dielectric constant of 2.20 and thickness of 0.787 mm. The circuit parameters of are given as: $Z_{0e1} = 1/Y_{0e1}$ = 119.38 Ω, $Z_{0o1} = 1/Y_{0o1}$ = 74.03 Ω, $Z_{ot1} = 1/Y_{ot1}$ = 25 Ω, R_1 = 30 Ω, θ_1 = 90°, $Z_{0e2} = 1/Y_{0e2}$ = 119.96 Ω, $Z_{0o2} = 1/Y_{0o2}$ = 75.66 Ω, $Z_{ot2} = 1/Y_{ot2}$ = 25 Ω, R_2 = 50 Ω, θ_0 = 45°.



(a)



(b)

Fig. 5. Simulation and measurement results: (a) S-parameters and (b) phase difference/isolation between output ports.

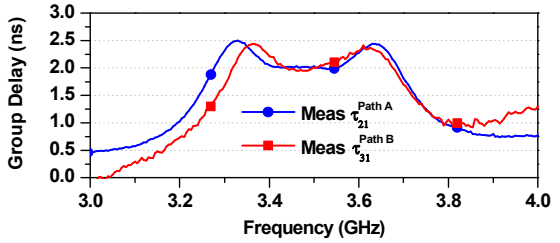


Fig. 6. Measured group delay between path A and path B.

Fig. 5 shows the simulation and measurement results of fabricated circuit. The measurement results are consistent with the simulation. In experiment, the magnitude of $|S_{21}|$ and $|S_{31}|$ are determined to be -3.97 dB and -3.76 dB at f_0 = 3.50 GHz. Similarly, $|S_{11}|$, $|S_{22}|$, and $|S_{33}|$ are higher than -28.75 dB, -27.27 dB and -20.77 dB at f_0 and higher than 5 dB at all frequencies. The phase difference between output ports is 91.05 ± 3.2^{o} from 3.3 GHz to 3.82 GHz (520 MHz). Likewise, isolation between output ports ($|S_{23}|$) is 23 dB. Fig. 6 shows the measured GD response of path A and path B. The GDs of path A and B are 2.02 ns and 1.98 ns at f_0.

IV. Conclusion

This paper demonstrated the quasi-reflectionless filtering power divider with arbitrarily prescribed group delay and flat phase difference. The proposed filtering power divider achieves flat phase difference within passband and quasi-reflectionless characteristics. The flat phase difference is achieved by equating the group delay of path A and path B. The passband group delay flatness as well as differential phase shift flatness can be controlled by series connected resistor. The proposed quasi-reflectionless filtering power divider with arbitrarily prescribed group delay and flat phase difference is applicable to MIMO phased array antenna to reduce beam squint caused by group delay and phased mismatching.

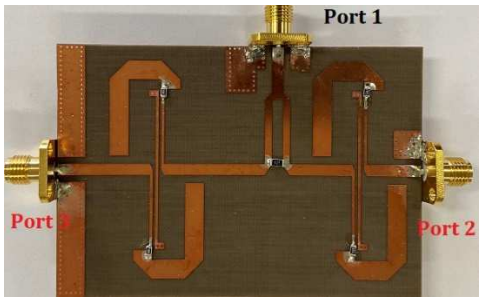


Fig. 7. Photograph of fabricated quasi-reflectionless power divider.

Acknowledgment

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References

[1] H. R. Fang, X. Tang, K. Mouthaan, and R. Guinvarch, "Two-octave digital all-pass phase shifters for phased array applications," *in Proc. IEEE Radio Wireless Symp. (RWW)*, pp. 169–171, Jan. 2013.

[2] Y. Lyu, Z. Zhu, and C. H. Cheng, "A new design of filtering power divider with arbitrary constant phase difference, impedance transformation and good isolation," *IEEE Access*, vol. 7, pp. 169495-169507, Nov. 2019.

[3] B. Mini-Circuits, "Reflectionless filters improve linearity and dynamic range," *Microwave Journal*, vol. 58, no. 8, pp. 42–50, Aug. 2015.

[4] R. Gomez-Garcia, D. Psychogiou, J. Munoz-Ferreras, and L. Yang, "Avoiding RF isolators: reflectionless microwave bandpass filtering components for advanced RF front-ends," *IEEE Microwave Magazine*, vol. 21, no. 12, pp. 68-88, Dec. 2020.

[5] R. Gomez-Garcia, J. M. Munoz-Ferreras, and D. Psychogiou, "RF reflectionless filtering power dividers," *IEEE Trans. Circuits Syst. II*, Exp. Briefs, vol. 66, no. 6, pp. 933–937, Jun. 2019.

[6] B. Lee, S. Nam, and J. Lee, "Filtering power divider with reflectionless response and wide isolation at output ports," *IEEE Trans. Microwave theory Techn*., vol. 67, no. 7, pp. 2684-2692, July 2019.

[7] G. Chaudhary and Y. Jeong, "Arbitrary prescribed wideband flat group delay circuits using coupled lines," *IEEE Trans. Microwave Theory Techn*., vol. 66, no. 4, pp. 1885-1894, Apr. 2018.

[8] G. Chaudhary and Y. Jeong, "Arbitrary prescribed flat wideband group delay absorptive microstrip bandpass filters", *IEEE Trans. Microwave Theory Techn*., vol. 69, no. 2, pp. 1404-1414, Feb. 2021.