A Novel Frequency Doubler Using Feedforward Technique and Defected Ground Structure

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***Abstract*—A novel design of frequency doubler using feedforward technique and defected ground structure (DGS) is proposed. The feedforward loop in the proposed frequency doubler suppresses the fundamental component (f_o), and the DGS diminishes the higher order harmonics such as third, fourth, and so on. Due to the combination of feedforward structure and DGS, only the doubled frequency component ($2f_o$) appears at the output port and the other unwanted components are suppressed excellently. A frequency doubler is designed at 1.85 GHz of f_o by the proposed technique and measured. The measured output power of $2f_o$ is -3 dBm when the input power is 0 dBm. The obtained suppression of f_o, $3f_o$, and $4f_o$ are 42.9, 19.2, and 29.7 dB, respectively.**

***Index Terms*—Defected ground structure (DGS), feedforward, frequency doubler, harmonic suppression.**

I. Introduction

DEMANDS for the signal source with high stability and low phase noise increase in microwave, millimeter-wave communication and radar systems. High frequency signal sources can be easily obtained by multiplying low frequency signal that has relatively high stability and low phase noise. However, in general, frequency multipliers include the unwanted fundamental and harmonic frequency components. When a multiplier operates with other microwave circuits such as mixer, amplifier, and so on, serious problems may occur due to the undesirable frequency components. In order to suppress the fundamental frequency component (f_o), quarter-wavelength open stub or balanced multiplier structure is adopted. But these methods have the limitation of suppression only to 25 dB generally[1], [2]. A balanced frequency doubler using input balun can be used to cancel fundamental. But the cancellation characteristics depend on the unbalance phase property of balun and uniformity of transistors. Typically 20 dB fundamental rejection at microwave frequency is obtained [3]. Another way to diminish the fundamental and unwanted harmonic components is to use band pass filters. But the insertion loss of the band pass filter causes multiplied signal to be less than the required signal level. In addition, it is not easy to make high Q-factor band-pass filter in monolithic microwave integrated circuit, fully monolithic frequency doubler design is very difficult.

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In this letter, a novel frequency doubler that suppresses fundamental and unwanted higher-order harmonic components is proposed. The proposed doubler is composed of the feedforward structure, which is widely used in linear power amplifiers, and defected ground structure (DGS) realized by etching a few dumb-bell shaped patterns on the ground plane of microstrip line [4]. Several applications using DGS to design a coupler, filter, and power amplifier have been already presented [5]–[7]. The feedforward loop suppresses f_o signal and DGS cut down the other unwanted harmonic components effectively than previous method.

II. Theory

The output current waveform to input voltage of transistors can be explained according to bias condition or conduction angle. The dc current consumption and harmonic signals to the bias are estimated by using averaging and correlation between drain (or collector) current and nth harmonic as shown in (1) and (2), where α is the conduction angle of input signal and $I_{\max}$ is the maximum allowable current [8]. The amplitude of the second harmonic is maximum when α is around 120°. Therefore, the bias point for frequency doubler should be selected in the vicinity of pinch-off, between class B and C. Once the bias is determined, the input and output ports have to be matched for fundamental (f_o) and the second harmonic signal ($2f_o$), respectively, to maximize the $2f_o$ output

$$I_n = \frac{1}{\pi}\int_{a/2}^{a/2} \frac{I_{\max}}{1-\cos\frac{\alpha}{2}}\left(\cos\omega t - \cos\frac{\alpha}{2}\right)\cos n\omega t d\omega t \quad (1)$$

$$I_{dc} = \frac{1}{2\pi}\frac{I_{\max}}{1-\cos\frac{\alpha}{2}}\left(2\sin\frac{\alpha}{2} - \cos\frac{\alpha}{2}\right). \quad (2)$$

Fig. 1 is the proposed frequency doubler, which adopts the feedforward structure to suppress f_o and DGS microstrip line to diminish the other higher-order harmonics. The feedforward structure is widely used to remove the intermodulation distortion in power amplifiers. It has wide operating frequency band and hardly oscillates because there is no feedback path. In this letter, the first loop of feedforward structure is used for suppressing f_o. Because active multipliers attenuate f_o theoretically, f_o can be more suppressed by adjusting the coupling coefficient of the couplers, which are located before and after the multiplier, and phase of the variable phase shifter [9]. To perfect f_o cancellation, the magnitude and phase of f_o are equal and out-of-phased at output coupler of feedforward structure. So coupling coefficients of input and output coupler is adjusted

to match magnitude and the phase of variable phase shifter is adjusted to out-of-phase match between two paths.

The DGS pattern under the microstrip line produces the additional equivalent inductance and increased characteristic impedance. In conventional microstrip lines, the line width is getting extremely narrower as the required line impedance increases. However, in the microstrip line with DGS, the line width is broader than that of the standard microstrip line for the same characteristic impedance because the additional inductance results in the highly increased characteristic impedance. The broadened width of the DGS microstrip line can be understood as the increased equivalent capacitance, which plays a great role in raising the phase constant and slow-wave effects [7]. In this work, the DGS microstrip line is used to suppress the higher-order harmonics over the third.

Fig. 2 shows the layouts of a standard microstrip line and DGS microstrip line. The substrate is RT/duroid 5880 with the dielectric constant of 2.2 and thickness of 31 mils. The DGS cell dimensions are; $a = 4$ mm, $b = 3.5$ mm, $d = 9.3$ mm, $g = 0.5$ mm, $w = 2.38$ mm, and $w_{\rm dgs} = 4.37$ mm. By adjusting the DGS cell parameters, it is possible to control the electrical characteristics.

Fig. 3 shows the measured S_{11} and S_{21} of the DGS microstrip line. The DGS microstrip line has characteristics that are just like those of low pass filters. The cut-off frequency is around 4 GHz, the insertion loss is the 0.4 dB at 3.74 GHz, and the attenuation value at 5.55 GHz is more than 23 dB.

III. Experiment and Measured Results

In order to show the validity of the proposed doubler, we have designed a frequency doubler that multiplies 1.87 GHz of fundamental signal to produce the frequency output at 3.74 GHz. The selected transistor is ATF10136 MESFET. The drain and gate bias voltages are set to 1.2 V and -1.25 V, respectively, for the operation near pinch-off voltage region, between class B and C. The matching points for input and output networks were determined by using the load-pull method and implemented by simulation on Agilent ADS.

Fig. 4 shows the measured output spectrum of the conventional single-ended frequency doubler. The spectra of the conventional doubler show the $2f_o$ output signal as well as the fairly large f_o and other higher-order harmonics. It has the conversion loss of 2.55 dB and fundamental suppression of -25.94 dB when the input signal is 0 dBm. Fig. 5 shows the measured data of the frequency doubler taking the feedforward Structure only without DGS. The measured fundamental suppression is 42.2 dB.

Fig. 6 illustrates the measured output spectrum of the proposed frequency doubler including the feedforward structure and DGS microstrip line, where the proposed frequency doubler is fabricated the same PCB. For the same input power, the output power of $2f_o$ is -3 dBm with the suppression of 42.9, 19.2, and 29.7 dB of f_o, $3f_o$, and $4f_o$, respectively. Table I summarizes output spectrum characteristics of several frequency doubler structures. The measured phase noise of the output signal $(2f_o)$ is 97.51 dBc/Hz (at 10-KHz offset) for that of input signal -101.3 dB, which is better than the theoretical

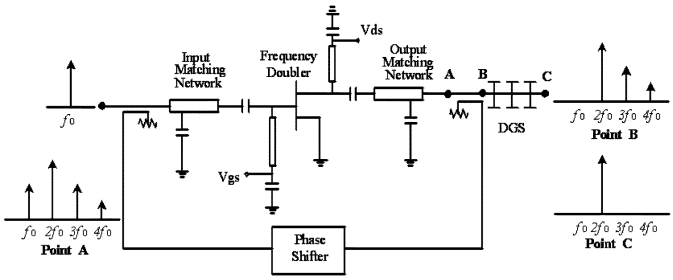

Fig. 1. Block diagram of the proposed frequency doubler using feedforward structure and DGS microstrip line.

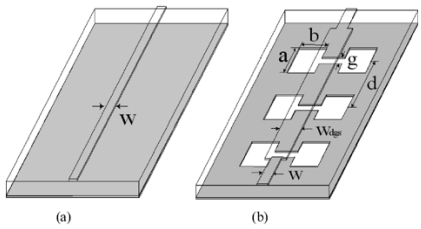

Fig. 2. Layouts of a (a) standard microstrip line and (b) DGS microstrip line.

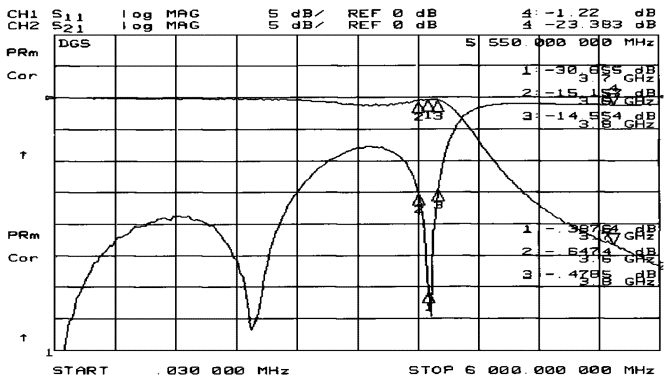

Fig. 3. Measured characteristics of the DGS microstrip line.

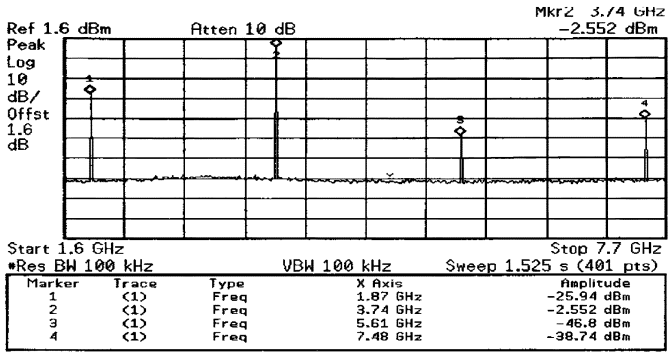

Fig. 4. Measured spectrum of the conventional frequency doubler.

phase degradation condition expressed by $20\log(2) = 6$ dB, by 2.2 dB. It is believed that this result is due to the clear elimination of the fundamental signal and higher-order harmonic signals. DGS microstrip line is operated as harmonic short. So the phase noise of the proposed frequency doubler is improved than the conventional.

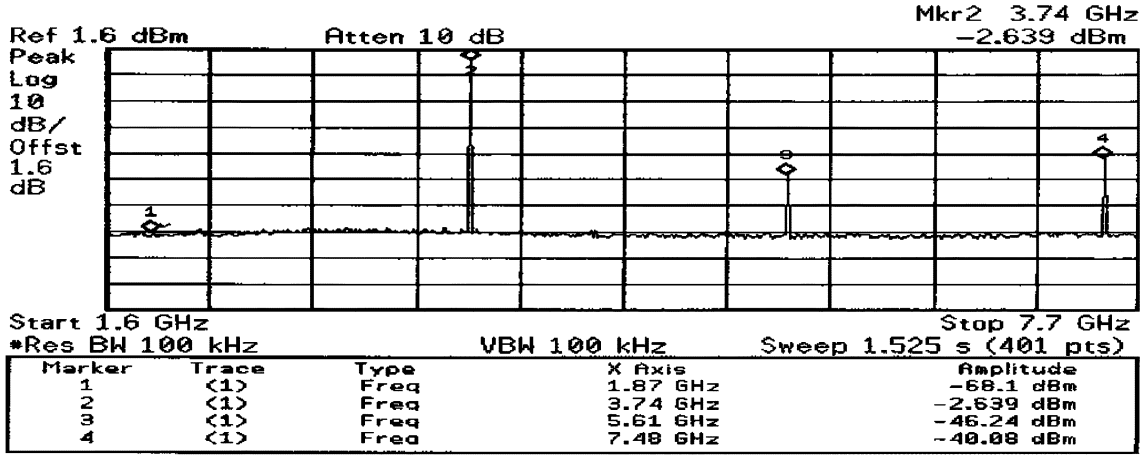

Fig. 5. Measured spectrum of the frequency doubler having the feedforward structure only.

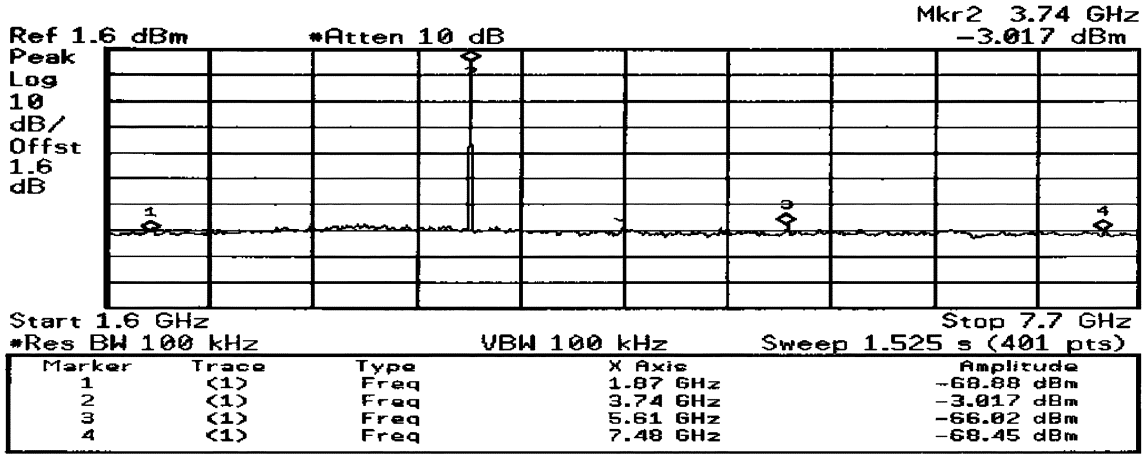

Fig. 6. Measured spectrum of the proposed frequency doubler having the feedforward structure and DGS microstrip line.

TABLE I
OUTPUT SIGNALS COMPARISON OF FREQUENCY DOUBLER STRUCTURES [dBm]

	P_{fo}	P_{2fo}	P_{3fo}	P_{4fo}
Only Doubler	-25.94	-2.55	-46.8	-38.74
FF + Doubler	-68.1	-2.64	-46.24	-40.08
FF+DGS+Doubler	-68.88	-3.02	-66.02	-68.45

IV. CONCLUSION

The new design technique for frequency doubler was proposed to obtain signal sources that have high stability and low phase noise. The fundamental frequency signal was excellently suppressed by using feedforward structure, and the unwanted higher-order harmonics were removed due to the DGS structure. The measured suppressions of the fundamental, third, and fourth harmonic components were 42.9, 19.2, and 29.7 dB, respectively. It is believed that the proposed frequency doubler can be integrated in monolithic integrated circuits form because the fabricated frequency doubler consists of a transistor, diodes, and hybrid circuit elements. It is also expected that the proposed frequency doubler have a great contribution to improve the quality of communication without high Q band-pass filters.

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