A New Design of Doherty Amplifiers Using Defected Ground Structure

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***Abstract*—In this letter, a new Doherty power amplifier having the ideal harmonic termination condition that has been usually ignored is proposed. A defected ground structure (DGS) is adopted on the ground pattern of the output $\lambda/4$ impedance inverter of the carrier amplifier and output offset transmission line of the peaking amplifier that are essential for proper load modulation operation of a conventional Doherty amplifier. As a result of the second and third harmonic termination, excellent improvement in power added efficiency (PAE), gain, maximum output power as well as linearity is obtained. The acquired improvements in gain, maximum output power ($P_{1\,\mathrm{dB}}$), PAE, and adjacent channel leakage ratio to wideband code division multiple access 2FA signal are 0.33 dB, 0.42 dB, 12.7%, and 5.1 dB, respectively. Moreover, physical length of microstrip line is shortened fairly by DGS, therefore the whole amplifier circuit size is considerably reduced.**

***Index Terms*—Defected ground structure (DGS), DGS Doherty amplifier (DDA), Doherty amplifier, linearity, power added efficiency (PAE).**

I. Introduction

DOHERTY amplifier is one of the most representative ways of power added efficiency (PAE) enhancement, and extensive research has been done on it. The key concept of Doherty amplifier is obtaining maximum efficiency over a 6-dB dynamic range using load modulation [1].

The design method for optimum output load-pull operation in conventional Doherty amplifiers (CDAs) has been reported in [2] by simply assuming the ideal harmonic termination of an active load–pull operation, so that a fundamental component could be only concerned for PAE. Since the sub-amplifiers in CDA are usually operating in nonlinear bias conditions, a lot of harmonic components arise. So the harmonic termination must be considered for the improvement of PAE and linearity. In addition, some previous works showed that the termination of the harmonic components plays a positive role in improving the maximum output power, PAE, and linearity [3], [4].

In this work, we propose a new design method for defected ground structure (DGS) Doherty amplifier (DDA) having ideal harmonic termination. At first, we explain the design and measurement of a DGS microstrip line ("DGS line"). Secondly, we show the improved output powers of the carrier and the peaking amplifier due to the DGS line. Finally, the comparison betweeen the CDA and DDA are discussed in terms of power gain, $P_{1\,\mathrm{dB}}$, PAE, and adjacent channel leakage ratio (ACLR) characteristic.

Manuscript received May 3, 2006; revised July 4, 2006. This paper was supported in part by the CBNU Funds for Overseas Research, 2006 under Contract OR-2006-4.

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Digital Object Identifier 10.1109/LMWC.2006.885636

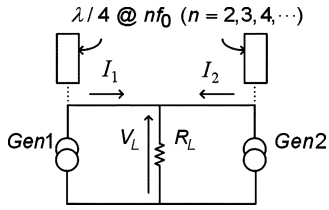


Fig. 1. Active load–pull circuit considering ideal harmonic termination.

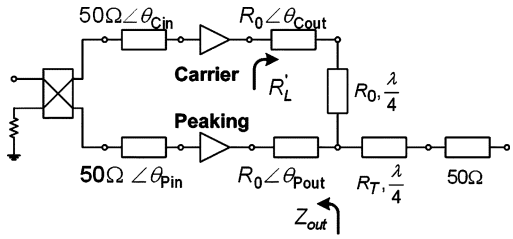


Fig. 2. Conventional Doherty amplifier.

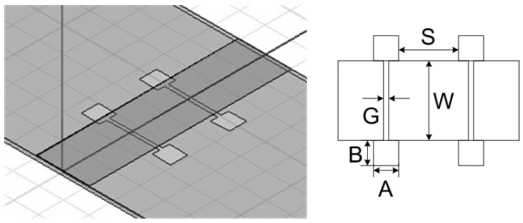
II. Design of DGS Doherty Amplifier

A. Active Load–Pull Method With Ideal Harmonic Termination

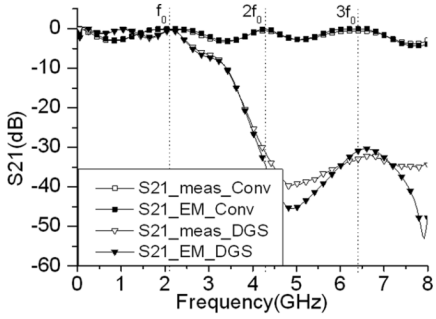
Fig. 1 shows an active load–pull circuit considering ideal harmonic termination. Active load–pull technique is based on the concept that the impedance of a radio frequency (RF) load seen by the first signal source $(Gen1)$ can be modified by applying the second signal source $(Gen2)$. In other words, the input resistance (R_1) seen by $Gen1$ can be controlled by changing currents I_1 and I_2.

An ideal harmonic termination condition should be satisfied in performing an active load-pull analysis, so the fundamental current is taken into consideration only. Previous studies assumed a weakly nonlinear case, therefore higher order harmonics were not considered. However, the amount of higher order harmonic components is significant because the peaking amplifier is usually operated deeply into class C.

Fig. 2 shows the block diagram of the CDA. CDA consists of carrier and peaking amplifier, $\lambda/4$ impedance transformer, offset transmission line, and input power divider. At higher output power range, both amplifiers operate and the load impedances are R_0, respectively. However, at lower output power range, only the carrier amplifier operates and peaking amplifier is in the off-state. At this time, usually Z_{out} of the peaking



(a)



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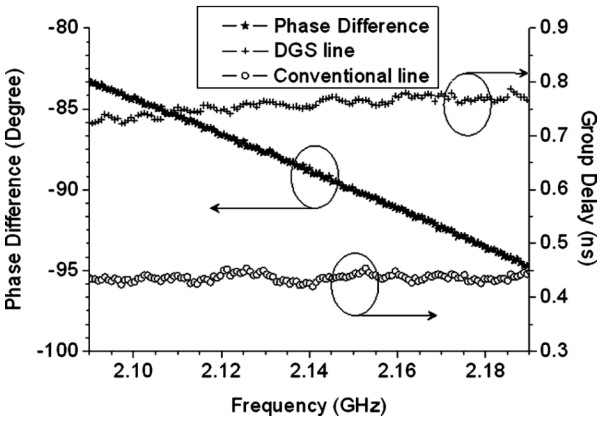


(c)

Fig. 3. (a) Geometry of the DGS line. (b) Transmission characteristic comparison at 0.5∼8 GHz. (c) Slow-wave effect of the DGS line.

amplifier is not open due to the parasitic components inside the amplifier. Therefore we need an offset transmission line $(\theta_{\rm Pout})$ to make $Z_{\rm out}$ of the peaking amplifier open at the output power combining point. Moreover, $\lambda/4$ impedance transformer with offset transmission line $(\theta_{\rm Cout})$ is essential for load impedance of the carrier amplifier to be 2_{R0} [5].

B. DGS Low Pass Transmission Line

We designed the DGS line using a dumbbell shaped DGS to obtain higher order harmonic termination condition [6]. The DGS line has to maintain low insertion loss and a good reflection characteristic at the fundamental frequency as it should be placed at the output of the power amplifier (PA).

Fig. 3(a) shows the geometry of the proposed DGS line of which the characteristic impedance is 16 Ω, implemented on the substrate with $\varepsilon_r = 2.2$ and $h = 31$ mil ($A = 3.4$ mm, $B = 3.6$ mm, $G = 0.7$ mm, $S = 8$ mm, $W = 10.46$ mm). The load resistance of amplifiers is matched to 16 Ω for the maximum output power, so the characteristic impedance of the

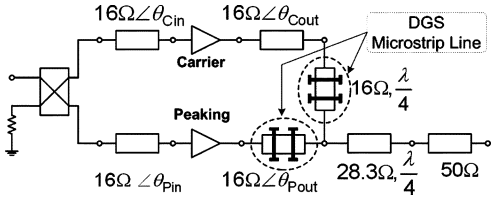


Fig. 4. Proposed DGS Doherty amplifier.

DGS line is 16 Ω. Fig. 3(b) shows the high frequency simulator system (HFSS) simulation and the measurement for the transmission characteristic comparison of the DGS line with the conventional line. Due to the characteristic impedance of 16 Ω, additional 28.28-Ω $\lambda/4$ transformers are used at the input and output of the 16-Ω line for matching to the 50 Ω measurement system. Excluding 0.1-dB insertion loss at the input and output $\lambda/4$ transformers, actual insertion loss of the 16-Ω DGS line would be 0.13 dB. It is noted that the measured suppression of the DGS line is more than 31 dB at the second and third harmonic frequencies. Slow-wave effect is also shown in Fig. 3(c). For the same physical length, the DGS line has electrical length and group delay time of 89.5° and 0.3 ns longer than that of the conventional line, respectively. That is the basis of the considerable size reduction of the DDA.

C. DGS Doherty Amplifier

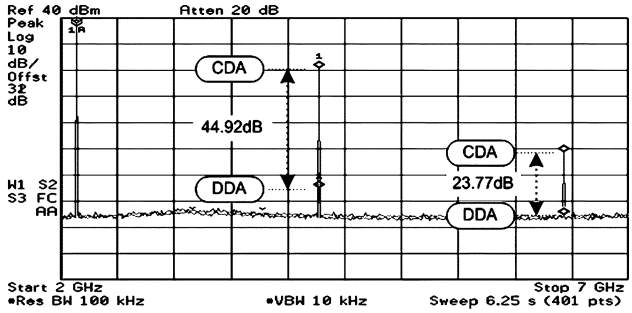
In order to verify the improved performances of the proposed DDA, the CDA and the DDA are designed for IMT-2000 basestation using a 4-W GaAs FET device. The carrier amplifier and peaking amplifier has a bias condition of class A ($I_{\rm DS} = 620$ mA) and class C ($V_{\rm GS} = -3.5$ V), respectively. The block diagram of the proposed DDA is shown in Fig. 4.

It is noted that no additional transmission line to apply DGS patterns has been inserted. We did just apply DGS unit on the ground pattern of the $\lambda/4$ impedance inverter that is essential for proper active load–pull mechanism. At the same time, we need an offset transmission line at the output of the peaking amplifier. In other words, DGS patterns are applied on the ground pattern of the output offset transmission line $(\theta_{\rm Pout})$ of the peaking amplifier.

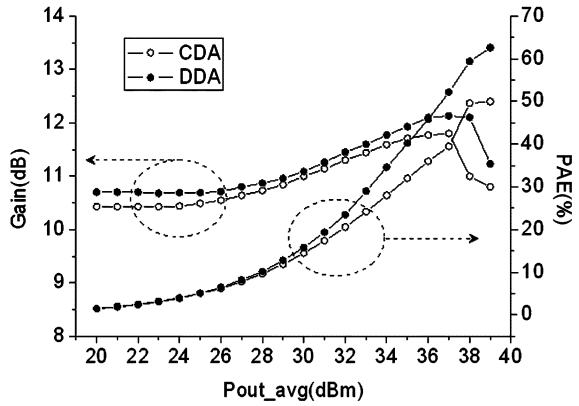
III. Measurement

The improved harmonic rejection characteristic of the DDA over the CDA is shown in Fig. 5(a). The second and third harmonic rejections are 44.92 dB and 23.77 dB (on the noise floor), respectively. Higher order harmonic termination leads to increase in gain, output power and PAE.

Fig. 5(b) shows the compared typical parameters between the CDA and DDA. Over the dynamic range, gain and $P_{1\,\rm dB}$ are increased about 0.33 dB and 0.42 dB, respectively. The maximum PAE of the DDA at P1 dB is 62.7%, a value about 12.7% higher than the CDA, and 10.4% higher than the conventional single ended GaAs FET amplifier. Fig. 5(c) and (d) shows the ACLR improvement for the wideband code division multiple access (WCDMA) 2FA signal. We obtained normally 5-dB ACLR improvement through the output dynamic range. Comparing the linearity of the CDA and DDA at the same output power level would be unreasonable since the maximum output power of the



(a)



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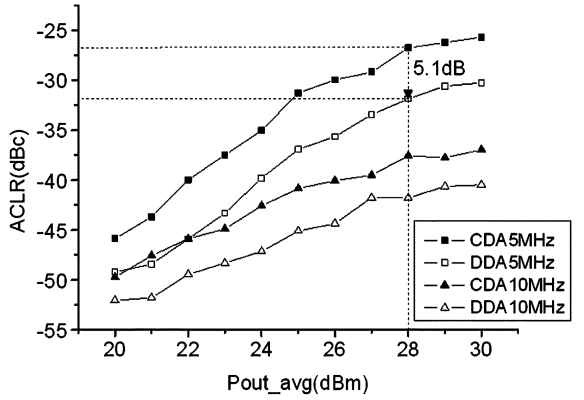

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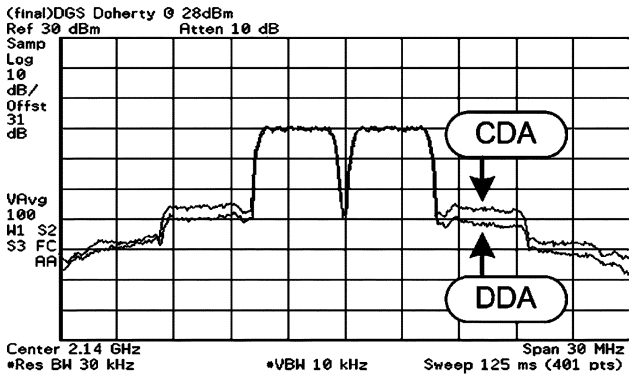

(d)

Fig. 5. (a) Harmonic suppression of DGS Doherty amplifier. (b) Gain, $P_{1\ \mathrm{dB}}$ and PAE improvement. (c) ACLR improvement for WCDMA 2FA. (d) Output spectrum ($@P\mathrm{out\_avg} = 28$ Bm).

DDA is slightly increased. However, we can conclude that the proposed method improved linearity since the ratio of the output power increase (0.42 dB) to the linearity improvement (about 5 dB) is small. The output spectrum is shown at the average output power of 28 dBm, 10 dB back-off from the $P_{1\ \mathrm{dB}}$.

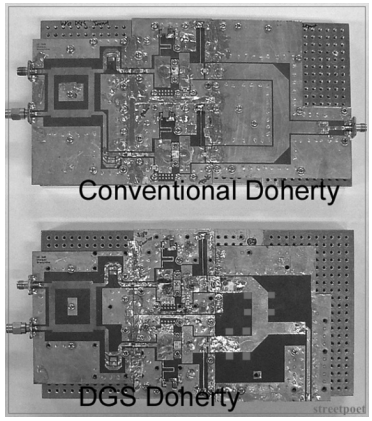

Fig. 6. Comparison of the whole circuit size of CDA and DDA.

The size reduction of the implemented DDA over the CDA is shown in Fig. 6. The ratios of the reduced lengths to the original ones are 71% (= 69 mm/96.96 mm) at the carrier amplifier output, and 62% (= 46.4 mm/74.86 mm) at the peaking amplifier output.

IV. Conclusion

In this letter, we proposed a new DDA having DGS microstrip line at the $\lambda/4$ impedance inverter of the carrier amplifier and output offset transmission line of the peaking amplifier. We could suppress higher order harmonics and reduce the circuit size effectively by the negligible insertion loss, excellent harmonic termination characteristic, and slow-wave effect. As a result of harmonic termination, a considerable improvement in PAE, ACLR, gain, and maximum output power have been achieved.

It is expected that the proposed design technique is well applicable to the conventional high power base-station Doherty amplifier to improve PAE, $P_{1\ \mathrm{dB}}$, and linearity without any additional lumped elements or transmission lines, while the total circuit size is reduced at the same time.

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