Design of Group Delay Time Controller Based on a Reflective Parallel Resonator

Girdhari Chaudhary, Heungjae Choi, Yongchae Jeong, Jongsik Lim, and Chul Dong Kim

In this paper, a group delay time controller (GDTC) is proposed based on a reflection topology employing a parallel resonator as the reflection termination. The design equations of the proposed GDTC have been derived and validated by simulation and experimental results. The group delay time can be varied by varying the capacitance and inductance at an operating frequency. To show the validity of the proposed circuit, an experiment was performed for a wideband code division multiple access downlink band operating at 2.11 GHz to 2.17 GHz. According to the experiment, a group delay time variation of 3±0.17 ns over bandwidth of 60 MHz with excellent flatness is obtained.

Keywords: Group delay time controller, resonance circuit, varactor diode, variable inductor.

I. Introduction

In mobile communications systems, transmitter performance is mainly limited by nonlinearity of power amplifiers (PAs). To improve the nonlinear performance of PAs, various types of linearization techniques, such as digital/analog predistortion, feedforward, direct/indirect feedback, polar loop, and Cartesian loop, have been proposed [1]-[4]. To achieve a broadband linearization of PAs, group delay (GD) time matching as well as amplitude and out-of-phase matching are very important design issues on the operating frequency band. A coaxial cable or GD bandpass filter is used as a GD time matching component in the conventional linear PAs. The GD time controller circuit is beneficial for linearization of PAs.

There have been several efforts to design GD time adjustor (GDTA) circuits [5]-[14]. In [5], the GD synthesizer circuit is based on a reflection topology employing resistance, inductance, and capacitance (RLC) series circuits in MMIC technology. The GD circuit presented in [6] changes the RF paths to obtain the different fixed GD times using RF switches. However, the microwave GDTA circuits presented in [7], [8] can control the GD time but have too narrow bandwidth, few MHz, and a large circuit size. The feedforward linear PA using the narrowband GDTA showed the benefit of the GDTA circuit in the design and operation of linear PA [9].

The variable GD line presented in [10] consists of a directional coupler with a periodic varactor load. The GD time can be controlled by changing the coupling coefficient of the coupler during the varactor loads adjustment. However, the GD variation is very slight and the time delay flatness is in need of improvement. Likewise, the circuit presented in [11] has a low GD tuning range and a narrow operating bandwidth.

The literature surveys show some effort to design CMOS

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variable GD lines [12], [13]. The approach discussed in [12] is based on a left-handed transmission line with cascaded metal-oxide semiconductor (MOS) varactors and shunt inductors.

The CMOS reflection-type variable GD line at a *K*-band presented in [13] consists of a 3-dB directional coupler and two-parallel resonator loads at through and coupled ports of the coupler. These circuits have demonstrated wideband operation but very short tuning (only a few picoseconds) range of GD time.

Several microwave circuits, such as phase shifter, attenuator, and amplifier, have been demonstrated using reflection topology [14]-[16].

In this paper, a group delay time controller (GDTC) based on the reflection topology employing parallel inductance and capacitance (LC) resonator circuits as the reflection termination is proposed to overcome the very narrow frequency bandwidth limitation of the previously presented GDTA circuits. The design equations of the proposed GDTC have been derived and have been validated through experimentation.

II. Design and Implementation

Figure 1 illustrates the port reduction method to derive the general design equation for the proposed GDTC circuit. By terminating the *m*-ports as a load network of (*n*+*m*)-ports, a new *S*-matrix of the reduced *n*-ports network can be obtained as

$$[S] = S'_{11} + S'_{12}\left[S_L^{-1} - S'_{22}\right]^{-1} S'_{21}, \quad (1)$$

where S_L is the *S*-matrix of a network when *m*-ports are terminated with loads, and S'_{ii} is the *S*-matrix of the (*n*+*m*)-ports network [17].

Figure 2 shows the proposed reflection type GDTC that consists of a 3-dB 90° hybrid coupler and LC parallel resonators as reflection termination. Since the through and the coupling ports of the hybrid coupler are terminated with parallel LC resonators, the S_L-matrix of the load network can be expressed as

$$[S_L] = \begin{bmatrix} \Gamma_{RP} & 0 \\ 0 & \Gamma_{RP} \end{bmatrix}, \quad (2)$$

where Γ_{RP} is the input reflection coefficient of the LC parallel resonator termination. Assuming the coupler to be lossless, perfectly matched, and having infinite isolation, the new reduced *S*-matrix of the proposed 2-port GDTC circuit is obtained with an *S*-matrix of a 4-port coupler and (2), which is given as

$$[S] = \begin{bmatrix} 0 & -j\Gamma_{RP} \\ -j\Gamma_{RP} & 0 \end{bmatrix}. \quad (3)$$

The input reflection coefficient of the LC parallel resonator termination can be expressed as

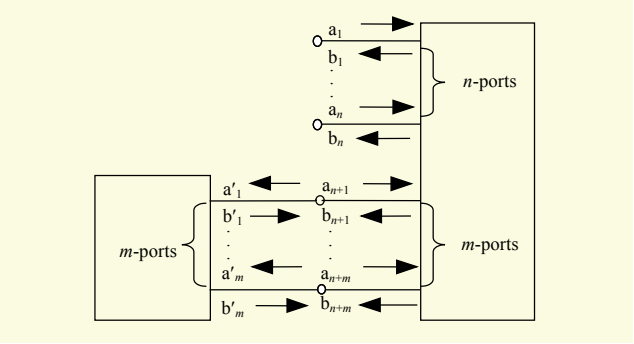

Fig. 1. Illustration of port-reduction method.

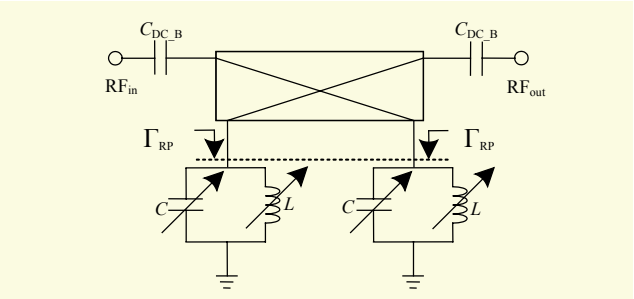

Fig. 2. Circuit diagram of proposed GDTC.

$$\Gamma_{RP} = \frac{(Y_0\omega L)^2 - (\omega^2 LC - 1)^2}{(Y_0\omega L)^2 + (\omega^2 LC - 1)^2} + j\frac{2Y_0\omega L(1-\omega^2 LC)}{(Y_0\omega L)^2 + (\omega^2 LC - 1)^2}, \quad (4)$$

where Y_0 is the termination admittance. Therefore, the transmission coefficient magnitude and phase of the proposed GDTC circuit are given as

$$|S_{21}| = \sqrt{\left(\frac{2Y_0\omega L(1-\omega^2 LC)}{(Y_0\omega L)^2 + (\omega^2 LC - 1)^2}\right)^2 + \left(\frac{(\omega^2 LC - 1) - (Y_0\omega L)^2}{(Y_0\omega L)^2 + (\omega^2 LC - 1)^2}\right)^2}, \quad (5)$$

$$\angle S_{21} = \tan^{-1}\left(\frac{(\omega^2 LC - 1)^2 - (Y_0\omega L)^2}{2Y_0\omega L(1-\omega^2 LC)}\right). \quad (6)$$

The GD gives a measure of how long it takes to traverse a system. Mathematically, it is defined as

$$\tau = -\frac{d\angle S_{21}}{d\omega}. \quad (7)$$

Therefore, the GD time of the proposed GDTC circuit is obtained using (6) and (7) as

$$\tau|_{\omega=\omega_0} = -\frac{d\angle S_{21}}{d\omega}\bigg|_{\omega=\omega_0} = \frac{4}{Y_0\omega_0^2 L} = 4Z_0 C, \quad (8)$$

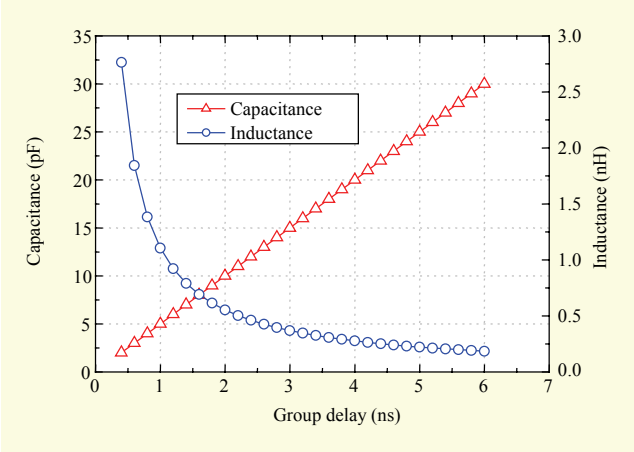

Fig. 3. Calculated value of capacitor and inductor for specific GD at 2.14 GHz.

where Z_0 is the termination impedance. From (8), the GD time variations can be obtained by varying the inductance and capacitance, assuming a resonance condition at the operating frequency.

Figure 3 shows the calculated capacitance and inductance to obtain specific GD times at the operating frequency. As shown in Fig. 3, the GD time is proportional to capacitance and inversely proportional to the inductance.

The required variable capacitance in this work was implemented with the varactor diode SMV1233-011LF of Skyworks, by controlling the reverse bias voltage. Similarly, the required variable inductance was obtained with the high impedance transmission line terminated with the varactor diode [8].

Figure 4 shows the measurement results of varactor diode and variable inductor at a frequency of 2.14 GHz. In this work, a 90-Ω high-impedance transmission line with electrical length of 23.88° is used to obtain the required variable inductance.

III. Simulation and Experimental Results

To show the validity of the proposed GDTC circuit, the simulation and experiment were performed for the wideband code division multiple access (WCDMA) downlink band operating at 2.11 GHz to 2.17 GHz.

The simulation was done using ADS 2006A. In the simulation, the equivalent circuit of the varactor diode provided by the manufacturer was used. Figures 5(a), 5(b), and 5(c) show the simulated and measured GD time variation, the insertion loss characteristics, and return loss characteristics, respectively. The simulated GD time and the insertion loss variations are 3±0.16 ns and 5.9 dB within the excellent insertion loss flatness of 0.5 dB, respectively. The maximum return loss is –23.86 dB in the passband for the overall GD

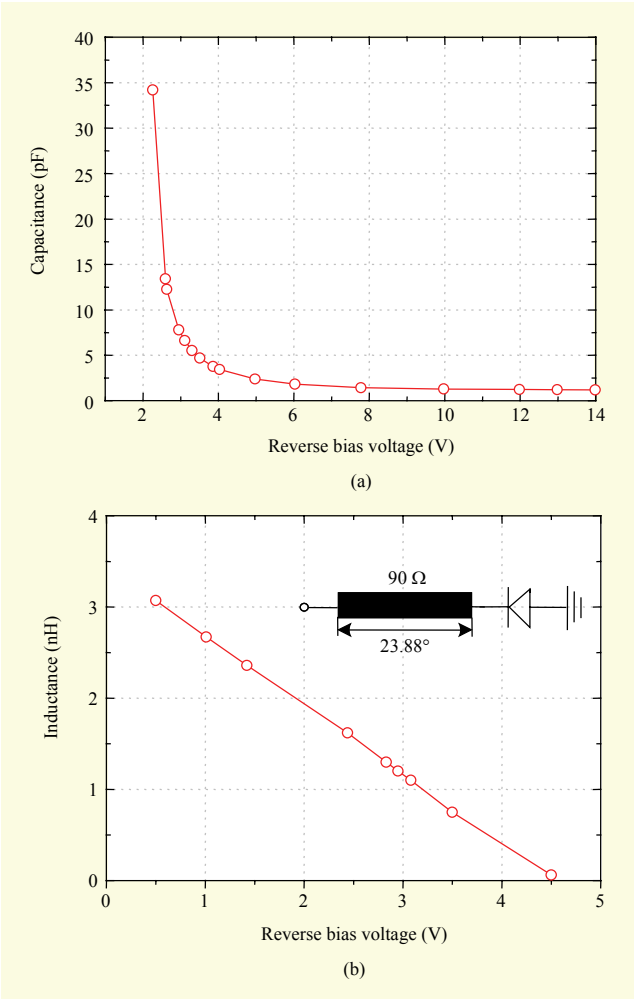

Fig. 4. Measurement results at 2.14 GHz of (a) varactor diode and (b) variable inductor.

time variation range.

From the experiment, the GD variation of 3±0.17 ns over a 60-MHz bandwidth with the excellent insertion loss flatness is obtained. The insertion loss variation is 6 dB, which is due to the variation of the junction resistance in the varactor diode according to the control bias voltage variation. The insertion loss variation can be easily compensated with an automatic gain control amplifier in the linear PA system.

The insertion loss flatness is less than 0.57 dB at fixed GD and the maximum return loss is –22.18 dB in the passband for the overall GD variation range. The reverse bias voltage variations of the varactor diodes for inductance and capacitance are 0.01 V to 3.53 V and 3.69 V to 13.18 V, respectively.

If the insertion loss flatness higher than 0.57 dB can be accepted, larger GD time variation can be obtained. So, a trade-off among the GD variations, insertion loss, and GD flatness should be considered. A slight of difference in simulation and measurement results of return loss

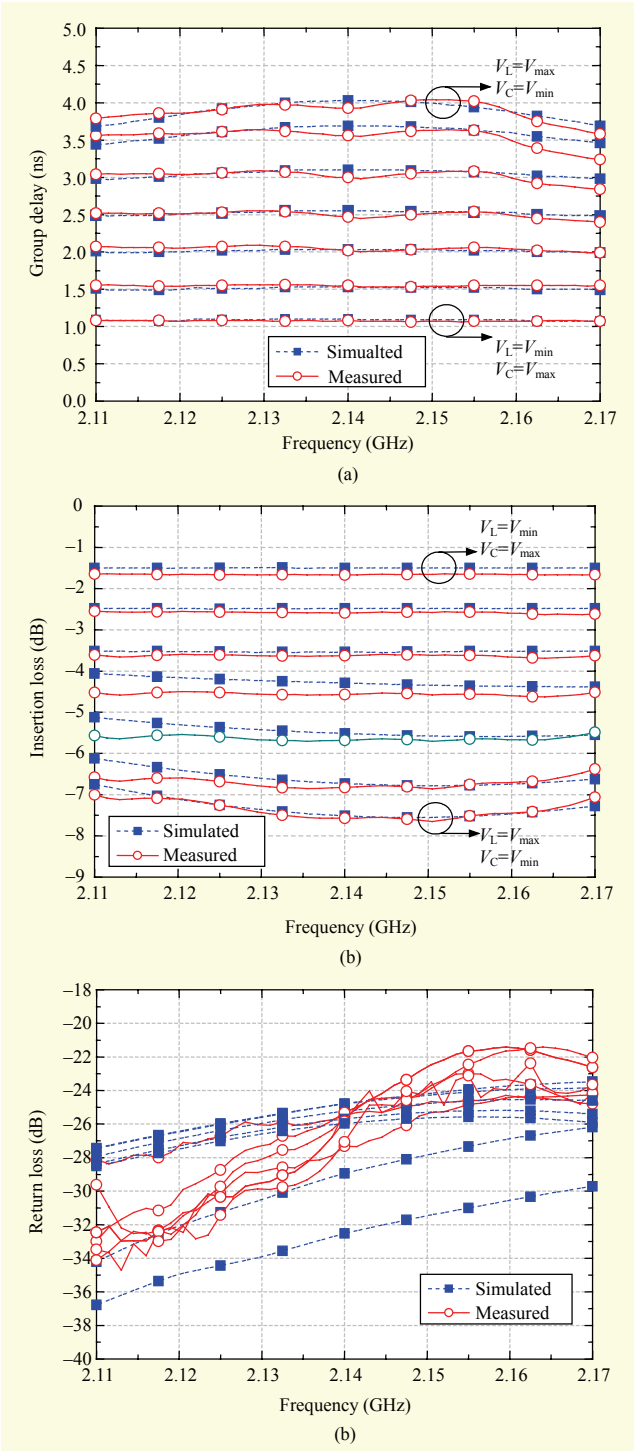

Fig. 5. Simulated and measured results: (a) GD time variation, (b) insertion loss characteristics, and (c) return loss characteristics (bias voltage variation: V_L: 0.01 V to 3.53 V and V_C: 3.69 V to 13.18 V).

characteristics is due to connecting elements at varactor diodes.

Table 1 shows the performance comparison among the previously presented GDTCs and the proposed GDTC circuit.

Table 1. Performance comparison of proposed GDTC circuit.

	Frequency	GD variation	BW	Proces
[7]	869 MHz to 894 MHz	1.0 ns	25 MHz	PCB
[8], [9]	908.5 MHz to 914 MHz	3.0 ns	5.5 MHz	PCB
[11]	N/A	1.0 ns	N/A	PCB
[12]	18 GHz to 24 GHz	0.02 ns	6 GHz	CMOS 0.18 μm
[13]	23 GHz to 25 GHz	0.087 ns	2 GHz	CMOS 0.13 μm
This work	2.11 GHz to 2.17 GHz	3.0 ns	60 MHz	PCB

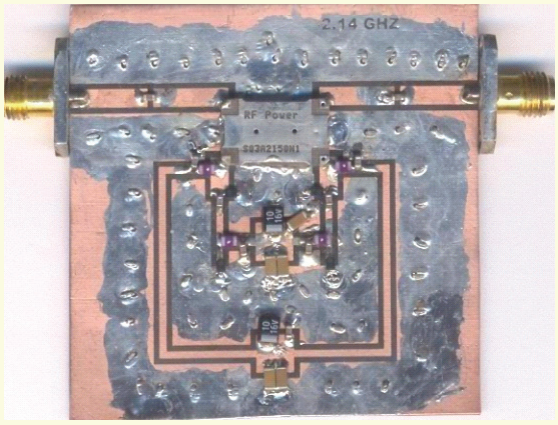

Fig. 6. Photograph of fabricated GDTC circuit.

The bandwidth of the proposed GDTC is much broader than those of the previous GDTCs within the microstrip technology. Figure 6 shows a photograph of fabricated GDTC circuit.

IV. Conclusion

In this paper, a design of a reflective-type GDTC consisting of a 3-dB 90° hybrid coupler and reflective parallel resonators has been investigated. The general design equations of the proposed circuit are derived and validated through experimentation. The simulation and experiment were performed for the WCDMA downlink frequency operating at 2.11 GHz to 2.17 GHz. The GD time and insertion loss flatness are excellent within the operating band having 3±0.17 ns of GD time variation.

The proposed GDTC circuit achieved the broadest bandwidth among the previously reported GD time circuits with an additional advantage of circuit size reduction. The proposed GDTC circuit is expected to play an important role in

broadband communication systems for which critical GD time matching is required.

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