3. NUMERICAL AND EXPERIMENTAL VALIDATION

In this section, the L-band antenna prototype is synthesized and experimentally assessed. The requirements are the following: working bands from $f_{\min} = 1.176$ Mhz up to $f_{\max} = 1.575$ Mhz, and the target value $VSWR^{\text{target}}(f)$ is imposed equal to 1.7 in the whole considered frequency range. Further requirements are the target values for the dimensions of the antenna monopole (L_X^{target} and L_Y^{target}) that are imposed equal to $\lambda'_{L5}/4 = \lambda'_{L5}/(\sqrt{\varepsilon_r}4)$, namely 35 mm. The HGA adopted in this work considers a population of $P = 10$ trial solutions, a threshold $\varepsilon = 10^{-2}$, and a maximum number of iterations $T_{\max} = 100$. The remaining parameters of the HGA have been set according the guidelines indicated in Ref. 12. A ceramic substrate, whose thickness is $h = 0.8$ mm, relative permittivity $\varepsilon_r = 3.38$, and tan $\delta = 0.002$ at $f = 10$ Ghz, is used both for numerical and experimental validation. From datasheet, we can assume the dieletric permeability of the substrate constant with a reasonable approximation in the whole operative frequency range.

First of all, the microstrip width w_{feed} has been calculated according to Eq. (1), and the result is $w_{\text{feed}} = 1.85$ mm. Successively, the numerical procedure, led by HGA, aimed to synthesize the monopolar prefractal antenna geometry has been executed. After the numerical study, an experimental validation has been carried out. The antenna prototype has been built using computer numerical control machine tools on substrate whose dimensions were 4.7×4.3 mm^2 and it has been equipped with SMA connectors at input port (Fig. 2). The prefractal monopole has dimensions equal to $L_{\text{X-a}} = 38$ mm and $L_{\text{Y-x}} = 33$ mm. The VSWR values have been measured with scalar network analyzer by placing the antenna inside an anechoic chamber. Numerical and measured VSWR data values have been compared in Figure 3. Both the dimensions of the Julia-Set monopole and the VSWR values are considered satisfactory according to the project specifications.

To evaluate the radiation properties of the prototype and to give further assessment of the antenna performance, Figure 4 shows the simulated and measured gain patterns of the considered prefractal monopole. The agreement between measured and simulated data is quite satisfactory.

4. CONCLUSION

In this Letter, the design of a prefractal Julia-set monopole antenna operating in *L*1–*L*5 bands and feed by a microstrip line is reported. The shape of the monopole is based on Julia-set to comply with geometrical and electrical constraints. The antenna has been synthesized through a HGA to optimize dimensions and prefractal geometry. An antenna prototype has been built and experimentally assessed. The comparison between measured and numerical VSWR values gives satisfactory results which confirm the reliability of the design methodology.

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DESIGN OF HIGH EFFICIENCY RF-DC CONVERSION CIRCUIT USING NOVEL TERMINATION NETWORKS FOR RF ENERGY HARVESTING SYSTEM

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ABSTRACT: *In this letter, a high efficiency RF-DC conversion circuit for RF energy harvesting system (EHS) is proposed. The proposed circuit consists of Villard voltage doubler, the input and output termination networks which can suppress the unwanted RF signals produced by Schottky diodes. The fabricated circuit operating at 2.45 GHz has a maximum RF-DC conversion efficiency of 83.37% and output voltage of 11.30 V at an input RF power of 140 mW. The proposed circuit has an advantage of simple design which helps to reduce the design cost of EHSs.* © 2012 Wiley Periodicals, Inc. Microwave Opt Technol Lett 54:2330–2335, 2012; View this article online at wileyonlinelibrary.com. DOI 10.1002/mop.27087

Key words: *RF-DC conversion; RF energy harvesting system; termination networks*

1. INTRODUCTION

As the idea of wireless power transmission (WPT) system was first suggested by Tesla [1], various studies have been performed

to design RF energy harvesting system (EHS). A rectenna which is most important component in EHS, consist of a receiving antenna and rectifier which converts the received RF signal into DC voltage. To use all received RF signal in EHS, the rectenna with a high efficient RF-DC conversion circuit is required. Various antenna structures such as dual-circularly polarized patch antenna, antenna arrays, circularly polarized antenna [2–6], and so forth, have been developed to achieve high conversion efficiency. In Ref. 7, the resistor emulation approach and various design strategies to optimize the RF-DC conversion efficiency at the output stage of rectifier were discussed for a low-power RF EHS. Similarly, the lumped-element finite difference time domain method was used to design RF-DC conversion circuit in Ref. 8. However, these methods require much time to design the optimum RF-DC conversion circuit. In Ref. 9, an antiparallel dual-diode microwave rectifying circuit was used to obtain high voltage at output stage. However, it increases the cost of rectenna system due to use of two rectifier circuits.

From the previous studies of RF-DC conversion circuits, it was found that the RF-DC conversion efficiency was increased by suppressing the harmonic frequency components. For this purpose, harmonic blocking filters were used at input and output stage of rectifier circuit [4, 5]. However, the use of filter has some disadvantages, such as complexity in designing harmonic blocking filter circuit due to the arbitrary terminated impedances. Also, an extra matching network must be designed at the fundamental frequency, which increases the size and cost of overall circuit.

This letter presents a topology of highly efficient RF-DC conversion circuit based on the concept of the harmonic termination load networks in high efficiency power amplifier such as class-E or class-F power amplifier. The proposed termination networks are used at input and output stage of the rectifier circuit to suppress the nonlinear components generated by the diodes. The major benefits of proposed circuit are that an impedance matching at the fundamental and suppression of harmonics can be performed simultaneously with same termination networks. This proposed technique can give high RF-DC conversion efficiency and helps to reduce the overall circuit size of circuit.

2. PROPOSED STRUCTURE OF TERMINATION NETWORKS

The Schottky diode having a low threshold voltage and low junction capacitance is mainly used in the design of RF-DC conversion circuits. It is basically a nonlinear dynamic conductance device with a DC V-I characteristic [10] that can be expressed as.

$$I(V) = I_S(e^{\alpha V} - 1) \tag{1}$$

Where $\alpha = q/nkT$ and q, k, T, n, and I_S are the charge of an electron, Boltzmann's constant, the absolute temperature, ideality factor, and saturation current (10^{-6}–10^{-15} Å), respectively. If the diode voltage consists of a DC bias voltage and a small-signal RF voltage as below,

$$V = V_0 + v_0 \cos \omega_0 t \tag{2}$$

the diode current can be obtained by expanding Eq. (1) in a Taylor series about V_0.

$$I(V) = I_0 + \frac{v_0^2}{4} G_d' + \left(v_0 G_d + \frac{v_0^3}{8} G_d'' \right) \cos \omega_0 t + \frac{v_0^2}{4} G_d' \cos 2\omega_0 t + \frac{v_0^3}{24} G_d'' \cos 3\omega_0 t + \cdots \tag{3}$$

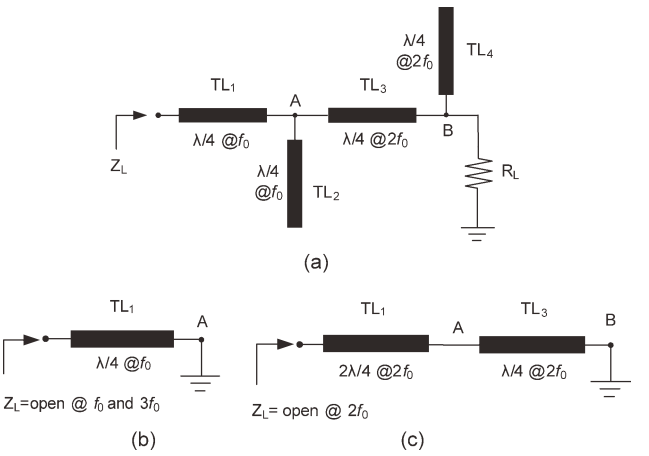

Figure 1 Proposed structure of output termination network and its equivalent circuit: (a) output load network topology, (b) equivalent circuit at f_0 and $3f_0$, and (c) equivalent circuit at $2f_0$

where G_d, G_d', and G_d'' are the first, second, and third derivatives, respectively. From Eq. (3), the output of diode includes the rectified DC component as well as the fundamental and the harmonic components. Except DC component, these harmonic components cause DC power dispersion and efficiency degradation, so that these should be suppressed to get high RF-DC conversion efficiency.

2.1. Output Termination Network for RF-DC Conversion Circuit

Figure 1(a) shows the structure of proposed output termination network in the RF-DC conversion circuit. The load impedances of proposed network are open at the fundamental (f_0), second ($2f_0$), and third harmonic ($3f_0$) frequencies, which imply the reflection of all RF components generated by the nonlinear diode and only transmission of DC power to the load. For the sake of circuit simplicity, only three RF frequencies terms are considered.

The operation of the proposed output termination network can be explained briefly as follows. The electrical lengths of transmission line TL_1 and TL_2 are quarter wavelengths ($\lambda/4$) at f_0. It provides a short circuit at the connection point (node A) at f_0 and $3f_0$ as shown in Figure 1(b). Therefore, the right side circuits of this connection, transmission lines TL_3 and TL_4, are ineffective at these frequencies. The short condition at node A will be transformed to open at the output port of the diode. This condition can provide the suppression of the f_0 and $3f_0$ components. Similarly, the line TL_2 will be open at node A for $2f_0$. If the length of transmission line TL_4 is $\lambda/4$ at $2f_0$, it provides the short condition at node B. If the length of TL_3 is also $\lambda/4$ at $2f_0$, the total length of TL_1 and TL_3 is $3\lambda/4$ at $2f_0$, as shown in Figure 1(c), which helps to transform the short impedance at node B to open at the diode output. As a result, the $2f_0$ component is also suppressed with the output termination network.

2.2. Input Termination Network for RF-DC Conversion Circuit

Figure 2(a) shows the proposed structure of the input termination network for the RF-DC conversion circuit. This network can provide the matching condition at f_0 and blocks the $2f_0$ and $3f_0$ components traveling toward the antenna. As the length of transmission line TL_6 is $\lambda/4$ at f_0, the $2f_0$ short condition can be obtained at node C as shown in Figure 2(b). Therefore, the left side circuit of this connection is ineffective at $2f_0$. By making TL_5 $\lambda/8$ long at f_0 (or $\lambda/4$ at $2f_0$), the short condition at node C is transformed to open at the input port of the diode.

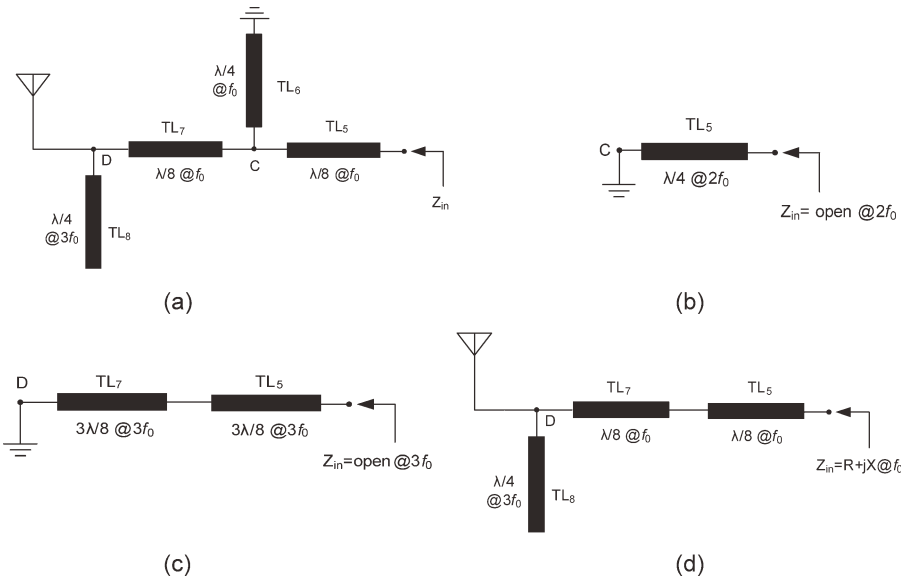

Figure 2 Proposed structure of input termination network and its equivalent circuit: (a) input termination network, (b) equivalent circuit at $2f_0$, (c) equivalent circuit at $3f_0$, and (d) equivalent circuit at f_0

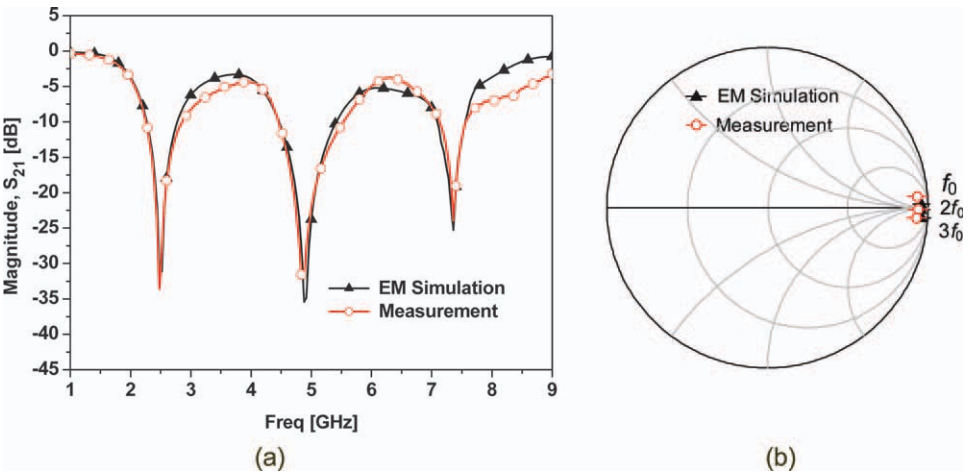

Figure 3 Simulation and measurement results of output harmonic termination load network: (a) attenuation characteristics and (b) input impedances. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

Similarly, if the length of transmission line TL_8 is $\lambda/4$ at $3f_0$, it provides a short condition at node D, as shown in Figure 2(c), and line TL_6 is ineffective at $3f_0$. This short condition at node D is transformed to open at the input of the diode by making the total length of TL_7 and TL_5, $3\lambda/4$ at $3f_0$ (or $\lambda/4$ at f_0).

Finally, the remained fundamental impedance matching can be obtained by setting the characteristic impedances of lines TL_5 and TL_7, as shown in Figure 2(d). Because the overall electrical length of transmission lines TL_5 and TL_7 is $\lambda/4$ at f_0, the input resistance of the diode can be changed to 50 Ω using the quarter wavelength transform characteristics, and the line TL_8 can resonate the susceptance component at node D. This proposed input termination network can provide easy impedance matching at f_0 and replace the low pass filter used in conventional RF-DC conversion circuits, which prevents the back-scattering of the harmonics generated at the diode of rectenna.

3. FABRICATION AND MEASUREMENT RESULTS

The proposed RF-DC conversion circuit was fabricated for ISM (Instrument, Scientific, and Measurement) frequency band operating at 2.45 GHz. To validate the proposed networks, simulations and experiments were performed on a substrate with a dielectric constant (ε_r) of 6.15 and thickness (h) of 1.52 mm. The simulation was done using HFSS v11 of Ansoft.

3.1. Design of Output Termination Network

Figure 3 illustrates the simulation and measurement results of the output termination network. Figure 3(a) shows the magnitude of the attenuation characteristics (S_{21}) at f_0, $2f_0$, and $3f_0$. In this figure, it is observed that the measurement results are in good agreement with the simulation results. The measured attenuation is greater than 28 dB at the RF frequencies

TABLE 1 The Input Impedance of Diode

Z_{in_diode}	58.404 − j 30.041 Ω
$Z_{in\_sim} = Z^*_{in\_diode}$	58.070 + j 29.550 Ω
$Z_{in\_meas} = Z^*_{in\_diode}$	58.766 + j 30.090 Ω

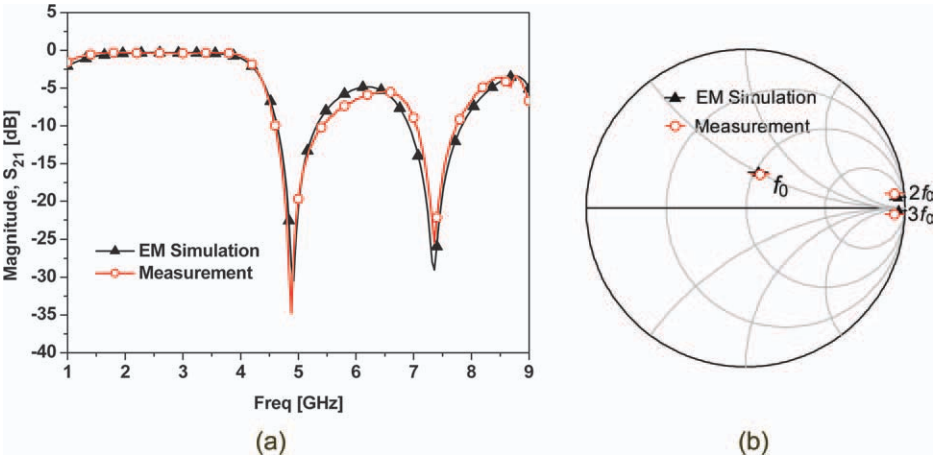

Figure 4 Simulation and measurement results of the input harmonics termination network: (a) attenuation characteristics and (b) input impedance. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

considered (f_0, $2f_0$, and $3f_0$). The load impedances at the RF frequencies are almost infinite, as shown in Figure 3(b).

3.2. Design of Input Termination Network

The extracted input impedance of the diode using the load-pull method for the optimum efficiency is shown in Table 1. The diode used in this work is HSMS-2822 of Avago. The simulation and measurement results of the input termination network are shown in Figure 4. The attenuation at $2f_0$ and $3f_0$ is greater than 28 dB, which is sufficient to suppress the back-scattering of the harmonics generated at the diode, as shown in Figure 4(a).The measured input impedances at $2f_0$ and $3f_0$ are almost infinite, as shown in Figure 4(b). The measured impedance at f_0 is almost the complex conjugate of the diode input impedances, as shown in Table 1, which confirms that the impedance matching at f_0 can be performed by just using the input termination network without any extra matching network in the RF-DC conversion circuit.

3.3. Measurement Results of Proposed RF-DC Conversion Circuit

Figure 5 shows the structure of the proposed high efficiency RF-DC conversion circuit which consists of a Villard voltage doubler and input/output termination networks. The Villard voltage doubler shown in this figure consists of two Schottky diodes, a series capacitor (C_S), load capacitor (C_L), and load resistor (R_L). A Schottky diode having a low threshold voltage and fast switching speed was chosen among the diodes as the authors' best knowledge.

The Villard voltage doubler can convert the voltage peak of the RF input signal into twice the output DC voltage, which is a suitable structure for the relatively high output voltage. The efficiency of the proposed RF-DC conversion circuit is calculated as.

$$\eta = \frac{\frac{V_{DC}^2}{R_L}}{P_{RF\_in}} \times 100\ \% \tag{4}$$

where V_{DC} is the DC output voltage at R_L. Figure 6 shows the measurement results of the RF-DC conversion efficiency and output voltage according to R_L. In this case, the input power, C_S, and C_L, are set 10 mW, 68 pF, and 50 pF, respectively. As seen from Figure 6, the efficiency is almost constant in the range of R_L over 1 and 1.55 kΩ, but decreases at R_L values above 1.6 kΩ. However, the output voltage increases with increasing load resistance. Based on these measurement results, the optimum R_L for high conversion efficiency can be chosen as 1 kΩ.

Figure 7 shows the variation of the output voltage and efficiency according to C_S to find the optimum C_S. The output voltage and efficiency are almost constant in the range of C_S over 50 pF and 80 pF. Figure 8 shows the variation of the output voltage and efficiency according to C_L. As seen from this figure, the output voltage and efficiency are almost constant for all values of C_L.

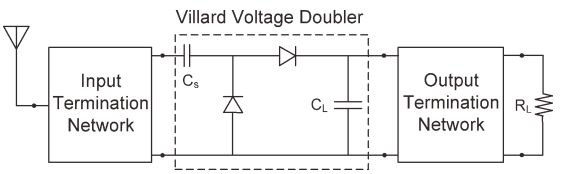

Figure 5 Structure of the proposed high efficiency RF-DC conversion circuit using input and output termination networks

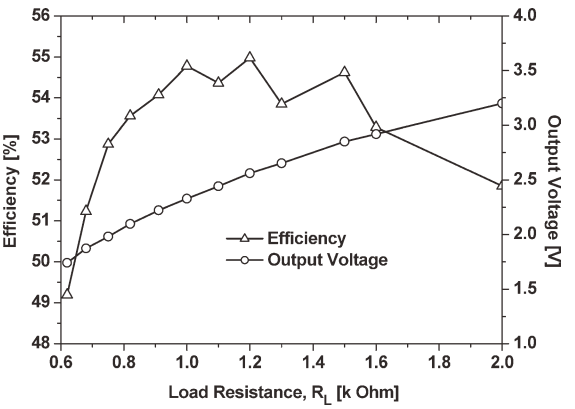

Figure 6 Variation of RF-DC conversion efficiency according to load resistance, R_L (@P_{in} = 10 dBm, C_S = 68 pF, C_L = 50 pF)

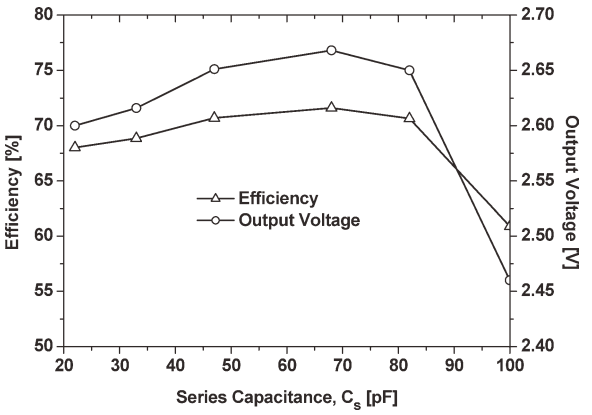

Figure 7 Variation of output voltage according to series capacitance, C_s (@R_L = 1 kΩ, P_{in} = 10 dBm)

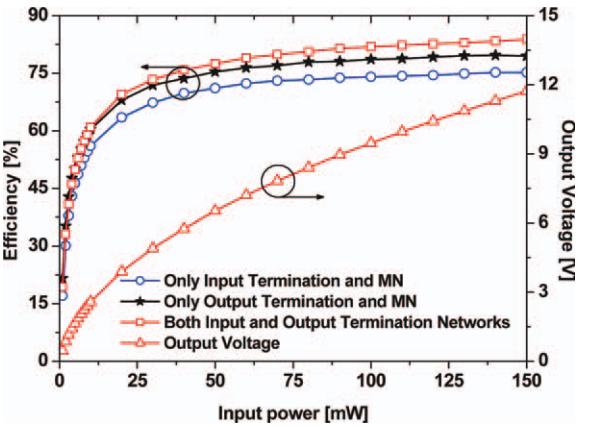

Figure 9 Measured efficiency and output voltage of the RF-DC conversion circuit. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

Figure 9 shows the measurement results of output voltage and the RF-DC conversion efficiency according to input power and input/output termination conditions. In this circuit, the values of C_S, C_L, and R_L were chosen to be 68 pF, 40 pF, and 1 kΩ, respectively. The measured conversion efficiency and output voltage increase linearly as the input power increase. The conversion efficiency became almost saturated when the input power exceed 40 mW. When the input power is 140 mW, a maximum RF-DC conversion efficiency of 83.37% and output DC voltage of 11.30 V can be obtained.

As seen from this figure, the efficiency of the circuit consisting of both the input and output termination networks is 8.5% higher than that of the circuit with only the input termination network (without the output termination network) and 3.5% higher than that of the circuit with only the output termination network (without the input termination network). From these measurement results, it can also be concluded that the output termination network is more crucial than the input termination network. However, the merits of input termination network are the impedance matching and the prevention of harmonics backscattering. Figure 10 shows a photograph of the fabricated RF-DC conversion circuit. The overall size of the proposed circuit is 55 × 35 mm^2.

A comparison of the performances of the proposed RF-DC conversion circuit with those of the previous presented circuits in the literatures is given in Table 2. From this table, it can be seen that the proposed RF-DC conversion circuit has the highest output voltage and efficiency among the previously presented circuits.

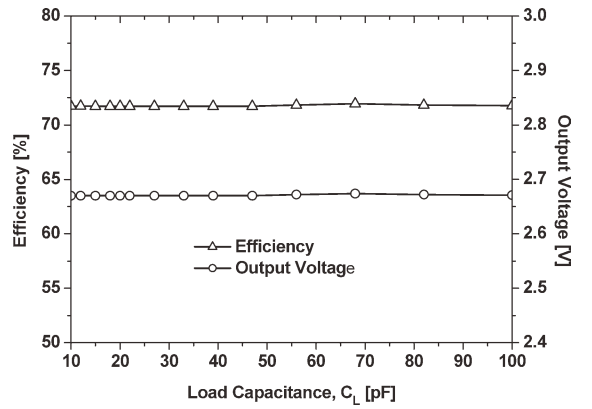

Figure 8 Variation of output voltage according to load capacitance, C_L (@C_S = 68 pF, R_L = 1 kΩ, P_{in} = 10 dBm)

4. CONCLUSIONS

In this letter, a high efficiency RF-DC conversion circuit using novel input/output termination networks is proposed. The input termination network operates as impedance matching network at the fundamental frequency as well as harmonics suppression network at the second and third harmonic components which is enough to block the second and third harmonic components. The output termination network suppresses unwanted RF signals and can transmit only the DC component to the load. The measured results of fabricated RF-DC conversion circuit show the highest output voltage and efficiency. Because of the simplicity of the proposed structure, it can be used in WPT system and various wireless communication systems required to supply the matching network at the fundamental frequency as well as to suppress the unwanted harmonics.

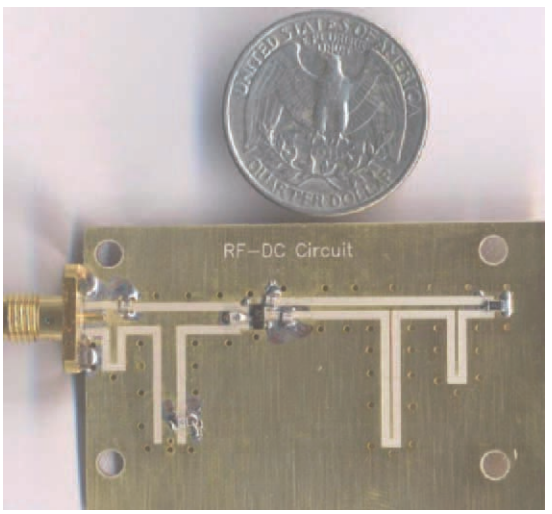

Figure 10 A photograph of the fabricated RF-DC conversion circuit. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

TABLE 2 Performance Comparison Among Previously Proposed RF-DC Circuits

	Rectifier structure	Frequency [GHz]	Output Voltage [V]	Efficiency [%]
[3]	Bride Circuit with 16 diodes	2.45	–	64
[4]	Single shunt	5.80	4.8	80
[5]	Single shunt	5.61	3.7	78
[6]	Dual series anti-parallel	5.80	6.22	76
[8]	Single series	5.80	2.8	67.5
[9]	Dual series anti-parallel	2.45	2.0	58
This work	Villard multiplier	2.45	11.30	83.37

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DRAIN-SOURCE VOLTAGE AND CURRENT WAVEFORMS MEASUREMENT METHOD USING HARMONIC ABCD MATRICES

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ABSTRACT: *In this article, a drain-source voltage and current waveforms measurement method for a fabricated power amplifier is presented. Harmonic components of the drain-source voltage and the current were obtained using measured output voltage and harmonic ABCD matrices of a load matching network. The drain-source voltage and current waveforms of a fabricated power amplifier that is operated nonlinearly were successively measured using the proposed measurement method without any influence in the power amplifier operation.* © 2012 Wiley Periodicals, Inc. Microwave Opt Technol Lett 54:2335–2337, 2012; View this article online at wileyonlinelibrary.com. DOI 10.1002/mop.27100

Key words: *waveform measurement; harmonic ABCD matrix*

1. INTRODUCTION

Voltage and current waveforms of a transistor are distorted, due to the nonlinear behavior of the transistor and the harmonic conditions of the load matching network. Therefore, it is necessary to verify drain-source voltage and current waveforms to confirm the operation mode of the power amplifier and to collect useful information about the nonlinear characteristics of the transistor.

Therefore, much research about the waveform measurement system has been reported [1–5]. However, most of the reported systems are complicated, because waveform measurement systems are integrated in load-pull systems. Inserted devices for measurement such as filters, phase shifters, and directional couplers influence the power amplifier operation as well. Unfortunately, none of the reported system to date has been compatible with the fabricated power amplifier.

In this article, a drain-source voltage and current waveforms measurement method for fabricated power amplifiers is proposed. The drain-source voltage and current waveforms are measured using harmonic ABCD matrices of a load matching network and a measured output voltage waveform in the proposed measurement method. To verify the proposed waveform measurement method, drain-source voltage and current waveform measurements were performed at 2.8 GHz using a single-ended switching-mode Class-E 10 W power amplifier with a gallium nitride high-electron mobility transistor (GaN HEMT) that was designed in [6].

2. DRAIN-SOURCE VOLTAGE AND CURRENT WAVEFORM MEASUREMENT

The proposed waveform measurement method to obtain drain-source voltage and current waveforms of a fabricated power amplifier is shown in Figure 1. The fabricated power amplifier consists of a transistor, a source matching network, and a load matching network. For the power amplifier, harmonic components are generated, due to the nonlinear behavior of the intrinsic active device. Moreover, the generated harmonic components affect the drain-source voltage $v_{DS}(t)$ and current $i_{DS}(t)$ as follows:

$$v_{DS}(t) = V_{DS,DC} + \sum_{k=1}^{N} V_{DS,k} \times cos(k\omega_0 \times t + \varphi_{DS,k}) \quad (1)$$

$$i_{DS}(t) = I_{DS,DC} + \sum_{k=1}^{N} I_{DS,k} \cdot \cos(k\omega_0 \cdot t + \theta_{DS,k}) \quad (2)$$

where $V_{DS,DC}$ and $I_{DS,DC}$ are dc components such as the drain bias voltage and current, $V_{DS,k}$ and $\varphi_{DS,k}$ are the amplitude and phase of the voltage at the k-th harmonic, $I_{DS,k}$, and $\theta_{DS,k}$ are the amplitude and phase of the current at the k-th harmonic, $k = 1,2,3\ldots$, and N is the harmonic index.

Thus, the drain-source voltage and current waveforms are obtained by combining the complex amplitude of the voltage and current at the fundamental and harmonic frequencies.