High-Efficiency CMOS Power Amplifier Using Uneven Bias for Wireless LAN Application

Namsik Ryu, Jae-Ho Jung, and Yongchae Jeong

This paper proposes a high-efficiency power amplifier (PA) with uneven bias. The proposed amplifier consists of a driver amplifier, power stages of the main amplifier with class AB bias, and an auxiliary amplifier with class C bias. Unlike other CMOS PAs, the amplifier adopts a current-mode transformer-based combiner to reduce the output stage loss and size. As a result, the amplifier can improve the efficiency and reduce the quiescent current. The fully integrated CMOS PA is implemented using the commercial Taiwan Semiconductor Manufacturing Company 0.18-μm RF-CMOS process with a supply voltage of 3.3 V. The measured gain, P_{1dB}, and efficiency at P_{1dB} are 29 dB, 28.1 dBm, and 37.9%, respectively. When the PA is tested with 54 Mbps of an 802.11g WLAN orthogonal frequency division multiplexing signal, a 25-dB error vector magnitude compliant output power of 22 dBm and a 21.5% efficiency can be obtained.

Keywords: Balun transformer, CMOS power amplifier, current-mode transformer, high efficiency, 802.11g WLAN.

I. Introduction

The demand for a higher integration of wireless transceivers in wireless communication systems has been growing rapidly to reduce the cost and size. To meet this demand, many chip set researchers have tried to enhance the transceiver integration using CMOS technology. As a result, system-on-chip (SoC) integration can be implemented in certain wireless applications, such as wireless LAN and Bluetooth. However, in the implementation of SoC integration, power amplifiers (PAs) with high performance are a major roadblock owing to the lossy substrate and low breakdown voltage characteristics of CMOS technology. In particular, the PAs of wireless LAN applications have required high efficiency and good linearity at a backed-off power level to efficiently amplify an orthogonal frequency division multiplexing (OFDM) signal with a high peak-to-average power ratio. For these reasons, many studies on a CMOS PA with high performance at a backed-off level have been actively performed [1]-[15].

The Doherty architecture PA is one of the most popular schemes for high efficiency at a backed-off power level [1]. In a conventional Doherty PA, an impedance inverter (quarter wavelength transmission line) is used to achieve an active load modulation. However, bulky transmission line transformers limit the performance of a fully integrated implementation of a CMOS Doherty PA. Previous integrated CMOS Doherty PAs have been implemented using a voltage-mode transformer based on a power combiner, which is a series combining transformers, as shown in Fig. 1 [3]-[5]. However, the series voltage combining method is very difficult to implement symmetrically and requires two or more transformers. For these reasons, the insertion loss of the voltage-mode transformer is increased and causes a degradation of the overall

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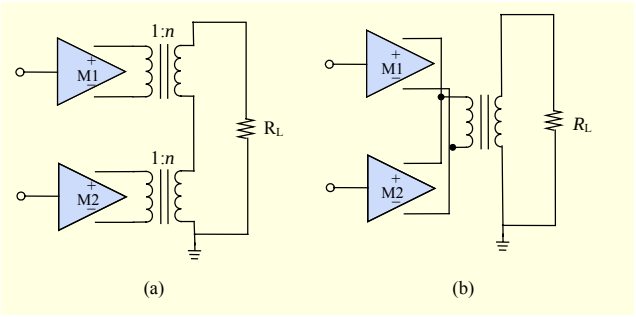

Fig. 1. Amplifier structures with (a) voltage-mode transformer-based power combiner and (b) current-mode transformer-based power combiner.

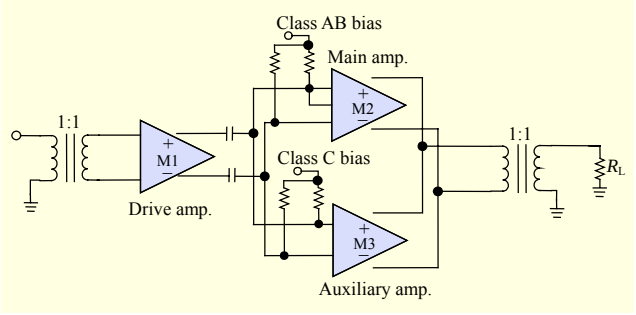

Fig. 2. Total block diagram of proposed PA.

efficiency and performance of a Doherty PA.

In this paper, a CMOS PA using a current-mode transformer-based power combiner is proposed, as shown in Fig. 1(b). The proposed structure can reduce the size and output power loss, owing to the use of only one transformer. In addition, uneven biased amplifiers such as those found in a Doherty scheme are used to enhance the efficiency at the backed-off power level and improve the nonlinear characteristics. A complete block diagram of the proposed PA is shown in Fig. 2. The PA consists of drive and power stages to obtain the high gain and high linear output power.

II. Power Combining Method of Power Amplifier

1. Impedance Transformation

Normally, the PA must have a low load impedance to increase the maximum output power at the limited voltage amplitude, as shown through (1):

$$P_{\text{out,max}} = \frac{V_{\text{max}}^2}{2R_{\text{L}}}. \quad (1)$$

Therefore, to deliver the maximum output power to the transmitting antenna, the low load impedance must be transformed into 50 Ω. In a typical GaAs heterojunction

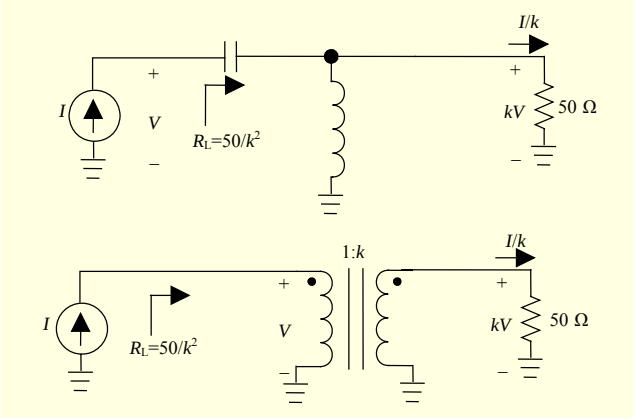

Fig. 3. (a) Impedance transformer using LC matching network and (b) magnetic coupled transformer.

bipolar transistor PA, the impedance transformation is implemented using an inductance-capacitance (LC) resonant matching network, as shown in Fig. 3(a). However, in CMOS technology, the loss of an LC resonant matching network cannot be ignored, owing to the low Q factor of the passive components and the sensitivity to the impedance error from a layout parasitic effect [10]. The magnetic coupled transformer can be used to implement the matching network as the solution of a conventional LC matching network, as shown in Fig. 3(b). The advantage of a magnetic coupled transformer is that it can be used to implement a high-efficiency matching network, regardless of the impedance transformation ratio [6]. Additionally, in the case of a CMOS PA that adopts a differential structure, the amplifier must use a balanced-to-unbalanced (balun) component to transform the differential inputs into a single output. Since a magnetic coupled transformer can perform an impedance transformation and balun operation simultaneously, it is useful for a CMOS PA design [6].

2. Power Combining Method

In a CMOS PA, a single amplifier is not sufficient to satisfy the output power requirements for certain applications, owing to a low breakdown voltage characteristic. Thus, most PAs have adopted a method for combining the output power of multiple PAs. One power combining method is the voltage-mode transformer-based power combiner. In a voltage-mode transformer-based power combiner, the secondary coils of the transformer are connected in series and their primary coils are driven by separate amplifiers, as shown in Fig. 4. The AC voltages are added to the secondary side to obtain a higher output power. The advantage of a voltage-mode transformer-based power combiner is that the impedance of each PA is upscaled n times, which relaxes the design of the PA and

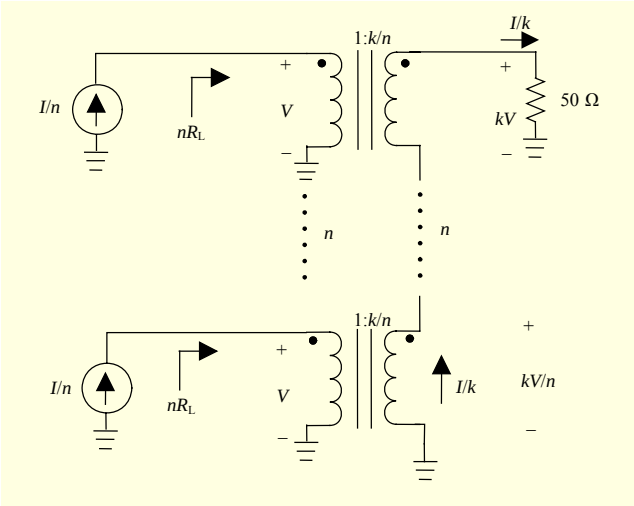

Fig. 4. Voltage-mode transformer-based power combiner.

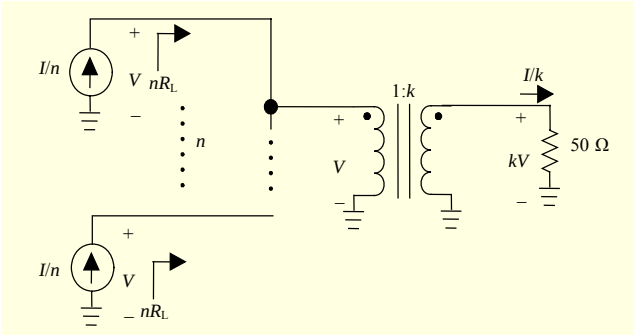

Fig. 5. Current-mode transformer-based power combiner.

reduces the sensitivity to the layout parasitic effect.

A conventional CMOS Doherty PA usually uses this voltage combining method. However, not all of the primary ports of a voltage-mode transformer may be symmetric with respect to the secondary ports, which can cause amplitude and phase mismatches. Such a mismatch can reduce the maximum output power and overall efficiency of a PA. The losses of separate transformers will also be added at the output port. Thus, the total number of transformer losses is so large that the losses cannot be ignored.

To avoid these problems, another solution for the power combining methods is the current-mode transformer-based combiner shown in Fig. 5. All the power stages can easily be made symmetric. The advantage of this topology is a smaller loss in the secondary coil. If the resistance of a secondary coil is r, the total resistive power loss is as follows:

$$P_{\text{loss},r}(\text{current\_mode}) = \frac{I^2 \cdot r}{k^2}, \quad (2)$$

where I/k is the output current. However, in the case of a voltage-mode transformer-based combiner, since the resistance

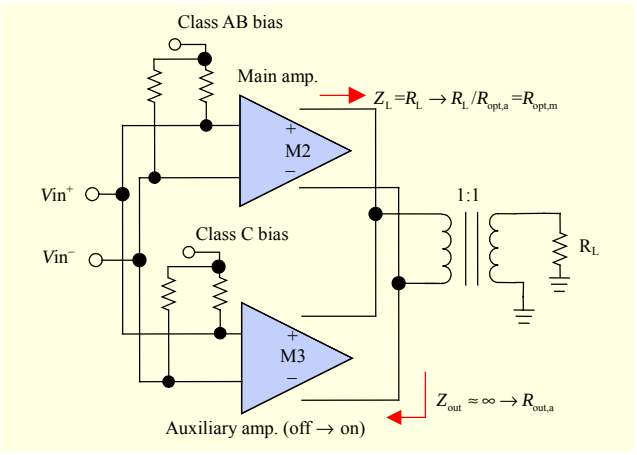

Fig. 6. Block diagram of proposed power stage.

values of secondary coils (r) are connected in series, the total resistive power loss in a secondary coil is

$$P_{\text{loss},r}(\text{voltage\_mode}) = \frac{I^2 \cdot n \cdot r}{k^2}, \quad (3)$$

where n is the number of stages. Thus, the total secondary loss of the current mode is n times smaller than that of the voltage mode. In this paper, the CMOS Doherty PA is designed using the current-mode transformer-based power combiner to reduce the transformer loss and size.

III. Operation of Proposed CMOS Power Amplifier

The proposed PA consists of the drive stage of a drive amplifier (M1) and the power stages of the class AB main amplifier (M2) and the class C auxiliary amplifier (M3), as shown Fig. 6. The class AB biased M2 provides linear amplification for all power ranges while the class C biased M3 only contributes to increasing the output linear power [5]. Therefore, the power stage amplifiers operate differently according to the input power level. At a lower power level, M3 does not operate, owing to a low bias condition ($V_{g,M3}<V_{th}$), and its consequential output impedance should be infinite to minimize the power loss. Additionally, M3 starts to operate at the power level at which M2 is saturated. In this operation, the output impedance of M3 is changed from infinite to the optimum output impedance of $R_{out,a}$, and the load impedance of M2 is decreased from R_L to $R_L/R_{out,a}(=R_{opt,m})$, which is the optimum load impedance of M2. As a result, the maximum output power of M2 is enhanced owing to a decrease of the load impedance, and the total maximum output power of the power stage is increased by combining the enhanced linear power of M2 and the output power of M3. Figure 7 shows the simulation results for the gain and output power characteristics of individual amplifiers and the combined amplifier, according

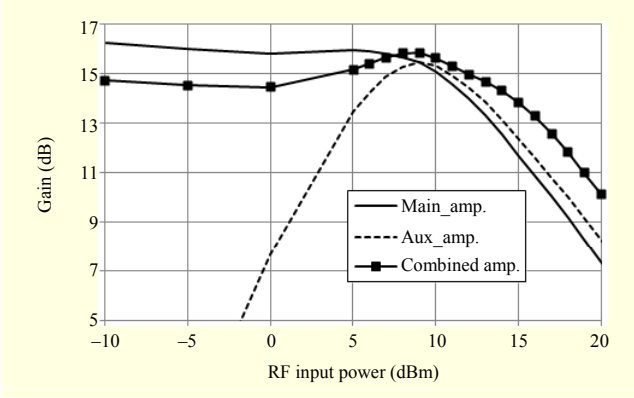

Fig. 7. Proposed power stage simulation results for RF input power vs. gain of individual amplifier and combined amplifier.

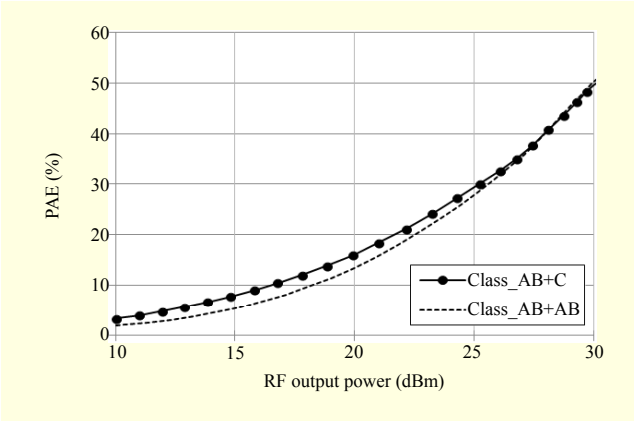

Fig. 8. PAE simulation results for even (class AB+AB) and uneven biased (class AB+C) amplifiers.

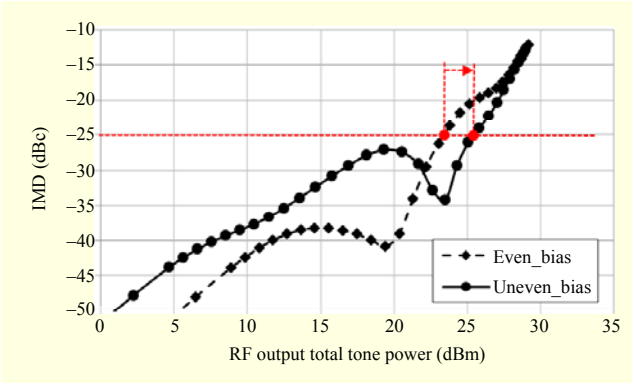

Fig. 9. IMD3 simulation results for even and uneven biased amplifiers.

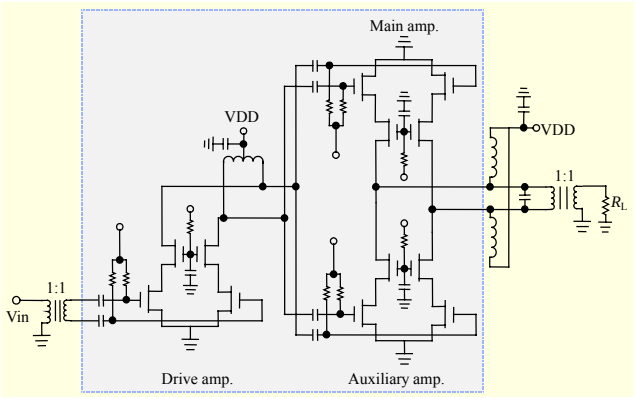

Fig. 10. Simplified schematic of designed PA.

to the RF input power. As shown in Fig. 7, the maximum output power of a combined amplifier is 4.5 dB higher than that of a class AB main amplifier alone, including a power combiner loss of 1 dB.

Although the maximum output power of the proposed amplifier has a small improvement of 1.5 dB compared to that of the even biased two-class AB amplifiers, the proposed amplifier can reduce the quiescent bias current and enhance the efficiency at a lower power level. Power added efficiency (PAE) curves for the output power of even biased (class AB) amplifiers and uneven biased (class C + class AB) amplifiers are shown in Fig. 8. Additionally, the proposed uneven biased amplifier has a good linearity performance since the higher drive power to the auxiliary amplifier causes a proper third order intermodulation distortion (IMD3) cancelation.

Figure 9 shows the simulation results of IMD3 according to the output power for even and uneven biased amplifiers. The simulation is performed using two-tone signals with 5-MHz tone spacing. As shown in Fig. 9, the proposed amplifier improves IMD3 at the higher power levels at which the auxiliary amplifier is operated. In the simulation, the two-tone total output power with IMD3 under 25 dBc is 2 dB higher than that with the even biased amplifier.

IV. Implementation of proposed CMOS PA

The design of the proposed PA is implemented using the commercial Taiwan Semiconductor Manufacturing Company 0.18-μm technology. A simplified schematic of the designed PA is shown in Fig. 10. Differential cascode structures are used as the drive and power stages to prevent gain reductions that are induced by the bonding wires. The common gate transistors of the power stage are implemented using a high breakdown voltage device (L_{min}=0.35 μm) to increase the output voltage swing. In addition, common source transistors are implemented using an RF transistor with a minimum gate length of 0.18 μm to achieve a desirable RF performance. In addition, all transistors in the drive amplifier are implemented with an RF transistor with a minimum gate length of 0.18 μm, since it can endure the output voltage swing of the drive stage.

The common source gate bias of an auxiliary amplifier for the class C operation is applied at 0.38 V, which is below the

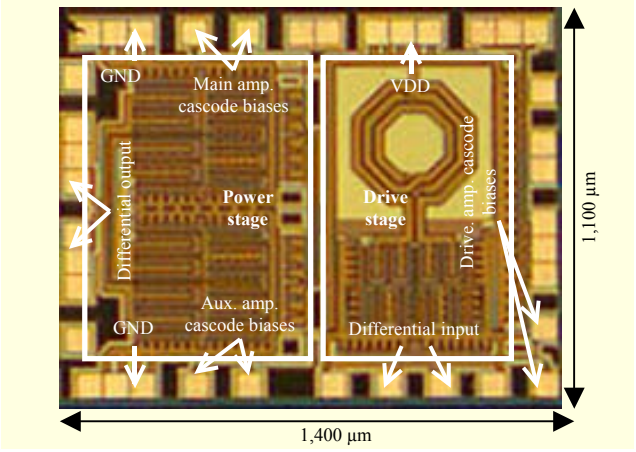

Fig. 11. Chip photograph of implemented PA.

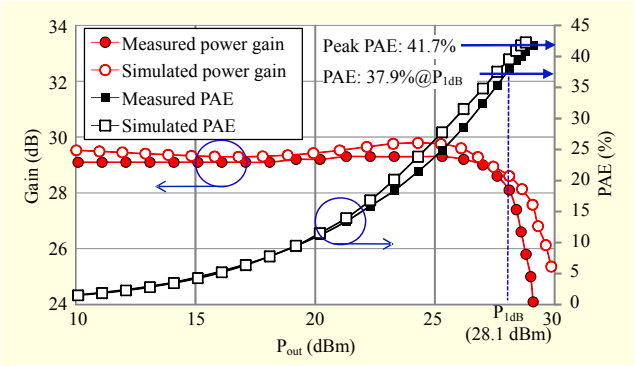

Fig. 12. Simulated and measured results for power gain and PAE according to output power level at 2.4 GHz.

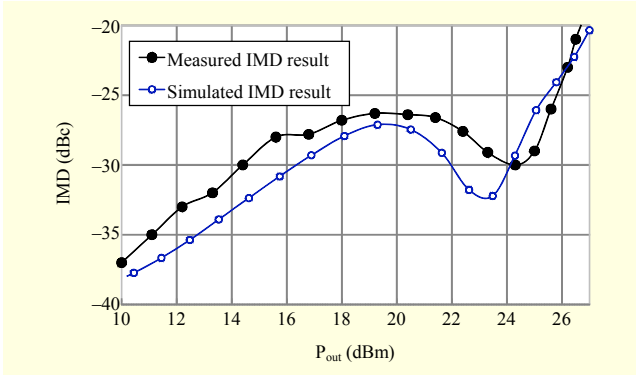

Fig. 13. Simulated and measured IMD performances for 2-tone signals with 5 MHz tone spacing at 2.4 GHz.

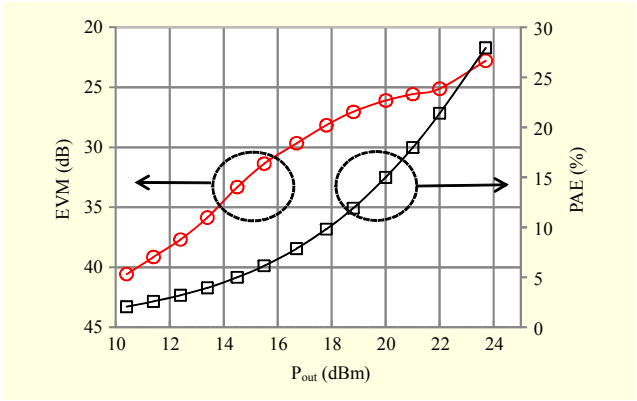

Fig. 14. Measured EVM and PAE performance of amplifier with 64-QAM OFDM at 2.4 GHz.

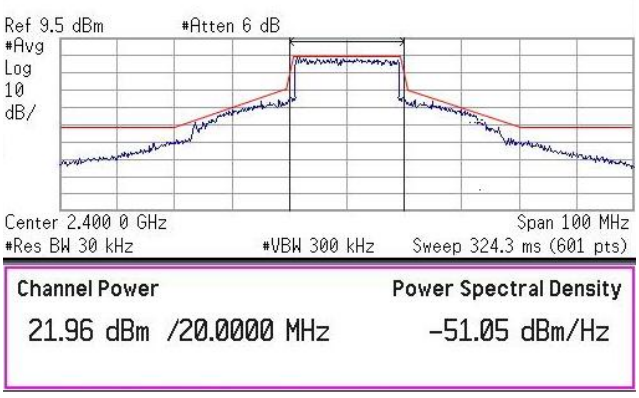

Fig. 15. Measured output spectrum mask of amplifier.

threshold voltage of 0.5 V, whereas that of the main and drive amplifiers is selected to be 0.6 V for the class AB operation and the linearity specification. Additionally, the gate bias of common gate transistors for all amplifiers is selected to be 2.2 V to reduce the voltage stress on the common source transistors, and the transistor sizes are chosen to obtain the optimum output impedance and target power.

The output signals of the main and auxiliary amplifiers are combined with a current-mode transformer. The input and output transformers are implemented with off-chip components to obtain a stable operation and reduce the chip size. A photograph of the chip layout of the proposed amplifier is shown in Fig. 11. The chip can be implemented at a compact size of 1,400 μm × 1,100 μm, including the pads.

V. Measurement Result

1. Continuous Wave (CW) Signal Measurement

Figure 12 shows the measured gain and PAE characteristics of the proposed amplifier for the CW signal at 2.4 GHz. The measured linear gain, 1 dB compression point (P_{1dB}), saturation power (P_{sat}), PAE at P_{1dB}, and peak PAE are 29 dB, 28.1 dBm, 29.5 dBm, 37.9%, and 41.7%, respectively. The amplifier has a quiescent current of 162 mA for the overall amplfier. A close agreement between the simulation and measurement results is observed.

The two-tone test is performed at 2.4 GHz with 5 MHz tone

Table 1. Comparison of CMOS PAs for WLAN application.

	Process	Supply	Frequency	P_{sat}	Peak PAE	P_{out} / PAE @ 25 dB EVM	Size
[9]	65 nm CMOS	3.3 V	2.4 GHz	31.5 dBm	25%	22.7 dBm/16%	N/A
[10]	65 nm CMOS	3.3 V	2.4 GHz	33.5 dBm	37.6%	26 dBm/20%	3 mm × 5 mm
[3]	0.25 μm CMOS	3.3 V	2.4 GHz	20.5 dBm	26.7%	13 dBm/19%	1.2 mm × 1.6 mm
[14]	90 nm CMOS	3.3 V	2.4 GHz	30 dBm	33%	22.7 dBm/124%	2 mm × 2.1 mm
This work	0.18 μm CMOS	3.3 V	2.4 GHz	29.5 dBm	41.7%	22 dBm/22%	1.4 mm × 1.1 mm
801.11g specification		Minimum EVM with 64-QAM-OFDM signal (54 Mbps): 25 dB Maximum transmitted output power: 100 mW (20 dBm)					

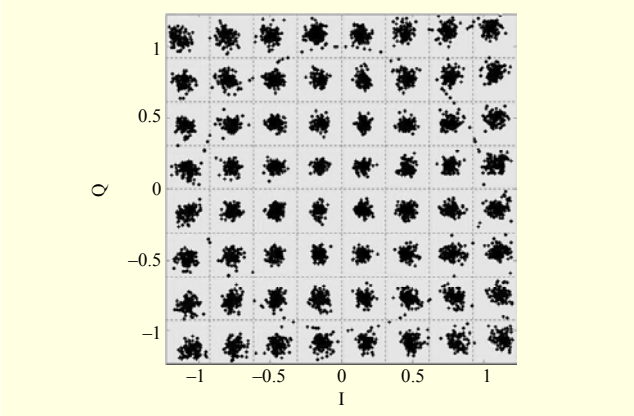

Fig. 16. Constellation error of amplifier with 64-QAM-OFDM signal.

spacing. The simulated and measured IMD3 characteristics according to the output power are shown in Fig. 13. For a linear operation of 25 dBc in the case of the two-tone signal, the PA must be operated under an output power of 25.8 dBm. Additionally, as shown in Fig. 13, the IMD3 of the fabricated amplifier is achieved under –25 dBc in all power ranges by adjusting the bias point of the main amplifier and the position of the sweet spot.

2. Modulation Signal Measurement

Finally, to verify whether the linearity of the fabricated amplifier is suitable for 802.11g WLAN system application, a high-level modulation signal is applied. The modulation signal source used is an OFDM signal with a data rate of 54 Mb/s using 64 QAM. The measured error vector magnitude (EVM) at 2.4 GHz is shown in Fig. 14. As shown in the figure, the measured average output power that satisfies the EVM requirement of 25 dB is around 22 dBm. This measured EVM compliant output power is 2 dB higher than the maximum output power requirement of 802.11g application, owing to RX/TX switching loss and line loss. Additionally, the PAE performance is 21.5% at the EVM compliant output power. Figure 15 shows the output spectrum mask of the fabricated amplifier at a channel average power of 21.9 dBm with an adjacent channel leakage ratio of 25 dBc. As shown in Fig. 15, a spectrum mask requirement can be satisfied at an average output power of 21.9 dBm. In addition, the constellation error of the amplifier at an average output power of 21.9 dBm is shown in Fig. 16.

VI. Conclusion

In this paper, a current-mode combined transformer-based uneven biased PA was demonstrated. The performances of the PA are summarized in Table 1, together with other state-of-the-art WLAN PAs. The proposed PA proved to be superior in terms of the peak PAE. Additionally, its efficiency with a 54-Mbps WLAN signal achieved 22% at the maximum linear output power, which satisfies the WLAN (802.11g) requirements. Its high efficiency results from the uneven bias and high linear characteristics of the proposed amplifier architecture. The PA showed a desirable PAE at a 25-dB EVM and spectral mask characteristics at the maximum average output power of 22 dBm. In addition, the amplifier was implemented at the small size of 1.4 mm × 1.1 mm, using the current-mode power combining method.

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