CMOS Doherty Amplifier With Variable Balun Transformer and Adaptive Bias Control for Wireless LAN Application

Namsik Ryu, Seunghyun Jang, Kwang Chun Lee, and Yongchae Jeong, *Senior Member, IEEE*

***Abstract*—This paper presents a novel CMOS Doherty power amplifier (PA) with an impedance inverter using a variable balun transformer (VBT) and adaptive bias control of an auxiliary amplifier. Unlike a conventional quarter-wavelength ($\lambda/4$) transmission line impedance inverter of a Doherty PA, the proposed VBT impedance inverter can achieve load modulation without any phase delay circuit. As a result, a $\lambda/4$ phase compensation circuit at the input path of the auxiliary amplifier can be removed, and the total size of the Doherty PA can be reduced. Additionally, an enhancement of the power efficiency at backed-off power levels can successfully be achieved with an adaptive gate bias in a common gate stage of the auxiliary amplifier. The PA, fabricated with 0.13-μm CMOS technology, achieved a 1-dB compression point (P1 dB) of 31.9 dBm and a power-added efficiency (PAE) at P1 dB of 51%. When the PA is tested with 802.11g WLAN orthogonal frequency division multiplexing (OFDM) signal of 54 Mb/s, a 25-dB error vector magnitude (EVM) compliant output power of 22.8 dBm and a PAE of 30.1% are obtained, respectively.**

***Index Terms*—Adaptive bias amplifier, CMOS power amplifier, Doherty power amplifier, variable balun transformer, 802.11g WLAN.**

I. Introduction

THE demand for higher integration of wireless transceivers has been growing rapidly to reduce the cost and size, in a recent wireless communication system. To meet these demands, many researchers who study chip sets have tried to enhance the degree of transceiver integration with low-cost CMOS technology [1]–[3]. As a result, system-on-chip (SoC) integration has been widely implemented in wireless applications such as wireless LAN and Bluetooth. In addition, recent SoC designers have attempted to integrate a PA module. However, in these efforts to create a highly integrated SoC, PAs capable of high performance levels have become a major roadblock owing to the lossy substrate and low breakdown voltages associated with CMOS technology. In particular, the OFDM signal of the 801.11g standard has a very high peak-to-average power ratio (PAPR). For these reasons, many studies for CMOS PAs have focused on efficiency enhancements and linearity improvement at a backed-off power level relative to the peak power [1]–[25].

Linearization techniques such as supply bias modulations and out-phasing methods are proposed to enhance the efficiency at backed-off power levels. However, these techniques have significant limitations with regard to the output power dynamic range and operating bandwidth. The Doherty PA is one of the most popular schemes with which to obtain high efficiency at backed-off power levels [1]. In the conventional Doherty PA, an impedance inverter such as a $\lambda/4$ transmission line is used to realize active load modulation. However, the large circuit size of the transmission line transformers limits the fully integrated implementation of a CMOS Doherty PA [16]–[22].

In order to facilitate high integration, previous integrated CMOS Doherty PAs used a lumped element pi-network as the impedance inverter. However, because CMOS differential PAs require two impedance inverters on each differential path, the size of the impedance inverters cannot be neglected. In addition, due to the low thresh-hold voltage of CMOS process, an auxiliary amplifier biased for class C operation is activated at a power level lower than its designed power level. As a result, the efficiency of a Doherty PA degrades in the backed-off power region [3]–[8]. To overcome these problems, a CMOS Doherty amplifier with a VBT impedance inverter and an adaptive bias control scheme is proposed.

In Section II, the conventional Doherty PA architecture and its operation are described. Section III explains the proposed VBT impedance inverter and the auxiliary cascode amplifier, which uses an adaptive bias control scheme. In Section IV, the implementation and measured results of the fabricated CMOS Doherty PA are described, followed by a brief conclusion in Section V.

II. Doherty Amplifier Operation

A. Load Modulation

The Doherty amplifier was first proposed in 1936 [1] and focused on efficiency enhancements or power conservation primarily. The original Doherty amplifier consisted of two tube amplifiers and an impedance inverter, as shown in Fig. 1(a). This impedance (Z)-inverter is configured using a $\lambda/4$ transmission line, and it modulates the load impedance (Z_m) of the main amplifier according to the operation of the auxiliary amplifier. This

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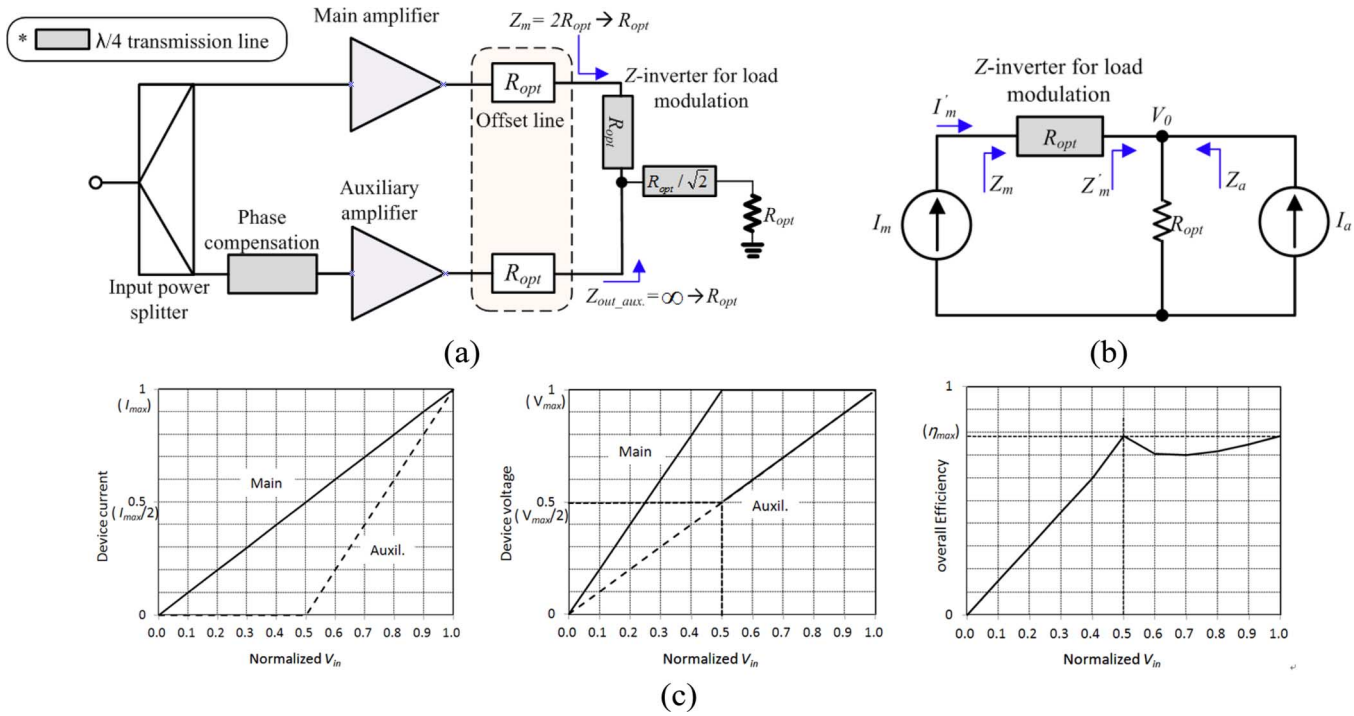


Fig. 1. (a) Conventional Doherty amplifier structure, (b) simplified schematic diagram for load modulation, and (c) ideal output current/voltage/efficiency of the main and auxiliary amplifier.

modulation ensures superior efficiency performance of the Doherty amplifier in the low-power region [5]–[7].

Fig. 1(b) shows a simplified schematic diagram which explains the load modulation process. It is assumed that both amplifiers have high output impedance and that both can be replaced with current sources. Load modulation is conducted according to the fundamental current ratios of both amplifiers. In the Doherty PA, the main amplifier is normally biased with the class AB or B mode, while the auxiliary amplifier is biased with the class C mode. Therefore, only the main amplifier is operated until its maximum output voltage is reached. Thus, the first efficiency peak is achieved. When the input voltage is increased further, the auxiliary amplifier is turned on, while the load impedance of the main amplifier is decreased. Although the output voltage of the main amplifier remains constant, the total output voltage of the Doherty PA is increased by the operation of the auxiliary amplifier. As a result, a second efficiency peak can be achieved at the maximum voltage of the auxiliary amplifier, as shown Fig. 1(c). These two peak efficiency points help to enhance the efficiency at backed-off output power levels. The key factor to this operation is the load modulation of the amplifiers by the impedance inverter. The load impedance of each amplifier can be derived by the active load-pull principle [16]–[25]. This is expressed in (1a) and (1b):

$$Z_m = 2 \cdot R_{\text{opt}}, Z_a = \infty, \ @\ 0 < \frac{V_{\text{in}}}{V_{in,\max}} \leq \frac{1}{2} \quad \text{(1a)}$$

$$Z_m = \frac{2 \cdot R_{\text{opt}}}{1 + \dfrac{I_a}{I_m}}, \ Z_a = \left(1 + \frac{I_m}{I_a}\right) \cdot \frac{R_{\text{opt}}}{2}, \quad @\ \frac{1}{2} < \frac{V_{\text{in}}}{V_{in,\max}} \leq 1 \quad \text{(1b)}$$

where $V_{\text{in}}, V_{\text{in,max}}, Z_m$, and Z_a are the input voltage, the maximum input voltage, and the load impedances of the main and auxiliary amplifiers, respectively. I_m and I_a correspondingly represent the total drain current of the main and auxiliary amplifiers, and R_{opt} is the optimum load impedance required to obtain the maximum output power [3].

As shown in (1a) and (1b), the main PA maintains a load impedance of $2 \cdot R_{\text{opt}}$ while the auxiliary PA is turned off. Thus, the first maximum efficiency of the Doherty PA is generated by operation of the main PA at half of $V_{\text{in,max}}$, as shown in Fig. 1(c). In addition, when V_{in} increases from half of $V_{\text{in,max}}$ to $V_{\text{in,max}}$, I_a and I_m are reached at the same maximum output current while Z_m is changed to R_{opt}, Z_a is also changed to R_{opt}. As a result, the Doherty PA scheme leads to an overall output power increase of 6 dB with achieving the second peak efficiency at the maximum output power of the amplifier.

Consequently, the Doherty PA has superior efficiency compared to the class B PA throughout the output power range. Accordingly, the Doherty PA is a useful PA scheme in modern wireless systems for high-PAPR applications.

B. Linearity

The Doherty PA has a linear gain for all output power ranges through load modulation. At a low power level, only the main amplifier is turned on. Therefore, the load impedance of the main amplifier is twice that at the high power level, and the gain is doubled. However, the input power of the main amplifier becomes half of the total input power due to the use of an input power splitter. When the auxiliary amplifier is turned on at high power level, the gain of the main amplifier is reduced due to the reduced load impedance, whereas the total gain is compensated by the auxiliary amplifier operation. Ultimately, the gain

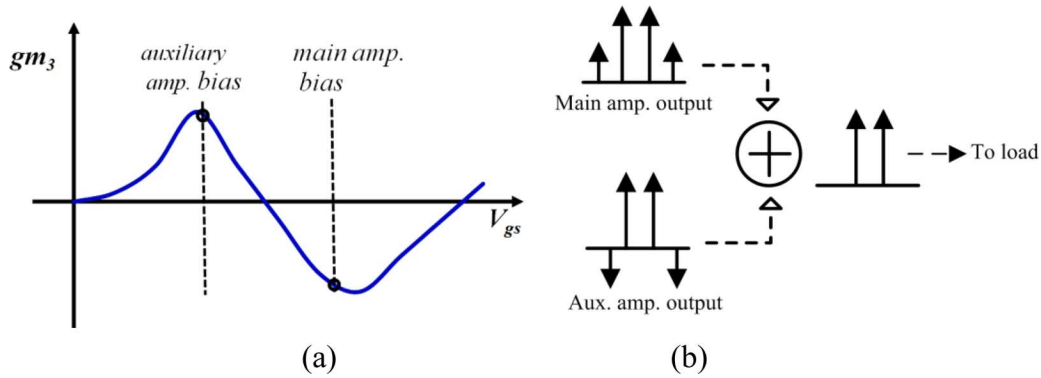


Fig. 2. (a) Third-order transconductance coefficient (g_{m3}) curve of a general MOSFET according to the bias point and (b) output fundamental and third order IM signal of each amplifier with the phase in the spectrum domain.

of the Doherty PA is constant throughout the input power range. Thus, the Doherty PA can achieve a linear AM-AM response as a function of the input power.

The main and auxiliary amplifiers have nonlinearity like other class AB, B, or C amplifiers. However, the nonlinearity of each amplifier can be cancelled out by the destructive combination of differently biased amplifiers. The transfer function of the main and auxiliary amplifiers can be modeled using a Taylor series expansion equation, as follows:

$$\begin{aligned} I_{\rm out}(v_{\rm in}(t)) &= \frac{dI_{\rm DS}}{dV_{\rm GS}} \cdot v_{\rm in}(t) + \frac{1}{2!}\frac{d^2 I_{\rm DS}}{dV_{\rm GS}^2} \cdot v_{\rm in}^2(t) \\ &\quad + \frac{1}{3!}\frac{d^3 I_{\rm DS}}{dV_{\rm GS}^3} \cdot v_{\rm in}^3(t) + \cdots \\ &= g_{m1} \cdot v_{\rm in}(t) + g_{m2} \cdot v_{\rm in}^2(t) + g_{m3} \cdot v_{\rm in}^3(t) + \cdots \end{aligned} \tag{2}$$

where $v_{\rm in}, g_{mn}$, and $I_{\rm out}$ are the input voltage, the nth order coefficients of the nonlinear transconductance, and the output current, respectively.

Fig. 2(a) shows the third-order transconductance coefficient (g_{m3}) curve of a standard MOSFET as function of the gate bias voltage. This parameter is related to the third-order harmonics and the generation of intermodulation distortion (IMD) signals. As shown in Fig. 2(a), its polarity changes according to the gate bias. With the proper combination of the main and auxiliary amplifiers, the third-order IMD signals can be cancelled, as in Fig. 2(b). To understand the cancellation operation of the third-order IMD in the spectrum domain, the input two-tone signals are expressed as

$$v_{\rm in}(t) = A\left\{\cos(\omega_1 t) + \cos(\omega_2 t)\right\}. \tag{3}$$

When two-tone signals are injected into the main and auxiliary amplifiers, the third-order IMD signals generated by the main and auxiliary amplifiers can be calculated. To clarify this, we assume that this is an ideal memoryless amplifier. In this case, the upper and lower IMD signals will be the same. Therefore the upper third-order IMD signals of the main and auxiliary amplifier at $2(\omega_2 - \omega_1)$ in terms of $I_{\rm out}(v_{\rm in})$ are given as

$$\begin{aligned} I_{\rm out\_main}(2\omega_2 - \omega_1) &= \frac{3}{4} g_{m3\_\rm main} \cdot A^3 \cdot e^{j\theta_{\rm main}} \\ I_{\rm out\_aux.}(2\omega_2 - \omega_1) &= \frac{3}{4} g_{m3\_\rm aux.} \cdot A^3 \cdot e^{j\theta_{\rm aux.}} \end{aligned} \tag{4}$$

where $\theta_{\rm main}$ and $\theta_{\rm aux.}$ are the phases of the third-order IMD signals, which depend on the $g_{m3\_\rm main}$ and $g_{m3\_\rm aux}$ values of the main and auxiliary amplifiers, respectively. As shown in Fig. 2(a), the third-order g_{m3} of a class C biased auxiliary amplifier has opposite polarity relative to that of the class AB biased main amplifier. As a result, the third-order IMD signals are cancelled out by the combination of the opposite phase signals. Fig. 2(b) shows the output fundamental signals and the third-order IMD signals at the output port of each amplifier with a phase in the spectrum domain. Although this g_{m3} cancellation scheme cannot be perfect due to memory effect and PVT variation in a real case, the linearity improvement effect was proved in many previous studies [3]–[6].

III. Design of the CMOS Doherty Amplifier

A. Load Modulation With a Variable Balun Transformer

In the CMOS amplifier design, a single amplifier is not sufficient for the high output power requirement due to its low breakdown voltage. In addition, since there is no back-via, which is used for a ground connection in the HBT and GaAs process, the gain reductions caused by the ground wire bonding degeneration effect cannot be ignored. Thus, the CMOS amplifier relies on differential or cascode structure to prevent wire bonding degeneration loss and avoid the breakdown issue. Additionally, the antenna and filter connected to the output port of the PA are usually single-ended components. As a result, a balun transformer is necessary to connect the differential amplifier to the single-ended components and to convert the optimum load impedance of the PA to 50 Ω.

Recent CMOS PAs use a coupled transformer to achieve output impedance matching instead of on-chip passive components with a low Q-factor. Fig. 3(a) shows the conventional balun transformer used for the output matching of the amplifier. In order to implement an impedance inverter for load modulation without a $\lambda/4$ transmission line, the input resistance of the transformer ($R_{\rm in}$) has to be changed from $2 \cdot R_{\rm opt}$ to $R_{\rm opt}$ while the output resistance of the transformer ($R_{\rm out}$) has to be changed from $R_{\rm out}$ to $2 \cdot R_{\rm out}$. Fig. 3(b) shows the proposed VBT for active load modulation. In the proposed VBT, downward and upward *LC* transformers have been added at the input and output ports of the conventional balun, respectively. In addition, the VBT has bigger capacitors (C_a' and C_b') compared

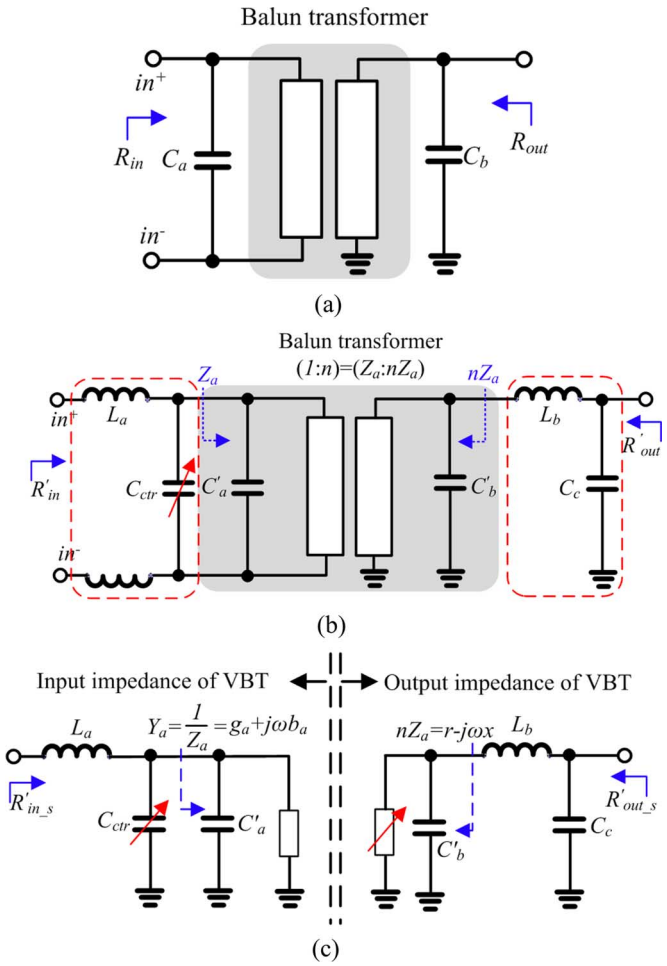


Fig. 3. (a) Conventional balun transformer for output matching, (b) architecture of the proposed VBT, and (c) simplified equivalent circuit of the VBT.

to those (C_a and C_b) of the conventional transformer to achieve matching using the additional inductor (L_a, L_b). A simplified equivalent circuit of the proposed VBT can be represented as shown in Fig. 3(c). To simplify the analysis, only single input impedance is considered in Fig. 3(c). The input impedance of VBT, $Z'_{\text{in\_s}}$, is given as follows:

$$\begin{aligned} Z'_{\text{in\_s}} &= \left(Z_a // -j\frac{1}{\omega C_{\text{ctr}}} \right) + j\omega L_a \\ &= \frac{g_a}{g_a^2 + \omega^2(b_a + C_{\text{ctr}})^2} - j\omega \\ &\quad \cdot \frac{b_a + C_{\text{ctr}}}{g_a^2 + \omega^2(b_a + C_{\text{ctr}})^2} + j\omega L_a \end{aligned} \tag{5}$$

where

$$Y_a = \frac{1}{Z_a} = g_a + j\omega b_a. \tag{6}$$

Z_a and Y_a and C_{ctr} are the input impedance and admittance of a $1{:}\,n$ coupled transformer, and variable capacitance to achieve variable impedance transformation, respectively. In addition, g_a and ωb_a are the conductance and susceptance of the Y_a, respectively. If the C_{ctr} is increased from 0 pF, an imaginary part with C_{ctr} of 0 pF should be removed by the serial inductance (L_a). As a result, the L_a can be selected as

$$L_a = \frac{b_a}{g_a^2 + \omega^2 (b_a)^2}. \tag{7}$$

Hence, the imaginary part of $Z'_{\text{in\_s}}$ is rewritten as follows:

$$-j\omega \cdot \left(\frac{b_a + C_{\text{ctr}}}{g_a^2 + \omega^2(b_a + C_{\text{ctr}})^2} - \frac{b_a}{g_a^2 + \omega^2(b_a)^2} \right). \tag{8}$$

In addition, the input resistance $(R'_{\text{in\_s}})$ is written as follows:

$$\begin{aligned} R'_{\text{in\_s}} &= \frac{g_a}{g_a^2 + \omega^2 b_a^2}, \quad @\ C_{\text{ctr}} = 0 \\ R'_{\text{in\_s}} &= \frac{g_a}{g_a^2 + \omega^2(b_a + C_{\text{ctr}})^2}, \quad @\ C_{\text{ctr}} \neq 0. \end{aligned} \tag{9}$$

From (8) and (9), we can calculate the optimum Z_a and C_{ctr} for target of impedance variation. Similarly, the output impedance of VBT $(R'_{\text{out\_s}})$ can be expressed as follows:

$$R'_{\text{out\_s}} = \frac{nZ_a}{(nZ_a \cdot \omega C_c)^2 + (\omega^2 L_b C_c - 1)^2}. \tag{10}$$

In this equation, nZ_a, L_b and C_c are the output impedance of the $1{:}\,n$ coupled transformer, and the inductance and capacitance of the upward LC transformer, respectively.

The input and output impedances of VBT can be explained qualitatively via (9) and (10). As C_{ctr} increases, the $R'_{\text{in\_s}}$ will decrease and $R'_{\text{out\_s}}$ will increase. Fig. 4(a) shows simulated input and output impedance variations according to C_{ctr} at 2.4 GHz. The variation of C_{ctr} in the VBT network mostly affects the real part of the impedance with minimal changes of the imaginary part of the impedance, as shown in Fig. 4(a). An HFSS electromagnetic (EM) simulation was conducted to design the coupled balun transformer. The designed transformer has an insertion loss of 1.5 dB at 2.4 GHz. The values used for L_a, L_b, and C_c are 0.15 nH, 1.8 nH, and 2.0 pF, respectively. As shown in Fig. 4(b), the total resistance transforming ratio of VBT is from 50:50 Ω to 22:98 Ω for a C_{ctr} variation range of 0 pF to 1.4 pF. Therefore, the resistance variation of the proposed VBT can be controlled properly for the load modulation of the Doherty PA by C_{ctr}. Additionally, Fig. 4(c) shows the phase transfer characteristic of VBT as the function of C_{ctr} in the range of 0 pF to 1.4 pF. Although the VBT has 23.1° of phase variation throughout the C_{ctr} range, the phase should be considered only within auxiliary amplifier operating range. When the auxiliary amplifier is operated at full capacity, C_{ctr} has to be 1.4 pF and the balun of the auxiliary amplifier has to be matched to obtain 180° phase transfer characteristic. Thus, the phase difference between two baluns is 5.4° when the PA is operated at maximum output power. This phase error can be compensated by tuning the matching network of an auxiliary amplifier. As a result, the proposed Doherty PA can be implemented at small size since it does not require bulky $\lambda/4$ transmission lines and additional phase compensation circuit on the RF signal path of the auxiliary amplifier.

B. Auxiliary Amplifier With Adaptive Bias

Load modulation of the Doherty PA is based on the amounts of current of the active devices with respect to the power

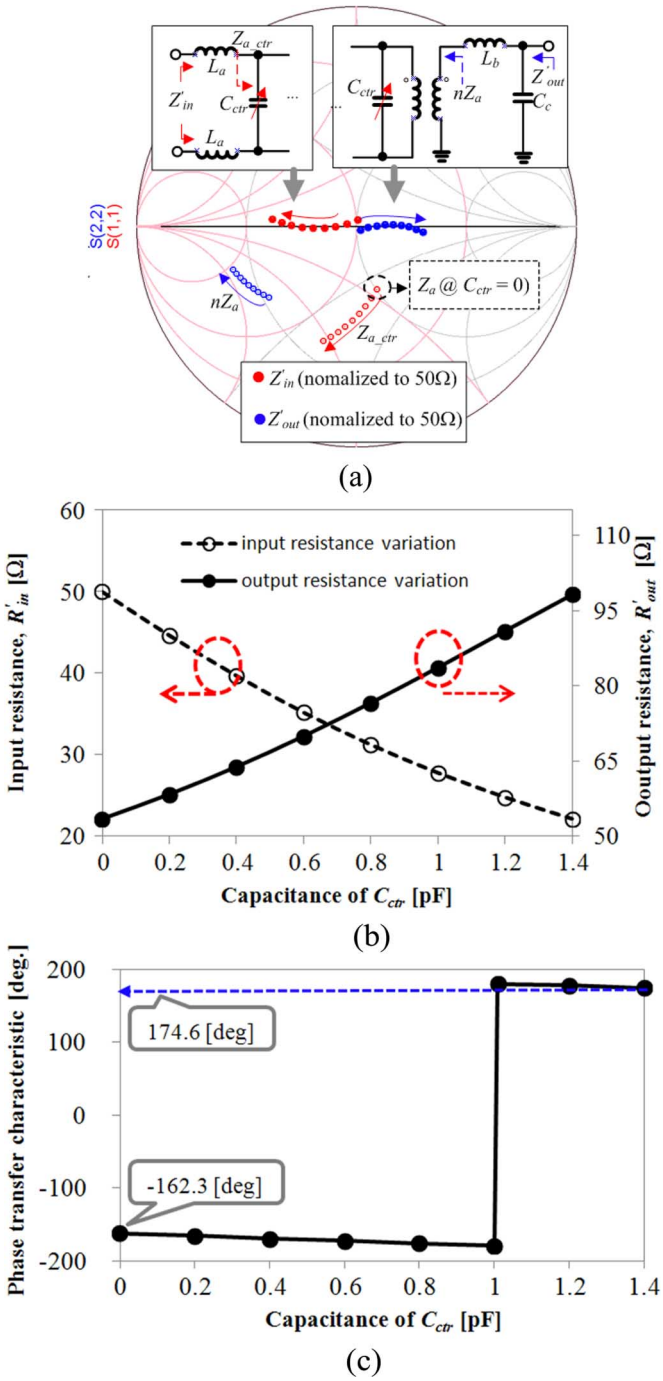


Fig. 4. (a) Simulated input and output impedance variations of VBT according to C_{ctr}, (b) input and output resistance variation curves, and (c) simulated phase-transfer characteristic of VBT as function of C_{ctr}.

level. For proper Doherty operation, the auxiliary amplifier rather than the main amplifier has important role in delivering an appropriate fundamental current [18]–[20]. As mentioned in Section II, the drain current of the auxiliary amplifier has to be zero in the low-power region and must be identical to that of the main amplifier at the maximum input power level. However, in a real situation, the drain current of the auxiliary amplifier is slightly lower than that of the main amplifier at the maximum input power level due to the lower bias of the auxiliary amplifier. In addition, a class C biased auxiliary amplifier with a cascode structure does not have a zero drain current at

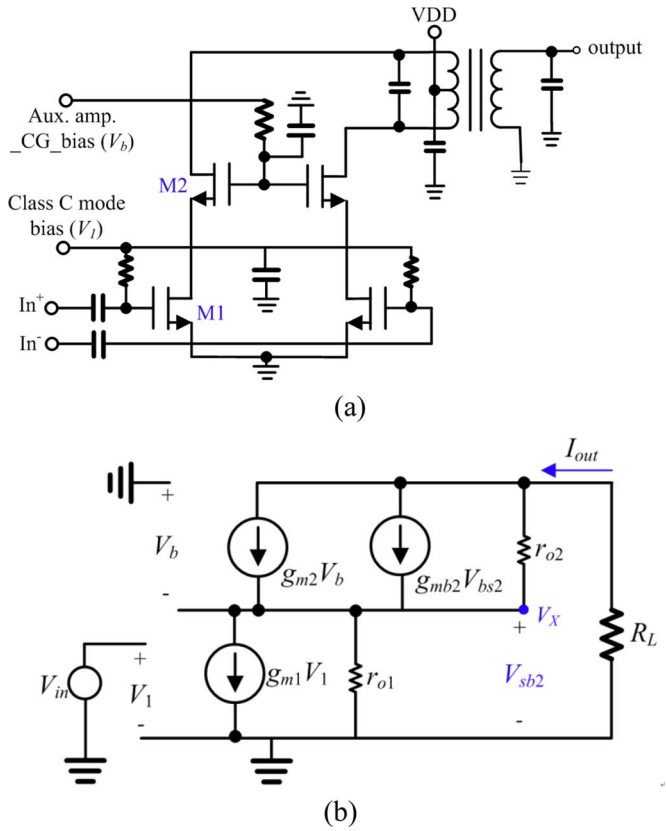


Fig. 5. (a) Simplified schematic of an auxiliary amplifier with a cascode structure and (b) simplified equivalent circuit of a single-stage cascode amplifier.

the desired backed off power level due to the low thresh-hold voltage (V_{th}) and the gain of the common gate stage. For these reasons, an adaptive biased CMOS auxiliary amplifier can improve the efficiency at a backed-off power level and can increase the gain at the maximum input power level.

As shown in Fig. 1(c), the ideal transfer characteristic of the auxiliary amplifier can be expressed simply as follows:

$$I_{\mathrm{out}}^{\mathrm{aux.}} = 2G_m \cdot (v_{\mathrm{in}} - \frac{V_{\mathrm{in,max}}}{2}), \quad @\frac{V_{\mathrm{in,max}}}{2} < v_{\mathrm{in}} < V_{\mathrm{in,max}}$$
$$I_{\mathrm{out}}^{\mathrm{aux.}} = 0, \quad @0 < v_{\mathrm{in}} < \frac{V_{\mathrm{in,max}}}{2}, \tag{11}$$

where G_m denotes the transconductance. If the characteristic of an ideal auxiliary amplifier follows that of the main amplifier, the adaptive G_m of the auxiliary amplifier has to serve the function of v_{in}.

Fig. 5 shows a simplified schematic and the equivalent circuit of the auxiliary cascode amplifier. As shown in Fig. 5(b), the output current of the cascode amplifier can be written as

$$I_{\mathrm{out}} = g_{m2}V_2 + g_{mb2}V_{bs2} = \frac{1}{2}k'_{M2}(V_b - V_x - V_{\mathrm{th}})^2 \tag{12}$$

where

$$k'_{M2} = \mu_{n,M_2} C_{ox,M_2} \frac{W_{M_2}}{L_{M_2}}$$

Given that V_x depends on the transconductance of the common source stage, (12) can be rewritten as follows:

$$I_{\mathrm{out}} = \frac{1}{2}k'_{M2}(V_b + g_{m1}V_{\mathrm{in}}r_{o1} - V_{\mathrm{th}})^2. \tag{13}$$

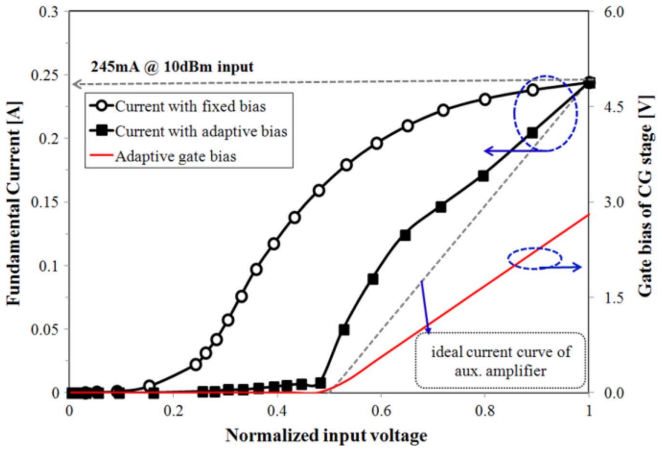


Fig. 6. Simulated fundamental currents of an auxiliary amplifier with/without the adaptive gate bias of the common gate stage.

Therefore, the total transconductance of the cascode amplifier is given as

$$G_m^{\text{cascode}} = \frac{I_{\text{out}}}{V_{\text{in}}} = \frac{1}{2}k'_{M2} \cdot V_{\text{in}} \cdot \left(\frac{V_b - V_{\text{th}}}{V_{\text{in}}} + g_{m1}r_{o1}\right)^2. \tag{14}$$

Thus, G_m of the cascode amplifier can be controlled by adjusting the gate bias of the common gate (CG) stage, which is the function of the input voltage. Fig. 6 shows the simulation results for the output current of the auxiliary amplifier with a fixed CG gate bias of 2.8 V and sweeping bias from 0 V to 2.8 V according to v_{in}. In the simulation, the gate bias of the common source stage is set to 0.18 V as class C mode bias. As shown in Fig. 6, the current consumption of the auxiliary amplifier with the adaptive bias can reduce the input voltage by half of $V_{\text{in,max}}$. As a result, the efficiency of the Doherty PA can be improved in the low-power region. In addition, the reduced gain of the auxiliary amplifier can be offset by injecting the higher gate bias of the CG. Thus, the auxiliary amplifier with the adaptive bias can control the power gain according to the input power level while maintaining the nonlinearity cancellation characteristics.

IV. Implementation and Measured Results

A. Implementation

The proposed PA is implemented using Taiwan Semiconductor Manufacturing Company (TSMC) 0.13 μm technology. The layout of the VBT network with the balun is shown in Fig. 7(a). The metal lines for the balun are ultra-thick metal with a high Q factor and high current capability. In addition, the variable capacitor of the VBT network is implemented with a two-bit switching capacitor array to minimize the nonlinearity caused by the variable capacitor [26]. A thick gate oxide transistor is used as the switching capacitor array, and the size is optimized to be operated within available voltage swing range for reliability. Fig. 7(b) shows the simulation result for maximum drain/source voltage swings of the switching transistor with respect to the PA operation. In order to avoid forwarding bias from body to drain or source while the switch is turned on, the transistor size should be large enough to make small drain voltage swing. However, due to large parasitic capacitance caused by

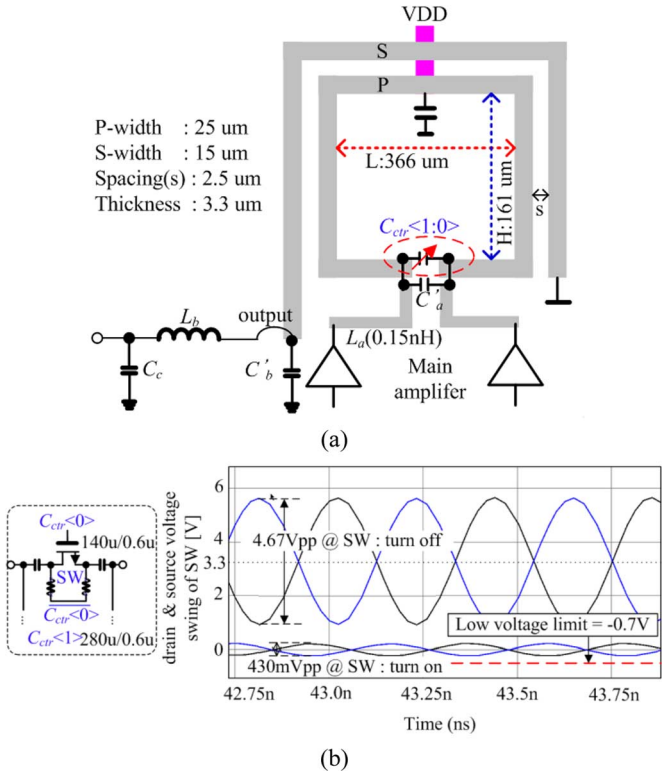


Fig. 7. (a) The layout of the VBT network, and (b) switching capacitor schematic and maximum V_{ds} voltage swings of that with respect to PA operation.

switching transistors, C'_a should be optimized to compensate for the parasitic capacitance by C_{ctr}. Ultimately, a switch size of 360 μm/0.35 μm was selected, and additional VBT insertion loss of 0.5 dB is caused by the turn-on resistance of C_{ctr}.

A simplified schematic of the designed PA is shown in Fig. 8 with the measurement setup. As shown in Fig. 8, differential cascode structures are used for the auxiliary and main amplifiers. The proposed VBT network is connected at the output stage of the main amplifier to serve as an impedance inverter. The power combination with the on-chip balun transformers of the main and auxiliary amplifiers is done with a current combining method, as implemented in a previous study [16]. Owing to the size reduction, the input transformer is implemented with an off-chip component, and a direct driving method is adopted without an additional power splitter. In addition, since the proposed Doherty PA does not require an additional phase compensation circuit, the overall implementation size is very small. The common gate transistors of each amplifier are implemented with a high breakdown voltage device ($L_{\min} = 0.35$ μm) to reduce the output voltage swing limitation. In addition, the common source transistors are implemented using an RF transistor with a minimum gate length of 0.13 μm to achieve a desirable RF performance. The common source gate bias of the auxiliary amplifier is set to 0.18 V for class C operation; this is below the threshold voltage of 0.3 V, whereas that of the main amplifiers is set to 0.4 V for class AB linear operation. Additionally, the gate bias of the common gate transistor for the main amplifier is set to 2.1 V to reduce the voltage stress on the common source transistors, whereas that for the auxiliary amplifier is adjusted from

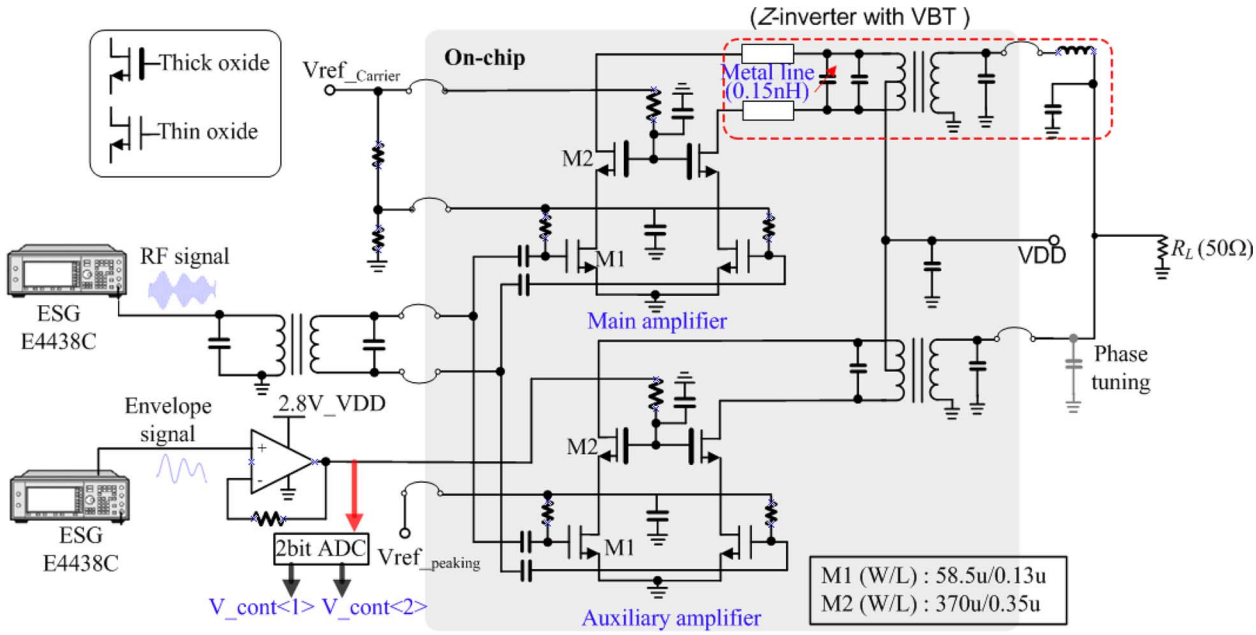


Fig. 8. Measurement environment and full schematic of the proposed Doherty amplifier.

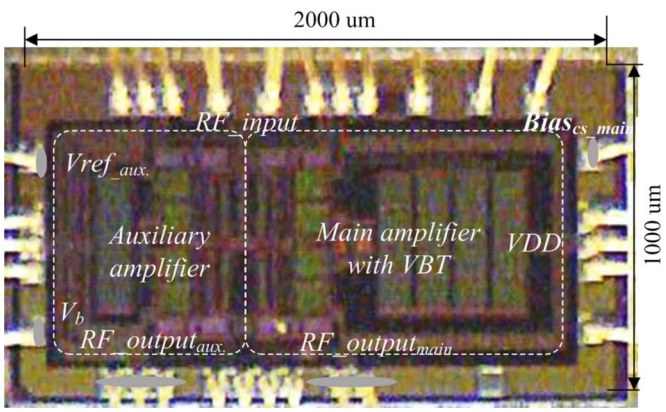


Fig. 9. Chip photograph of the implemented Doherty PA.

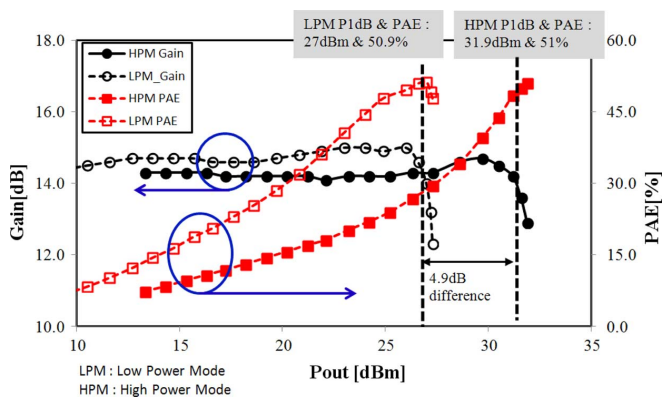


Fig. 10. In the switching mode, measured results for the power gain, PAE and output power (Pout) with the CW signal.

0 V to 2.8 V, or fixed at 2.8 V, as mentioned in Section III. The same transistor size is used in both amplifiers to achieve proper Doherty operation. A photograph of the implemented Doherty PA is shown in Fig. 9. The overall chip size, including the pads, is 2,000 × 1,000 μm^2.

B. Measured Results for the CW Signal

The fabricated Doherty PA chip is mounted on a FR-4 printed circuit board (PCB) and measured with a single tone continuous wave (CW) of 2.4 GHz. Fig. 10 shows the power gain and power-added efficiency (PAE) according to the output power. In the low-power mode (LPM), only the main amplifier is operated. Both the switching capacitor of VBT and the auxiliary amplifier are turned off in this case. However in the high-power mode (HPM), the main and auxiliary amplifiers are operated at a fixed bias level, and the switching capacitor of VBT is turned on. As shown in Fig. 10, the measured output power and PAE at a 1 dB compression point (P_{1dB}) in the LPM are 27 dBm and 50.9%, respectively, while those of the fabricated Doherty PA in the HPM are 31.9 dBm and 51%, respectively. Although the difference in the P_{1dB} between the HPM and LPM is 4.9 dB, two efficiency peak curves are obtained. Nonetheless, since the drain current consumption of the auxiliary amplifier with the fixed bias is too high at low power, the PAE of the amplifier is reduced rapidly at the transition power level from the LPM to the HPM. In order to reduce the drain current of the auxiliary amplifier at a low-power level, an adaptive bias scheme is used with the CG stage of the auxiliary amplifier and the switching capacitor of VBT according to the input power level, as shown in Fig. 11(a). With the adaptive bias scheme, the auxiliary amplifier is properly turned on at backed-off output power levels, as shown in Fig. 11(b). As a result, the drain current and gain of the auxiliary amplifier can be reduced effectively, leading to the ideal operation of the auxiliary amplifier in the low power region. The measured efficiency and power gain performances are illustrated in Fig. 12. The PAE of the proposed PA is greater than 25.3%, and the gain flatness is less than 1 dB in the backed-off output power region above 12 dB. If the adaptive bias scheme is turned on at higher input power, the efficiency will be better at backed-off power level. However, since

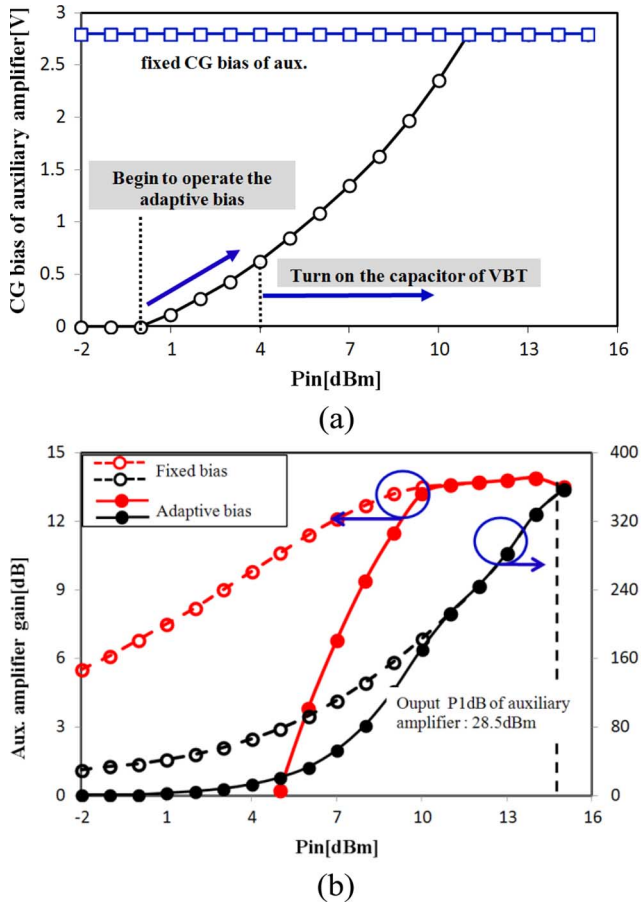


Fig. 11. (a) Aux. CG bias voltage shape in the fixed bias mode and the adaptive bias mode, and (b) measured power gain and drain current of the auxiliary amplifier with/without adaptive bias.

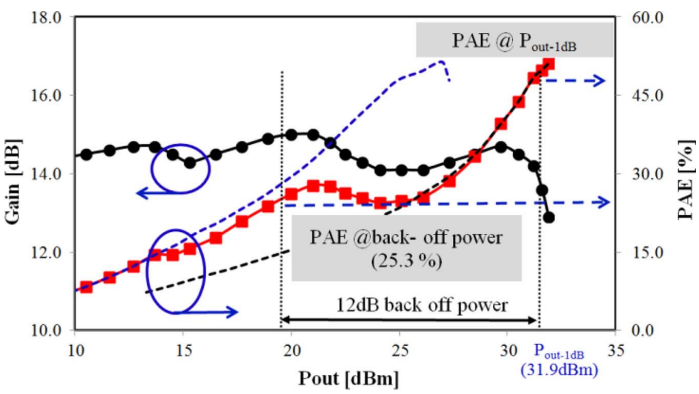


Fig. 12. Measured CW characteristics of the proposed Doherty amplifier with adaptive bias control.

the linearity and efficiency at backed-off power level should be concerned together, the turn-on power level of adaptive bias is determined by trade-off between efficiency and linearity. A two-tone test is performed at 2.4 GHz with a tone spacing of 5 MHz. The measured third-order IMD characteristics according to the output power are shown in Fig. 13. Relatively good linearity characteristics were obtained in the low-power region for the LPM case, whereas this was noted in the high-power region in the HPM case. For good linear operation with a third-order IMD of 28 dBc, the switching-mode PA must be changed from

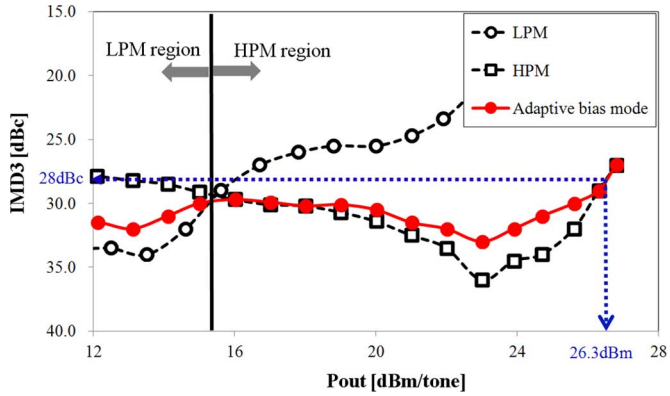


Fig. 13. Measured IMD3 performances for two-tone signals with a 5 MHz tone spacing at 2.4 GHz.

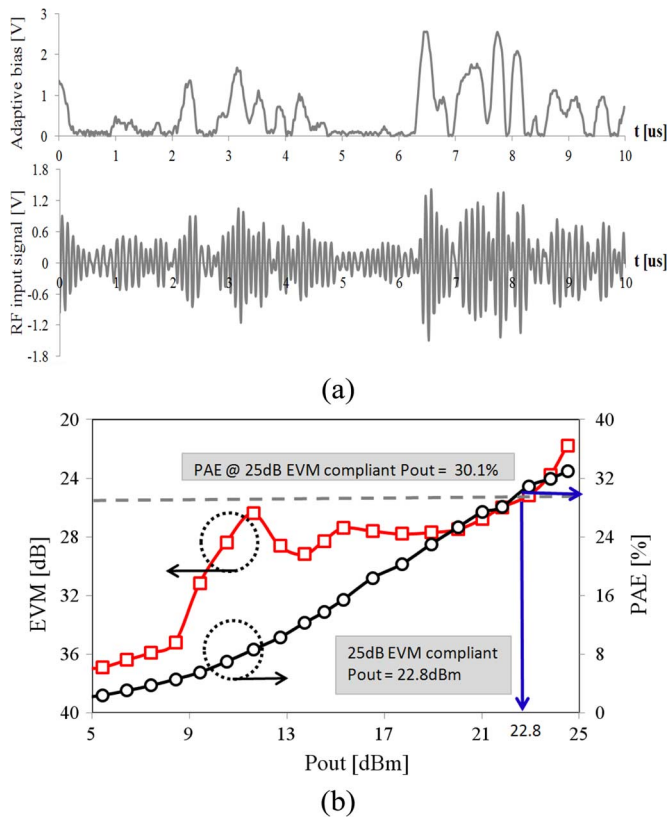


Fig. 14. (a) Measured CG stage gate bias of the auxiliary amplifier as compared to the modulated RF input signal amplitude for 802.11g WLAN and (b) measured EVM and PAE performances of the fabricated PA.

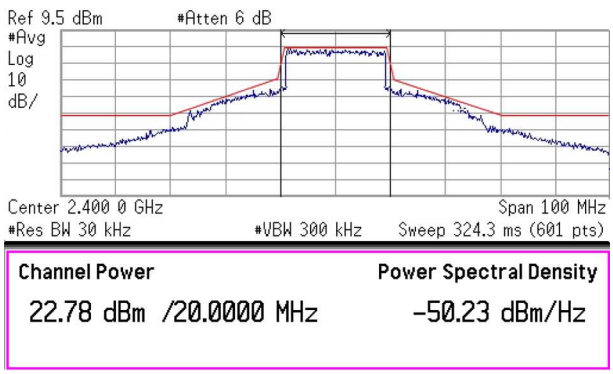
LPM to HPM at an output power of 15 dBm per tone. With the adaptive bias scheme, the fabricated Doherty PA can keep the IMD3 under 28 dBc up to an output power of 26.3 dBm per tone.

C. *Measured Results for the Modulation Signal*

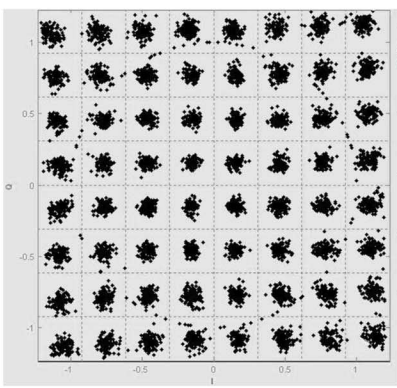
Finally, to verify whether the linearity characteristic of the fabricated Doherty PA is suitable for 802.11g WLAN system applications, a high-level modulation signal is applied. The modulation signal source used an OFDM signal with a data rate of 54 Mb/s using a 64 QAM. The measured CG stage-gate bias trace is compared with the OFDM modulated RF signal amplitude, as shown in Fig. 14(a). The CG stage-gate bias trace follows the envelope of the OFDM modulated RF signal well. The

TABLE I
COMPARISON OF CMOS PAS FOR WLAN APPLICATIONS

Ref.	Process	Supply	Frequency	P_{sat}	Peak PAE	P_{out} / PAE @ 25 dB EVM	Size
[9]	65 nm CMOS	3.3 V	2.4 GHz	31.5dBm	25%	22.7dBm / 16%	N/A
[10]	65 nm CMOS	3.3 V	2.4 GHz	33.5dBm	37.6%	26dBm / 20%	3 × 5 mm^2
[14]	90 nm CMOS	3.3 V	2.4 GHz	30.0dBm	33%	22.7dBm / 24%	2 × 2.1 mm^2
[16]	0.18μm CMOS	3.3 V	2.4 GHz	29.5dBm	41.7%	22dBm / 22%	1.4 × 1.1 mm^2
This work	0.13μm CMOS	3.3 V	2.4 GHz	31.9dBm	51%	22.8dBm / 30.1%	2 × 1.0 mm^2
* 801.11g specifications		1) Minimum EVM with a 64-QAM-OFDM signal (54 Mbps): 25 dB. 2) Maximum transmitted output power: 100mW (20dBm).					



(a)



(b)

Fig. 15. (a) Measured output spectrum mask of the amplifier, and (b) constellation error of the amplifier with 64 QAM OFDM.

EVM at 2.4 GHz is shown in Fig. 14(b). The measured average output power that satisfies the EVM requirement of 25 dB is around 22.8 dBm, where the PAE at the EVM compliant output power is 30.1%. The measured EVM is lower than the expected value based on CW or two tone test due to AM-PM performance degradation caused by discontinuous load modulation. However, the proposed amplifier demonstrates that it has high efficiency at an EVM compliant output power level of 25 dB.

Fig. 15(a) shows the output spectrum mask of the fabricated Doherty PA with a channel average power of 22.8 dBm and an adjacent channel leakage ratio (ACLR) of −25 dBc. In addition, the constellation error of the amplifier at an average output power of 22.8 dBm is shown in Fig. 15(b). As a result, the proposed Doherty PA satisfies the system specifications of 801.11g without a digital pre-distortion (DPD) algorithm.

The electrical performances of the fabricated Doherty PA are compared with previous research results in Table I. The performances of the proposed Doherty PA are superior to those shown in the Table in terms of PAE at an EVM compliant output power of 25 dB and at the peak power. Although the PAE performance of proposed Doherty PA, without considering actual input balun loss and on-chip matching loss, cannot be fairly comparable with previous works, those loss factors have a small impact on PAE. Therefore, the proposed Doherty PA can be a good candidate for a highly efficient CMOS power amplifier.

V. CONCLUSION

A conventional Doherty PA with a quarter-wavelength transformer has limitations in terms of CMOS implementation due to its size and bandwidth. The proposed VBT network is employed as a solution to overcome these limitations. In addition, an adaptive bias control technique necessary to obtain proper linearity and efficiency levels is demonstrated. The prototype achieves a peak power in excess of 31.9 dBm and satisfies the 802.11g linearity requirement up to an output power of 22.8 dBm. In addition, the measured results clearly show that the prototype is capable of superior efficiency levels for WLAN applications. Thus, the CMOS Doherty PA with VBT and an adaptive bias control technique is very effective for high-efficiency CMOS power amplifier designs for WLAN applications.

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