A Design of Reconfigurable Negative Group Delay Circuit Without External Resonators

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***Abstract*—In this letter, we present the novel design and implementation of a microstirp line reconfigurable negative group delay circuit (NGDC) using a branch-line. Theoretical analysis shows that reconfigurable characteristics in the proposed circuit can be obtained by properly choosing the characteristic impedances of the branch-line and tuning only the termination resistance. Therefore, the proposed reconfigurable NGDC does not require any extra resonators. For experimental validation, the proposed circuit was designed and fabricated for a wideband code division multiple access downlink frequency operating at a center frequency (f_0) of 2.14 GHz. Measurement results show the group delays variation of -2 *ns* to -10 *ns* with signal attenuation variation of -25 *dB* to -36.6 *dB* at f_0. For enhancement of the negative group delay bandwidth, two NGDCs operating at slightly different center frequencies are cascaded and measured.**

***Index Terms*—Branch-line structure, negative group delay, reconfigurable, transmission line.**

I. Introduction

WITHIN finite frequency, the negative group delay (NGD) phenomenon is observed where the absorption or signal attenuation (SA) is maximum [1]; therefore, lossy bandstop resonators are used to realize the negative group delay circuit (NGDC). Based on lumped elements series/shunt *RLC* resonators or lossy transmission line (TL) resonators, various types of single and dual-band active/passive NGDCs have been presented with or without tunability [2]–[11]. Among the passive NGDCs, the reflection-type NGDCs are widely used [4]–[10]. However, the NGD phenomenon in these circuits is generated within *RLC* tuned reflection termination circuit, not within hybrids. Moreover, these works have ignored 90° hybrids in their analyses. Recently, the NGDCs based on a microwave transversal filter approach that do not require any lossy resonators have been reported [12]–[14].

In this letter, we propose a reconfigurable microstrip line NGDC based on a branch-line. The proposed NGDC requires no extra resonators. The reconfigurable characteristics can be obtained by properly choosing the characteristic impedances of the branch-line and changing only the termination resistances, without any tuning of the resonating LC element values [4], [5], [7], [8].

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II. Mathematical Analysis

Fig. 1 shows the structure of conventional and proposed reconfigurable NGDC. The proposed structure consists of a branch-line, where direct and coupled ports are terminated with variable resistors R. Since this structure is symmetrical about the AA' plane, even- and odd-mode analys can be applied to determine the S-parameters. Fig. 2(a) and (b) show the equivalent circuits of the proposed structure under even-and odd-mode excitations. Using the equivalent circuits, the reflection and transmission coefficients of the proposed structure can be found as shown in (1), where f and f_0 are the operating and design center frequencies

$$S_{11} = S_{22} = \frac{Y_0^2 - Y_{ino}Y_{ine}}{(Y_0 + Y_{ine})(Y_0 + Y_{ino})} \tag{1a}$$

$$S_{21} = \frac{(Y_{ino} - Y_{ine})Y_0}{(Y_0 + Y_{ine})(Y_0 + Y_{ino})} \tag{1b}$$

where

$$Y_{ine} = \frac{j}{Z_a}\tan\frac{\pi f}{4f_0} + \frac{\frac{1}{R} + \frac{j}{Z_a}\tan\frac{\pi f}{4f_0} + \frac{j}{Z_b}\tan\frac{\pi f}{2f_0}}{Z_b\left\{\frac{1}{Z_b} + j\left(\frac{1}{R} + \frac{j}{Z_a}\tan\frac{\pi f}{4f_0}\right)\tan\frac{\pi f}{2f_0}\right\}} \tag{2a}$$

$$Y_{ino} = -\frac{j}{Z_a}\cot\frac{\pi f}{4f_0} + \frac{\frac{1}{R} - \frac{j}{Z_a}\cot\frac{\pi f}{4f_0} + \frac{j}{Z_b}\tan\frac{\pi f}{2f_0}}{Z_b\left\{\frac{1}{Z_b} + j\left(\frac{1}{R} - \frac{j}{Z_a}\cot\frac{\pi f}{4f_0}\right)\tan\frac{\pi f}{2f_0}\right\}} \tag{2b}$$

and $Z_0 = 1/Y_0$ is a reference port impedance. For perfectly matched S_{11} and S_{22} at $f = f_0$, the value of Z_a and Z_b are found as (3)

$$Z_a = Z_0 \tag{3a}$$

$$Z_b = Z_0/\sqrt{2}. \tag{3b}$$

The magnitudes of S-parameters and group delay (GD) at $f = f_0$ can be determined as (4) by using (1)-(3)

$$S_{11}|_{f=f_0} = S_{22}|_{f=f_0} = 0 \tag{4a}$$

$$S_{21}|_{f=f_0} = \left|\frac{Z_0 - R}{Z_0 + R}\right| \tag{4b}$$

$$\tau|_{f=f_0} = -\frac{1}{2\pi f}\frac{d\angle S_{21}}{df}\bigg|_{f=f_0} = -0.6036\frac{\left(3R^2 - Z_0^2\right)}{f_0\left(Z_0^2 - R^2\right)} \tag{4c}$$

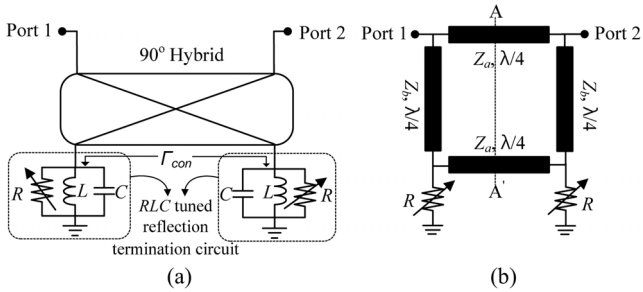

Fig. 1. Diagram of reconfigurable negative group delay circuits: (a) conventional and (b) proposed structure.

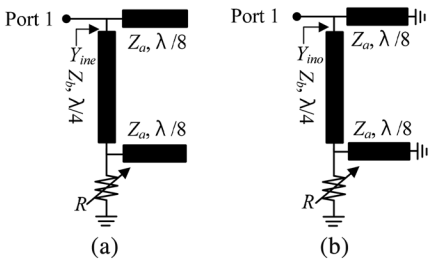

Fig. 2. (a) Even- and (b) odd-mode decompositions of the proposed reconfigurable negative group delay circuit.

As seen from (4c), the GD depends on R and Z_0. Moreover, the value of GD can be tuned by changing R only when the characteristic impedances of the branch-line (i.e, Z_a and Z_b) are fixed.

For better understanding of (4), the calculated normalized GD (τf_0), the magnitude of S_{21} are plotted in Fig. 3 for different values of R. As seen in this figure, the NGD is obtained in the region of $R < 50\ \Omega$. In the region of $R > 50\ \Omega$, the proposed circuit provides the positive GD. Similarly, the magnitude of S_{21} is also a function of R. As seen from figure, the SA (S_{21}) is increased as the maximum achievable NGD increases.

For illustration, the frequency responses (GD, magnitude of S_{21}, and input/output return losses) of the proposed circuit are calculated and plotted in Fig. 4 for different values of R. Here, the values of Z_a and Z_b are fixed as 50 Ω and 35.35 Ω, respectively. As seen in this figure, the GD is tuned from -1 ns to -10 ns with the S_{21} variation of -20.64 dB to -37.60 dB by changing only the value of R. In this case, the return losses are higher than 60 dB at f_0. Therefore, the proposed circuit provides reconfigurable NGD characteristics without using any extra resonators.

III. Simulation and Measurement Results

For experimental verification, we designed and fabricated the proposed microstrip line NGDC for a wideband code division multiple access downlink band operating at f_0 of 2.14 GHz. The circuit is fabricated on Rogers RT/Duriod 5880 substrate with a dielectric constant (ε_r) of 2.2 and a thickness (h) of 31 mils. In this work, the variable resistors are implemented with PIN diodes HSMP-4810 from Avago. Fig. 5(a) presents the circuit diagram of PIN diode which functions as a current-controlled variable resistor at microwave frequencies. To compensate the parasitic components of the PIN diode such that their input impedance is purely resistive, the PIN diode is terminated in TLs of length L_1 and L_2 as shown in Fig. 5(b). The design

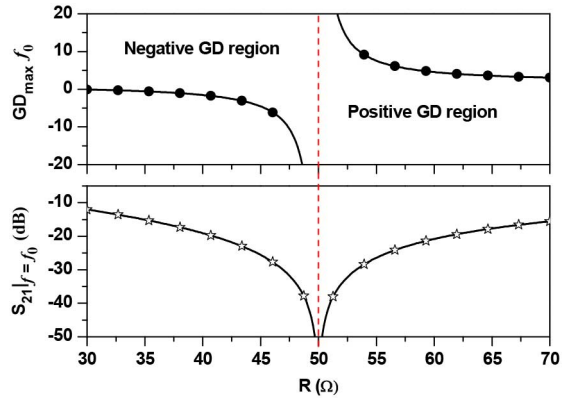

Fig. 3. Calculated normalized group delay (τf_0) and magnitude S_{21} at center frequency according to R.

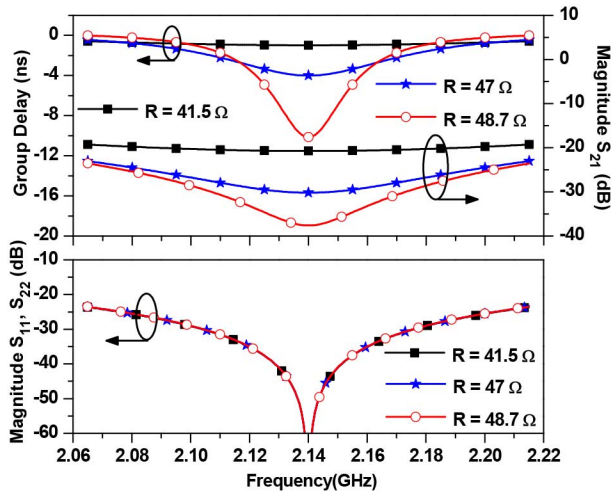

Fig. 4. Calculated group delay and S-parameters for different values of R with $Z_a = 50\ \Omega$ and $Z_b = 35.35\ \Omega$.

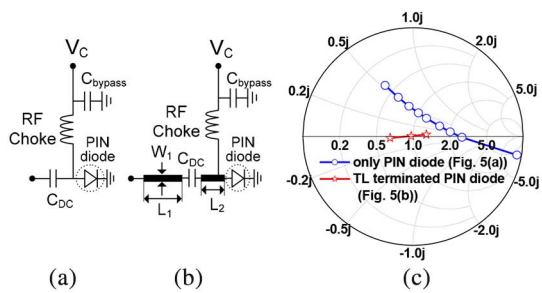

Fig. 5. (a) PIN diode, (b) transmission line terminated with PIN diode [7], [8], and (c) measured reflection coefficients of the PIN diode at $f_0 = 2.14$ GHz.

equations are presented in [7]and [8]. Here, the main purpose of DC-block capacitor (C_{DC}) is to block DC-current and this may be in series connection with parasitic inductance of PIN diode. However, the circuit is not operating at resonance in this case and TLs are purely used for compensating parasitic components of PIN diodes. The physical dimensions of circuit shown in Fig. 5(b) are determined as $L_1 = 14.4$ mm, $L_2 = 0.88$ mm, $W_1 = 0.88$ mm, $C_{DC} = 0.2$ pF, and $C_{bypass} = 18$ pF.

Fig. 5(c) shows the measured reflection characteristics of a PIN diode [refer to Fig. 5(a)] and a TL terminated PIN diode

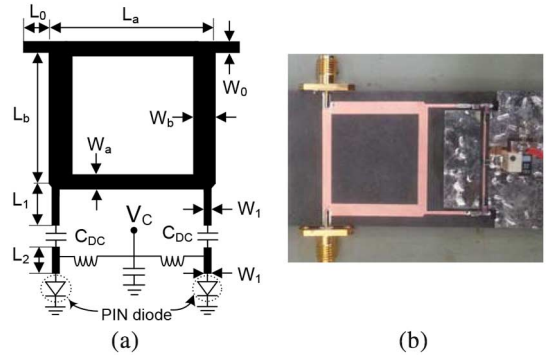

Fig. 6. (a) Simulation layout and (b) a photograph of fabricated negative group delay circuit.

TABLE I
PHYSICAL DIMENSIONS OF FABRICATED 1-STAGE CIRCUIT (UNITS: MILLIMETERS). REFER TO FIG. 6(A)

L_a	W_a	L_b	W_b	L_0	W_0	L_1	L_2	W_1	C_{DC} (pF)
27.6	2.4	26.4	3.9	5	2.4	14.4	4	0.88	0.2

[refer to Fig 5(b)]. These measurement results show that the variable resistance of the TL terminated with a PIN diode is obtained with almost zero imaginary parts by tuning the bias voltage.

In order to implement the overall circuit of the proposed reconfigurable NGDC, TL terminated PIN diode is integrated with the branch-line coupler. For this purpose, the characteristic impedances (Z_a and Z_b) and electrical lengths of the TLs of the branch-line coupler are determined as 50 Ω, 35.35 Ω, and 90° at $f_0 = 2.14$ GHz, respectively. Fig. 6(a) shows the layout of implemented reconfigurable NGDC. The physical dimension of the branch-line coupler was optimized using electromagnetic (EM) simulator Ansys HFSS 2014 to minimize effect of parasitic junction capacitance between transmission lines. In order to obtain reconfigurable GD from -1 to -10 ns, the resistance should be varied from 41 to 48.8 Ω. Since the equivalent circuit of PIN was difficult to implement in HFSS, the co-simulation was performed using HFSS and ADS 2013. For this purpose, the response of branch-line was determined by using HFSS and then used data in ADS to simulate the overall circuit. The physical dimensions of circuit are given in Table I after optimization. A photograph of the fabricated circuit is shown in Fig. 6(b).

Fig. 7 shows the simulation and measurement results of the proposed circuit and a comparison with the simulation results for ideal circuits. As the figure shows, the measurement and simulation results are in good agreement. The GD varied from -2 ns to -10 ns with SA variation from -25.57 to -36.56 dB at $f_0 = 2.143$ GHz, achieved by changing the bias-voltage 0.662 V to 0.68 V of the PIN diodes. The NGD bandwidth (bandwidth of NGD < 0 ns) is determined as 45 MHz. The input/output return losses are higher than 19 dB at f_0. The center frequency of maximum return losses are slightly moved toward lower frequencies which may be due to parasitic junction capacitance of branch-line.

One way to enhance the NGD bandwidth is to cascade several NGDCs with slightly different center frequencies [2], [6],

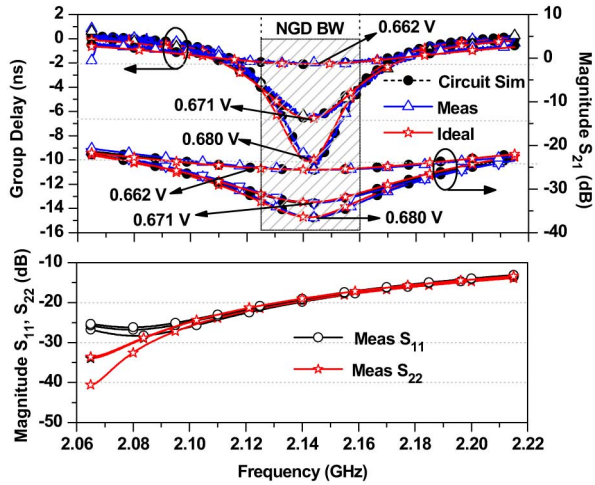

Fig. 7. Simulation and measurement of 1-stage reconfigurable NGDC.

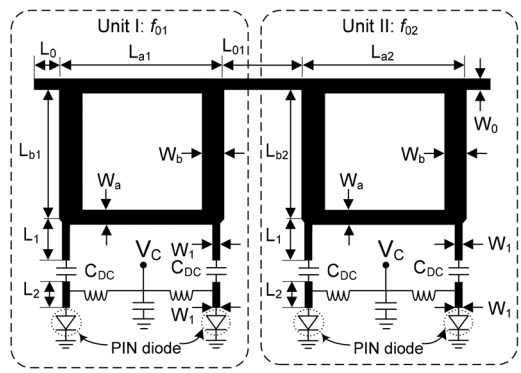

Fig. 8. Physical layout of cascaded 2-stage reconfigurable NGDC.

[10]as shown in Fig. 8. For this purpose, two different NGDCs are designed at $f_{01} = 2.10$ GHz and $f_{02} = 2.16$ GHz, respectively. The physical dimensions of cascaded 2-stage reconfigurable NGDC are shown in Table II.

The measurement results for the cascaded 2-stage NGDCs are given in Fig. 9. As the figure shows, the maximum achievable NGD is tuned from -2.23 ± 0.03 ns to -6.94 ± 0.9 ns over a bandwidth of 130 MHz, which is defined as the bandwidth region where the GD is negative. Similarly, the SA is tuned from -45.23 to -60.4 dB at $f_0 = 2.13$ GHz. The SA can easily be compensated for by using general purpose gain amplifiers. Compared to the 1-stage results presented in Fig. 7, 2-stage NGDC has wider NGD bandwidth, indicating its practical applicability.

The measured phase of S_{21} and input/output return losses are shown in Fig. 10. As seen in this figure, the slope of the phase is positive over a certain region. This positive phase slope parameter can be used to cancel out the negative phase slope to obtain zero GD or phase compensated response. The measured input and output return losses are higher than 18.8 dB at f_0 for the overall tunable range. The performance comparison of the proposed circuit is shown in Table III. As seen from this table, the proposed circuit provides the reconfigurable NGD characteristics without any extra resonators, which make the proposed circuit simpler. The proposed design method is very simple and

TABLE II
PHYSICAL DIMENSIONS OF FABRICATED 2-STAGE CIRCUIT (UNITS:. MILLIMETERS). REFER TO FIG. 8

L_{01}	L_{a1}	L_{a2}	L_{b1}	L_{b2}	W_a	W_b	L_0	W_0	L_1	L_2	W_1	C_{DC} (pF)
12	28.8	27.2	28.6	27.1	2.4	3.9	5	2.4	14.4	4	0.88	0.2

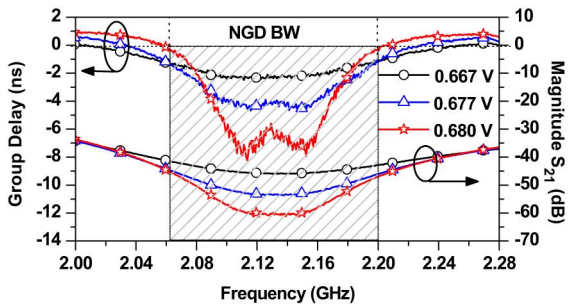

Fig. 9. Measurement results of cascaded 2-stage reconfigurable NGDC.

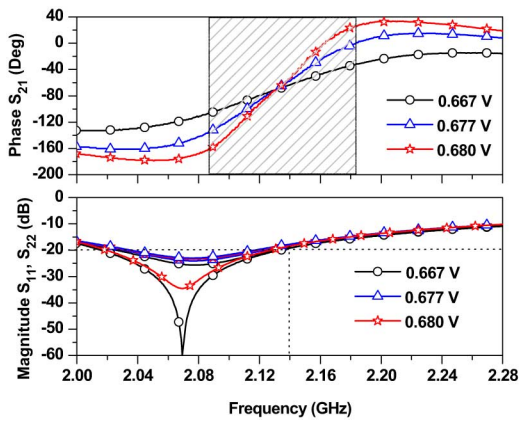

Fig. 10. Measured phase and return losses characteristics of cascaded 2-stage reconfigurable NGDC.

TABLE III
PERFORMANCE COMPARISON

	f_0	GD (ns)	S_{21max} (dB)	NGD BW (MHz)	A	Structure
[4], [5]	1.0	-1 to -10	-20 to -35	40	Y	
[7], [8]	2.14	-2 to -10	-28.5 to -40.2	35	Y	
[10]	2.14	-6.16	-8.65	15	Y	
[12]*	1.0	-2.5 to -4	Up to -10	200	N	
This work	**2.14**	**-2 to -10**	**-23.2 to -36.6**	**45**	**N**	

A: Extra series/parallel LC resonator required.
Y/N: Yes/No.
*: Active negative group delay with loss compensated.

can easily be extended for designing multiband reconfigurable NGDC. The proposed circuit can be applied to eliminate the beam-squint in serially fed antennas arrays [15].

IV. CONCLUSION

In this letter, we propose a microstrip line reconfigurable negative group delay circuit. The proposed circuit is based on a branch-line that does not require any extra resonators. The optimum design method is explained based on the derived general design equations. The reconfigurable frequency response characteristics (group delay and magnitude characteristics) are obtained by simply tuning the bias voltage of the PIN diodes. For enhancement of the negative group delay bandwidth, two negative group delay circuits operating at slightly different center frequencies are cascaded, demonstrated a practical applicability. The proposed circuit is expected to be applicable in multiple input multiple output (MIMO) antennas for minimizing the correlation between adjacent antennas.

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