A Fully Integrated High Efficiency RF Power Amplifier for WLAN Application in 40 nm Standard CMOS Process

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***Abstract*—This paper proposes a CMOS linear power amplifier (PA) design scheme for IEEE 802.11g (WLAN) application. The proposed PA consists of a programmable gain amplifier and a high power stage which is composed of a main amplifier with class AB bias and an auxiliary amplifier with class C bias. Based on the un-even bias scheme, the power stage can improve linearity and reduce current consumption in the low power region. It is fabricated with a TSMC 40 nm standard RF CMOS process. The measurements show that the designed PA reaches a 1 dB gain compression output power of 24.6 dBm and a peak drain efficiency of 38% with a 3.3 V power supply at 2.4 GHz operating frequency range. When the PA was tested with an IEEE 802.11g OFDM signal of 20 MHz channel bandwidth, the obtained −25 dB EVM compliant output power and drain efficiency are 18.5 dBm and 14%, respectively.**

***Index Terms*—CMOS power amplifier, efficiency enhancement, high efficiency, linear power amplifier, linearization, OFDM, WLAN.**

I. Introduction

THE growing demands for the low cost and small size implementation led to the highly integrated system-on-chip (SoC). According to these demands, many RF chip designers have sought to enhance transceiver integration by using low-cost CMOS technology. However, RF power amplifiers (PAs) are a major roadblock in these efforts to create highly integrated SoC, due to both the low breakdown voltage of the transistor and lossy substrate associated CMOS technology. In particular, the PAs for high data rate wireless communication systems have been required high efficiency and good linearity at the backed-off power levels to efficiently amplify a multiplexing signal with a high peak-to-average power ratio. Although many CMOS PA techniques for enhancement of efficiency and linearity have been introduced, PAs with the scaled-down CMOS technology still face many obstacles to reliable operation, such as hot carrier injection and time-dependent dielectric breakdown problems. Despite these problems, many studies for PAs using the standard deep-submicron CMOS process have been performed, since it is beneficial that the CMOS PAs can be readily integrated with various other control circuits in a transmitter [1]–[3].

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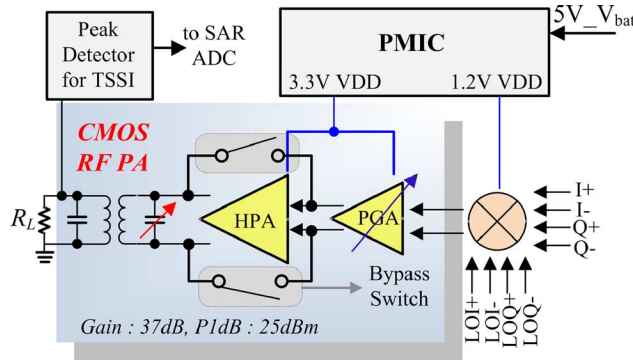

Fig. 1. Simplified block diagram of fully integrated power amplifier.

Thus, this paper describes some improved PA design techniques to realize high power and high efficiency in a small area using the standard 40 nm CMOS technology for 802.11g orthogonal frequency division multiplexing (OFDM) application. The designed PA consists of a high power amplifier (HPA) for high linear operation, a programmable gain amplifier (PGA) for output power adjustment, and bypass switches to support the external PA mode, as shown in Fig. 1. In addition, an internal balun is designed for impedance transforming and for combining differential output signals to a single load (R_L). The configuration and the operation principle of the proposed un-even biased HPA are described in Section II-A, and the amplifier design consideration for reliable operation is presented in Section II-B. Section III describes all of the measurement results and the last Section IV provides the conclusion of this paper.

II. Design and Implementation

A. Operation Principle of Proposed HPA

Fig. 2 shows the operation principle of an un-even biased HPA. This HPA is a pseudo-differential amplifier with a cascode configuration. A 3.3 V thick gate oxide transistor is used for the common gate (CG) stage to avoid the breakdown issue, whereas a thin gate oxide transistor with a minimum gate length of 40 nm is used for the common source (CS) stage to obtain the maximum RF gain. In addition, the transistors of the CS stage are separated into main transistor (M_1) and auxiliary transistor (M_2), and the gates of M_1 and M_2 transistors are biased

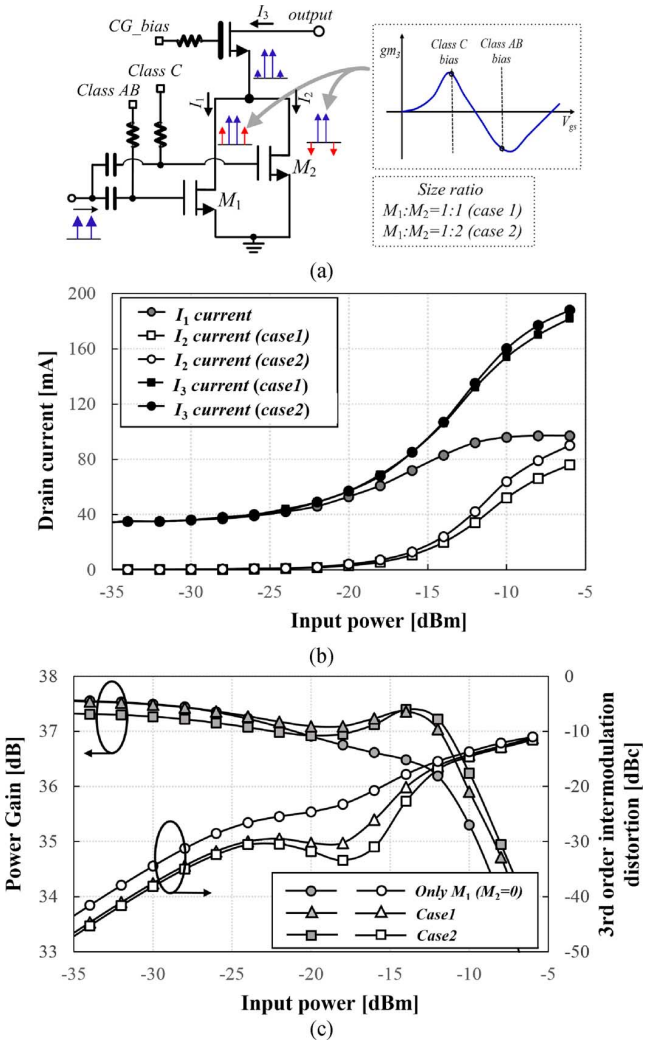

Fig. 2. (a) Simplified schematic of HPA and principle of g_{m3} cancellation, (b) simulated drain current flow curves for each transistors, and (c) simulated power gain and 3rd order intermodulation distortion curves as function of M_2 transistor size (with 5 MHz tone spacing).

at class AB of 0.65 V and class C of 0.15 V, respectively. Although M_1 and M_2 transistors have different nonlinear characteristics, the generated third harmonics have opposite polarities and the third harmonic nonlinearities are cancelled out by opposite phase combination, as shown in Fig. 2(a) [4], [5]. In addition, since M_2 does not consume the current at the low power region by a gate bias voltage that is lower than the threshold voltage (V_{th}), the average efficiency of the PA can be improved in the overall power range. However, since the transconductance (g_m) of M_2 is smaller than that of M_1, the size of M_2 should be optimized to obtain the proper linearization effect. Fig. 2(b) and (c) show the simulated drain current and power gain curves of the designed PA, respectively. In addition, the simulated 3rd order intermodulation distortion characteristics according to the input power levels are shown in Fig. 2(c). As a result, the proposed technique can improve the average efficiency and linearity simultaneously by using differently biased M_1 and M_2 transistors with a 1:2 size ratio.

B. Fully Integrated CMOS PA Circuit

Fig. 3 shows an overall schematic of the designed CMOS PA. As shown in Fig. 3(a), the gate widths of the CS and CG stages

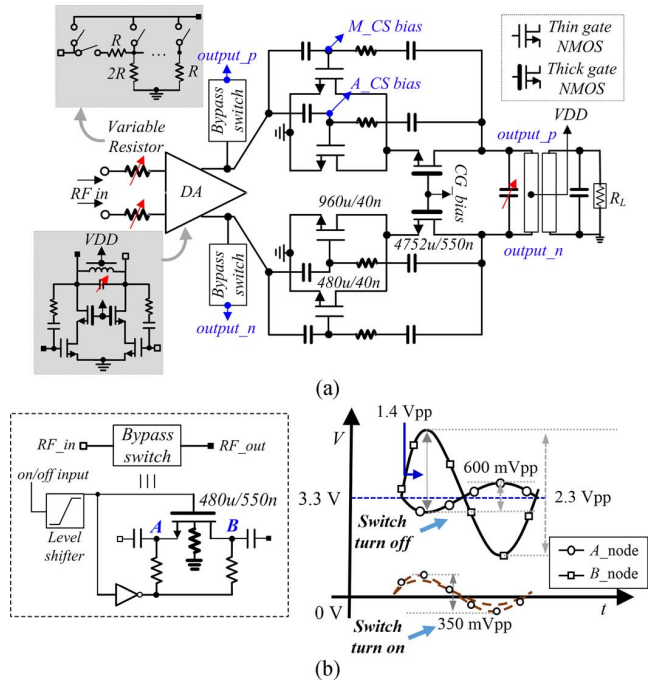

Fig. 3. (a) Overall schematic of the designed CMOS power amplifier, (b) bypass switch and drain/source voltage swings as function of on/off operation. (Turned off: at 25 dBm output power, turned on: at −5 dBm output power).

in the HPA are 1440 μm and 4750 μm, respectively. To avoid linearity degradation caused by large voltage swing at the drain node of the CS stage, the gate width of the CG stage is chosen to have low input impedance. The programmable gain amplifier (PGA) is implemented by employing a variable resistor at the input stage of the drive amplifier (DA). The DA is designed to be available for a 3.3 V supply voltage and to support enough linear power with an OIP_3 of 22 dBm. The variable resistor for the RF gain control of 18 dB is realized with ladder type 2-bit resistors so that the output power of the CMOS PA can be controlled by 6 dB step. Finally, the implementation of a bypass switch connected at the HPA output node is very challenging due to reliability problems. When the bypass switch is turned off and the HPA is turned on, the drain node of the switch transistor has a large voltage swing, and it leads to a forwarding bias between the body and drain nodes. To address these reliability issues of the switch transistor, it has been designed to fix the DC bias at the drain/source nodes according to the on/off operations, as shown in Fig. 3(b). The output internal balun is designed using the EMX tool so that a differential impedance of 20 Ω is transformed to a single output impedance of 50 Ω.

III. Measurement

The proposed CMOS PA was fabricated in the standard 40-nm CMOS process and was packaged in a flip-chip chip-scale package (FcCSP). The test board and chip photographs of the PA are shown in Fig. 4. The two stage PA is implemented in a small area of 0.57×0.97 mm^2 including the output balun and bypass switch, so that additional off-chip matching components are not required. The fabricated PA is mounted on an FR-4 printed circuit board for the measurement.

The measured output power and drain efficiency (DE) curves by TX gain control bit are shown in Fig. 5(a). The RF output

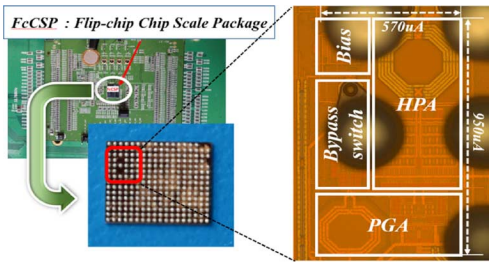

Fig. 4. Photographs of the designed WLAN SoC with FcCSP package and fabricated CMOS PA chip.

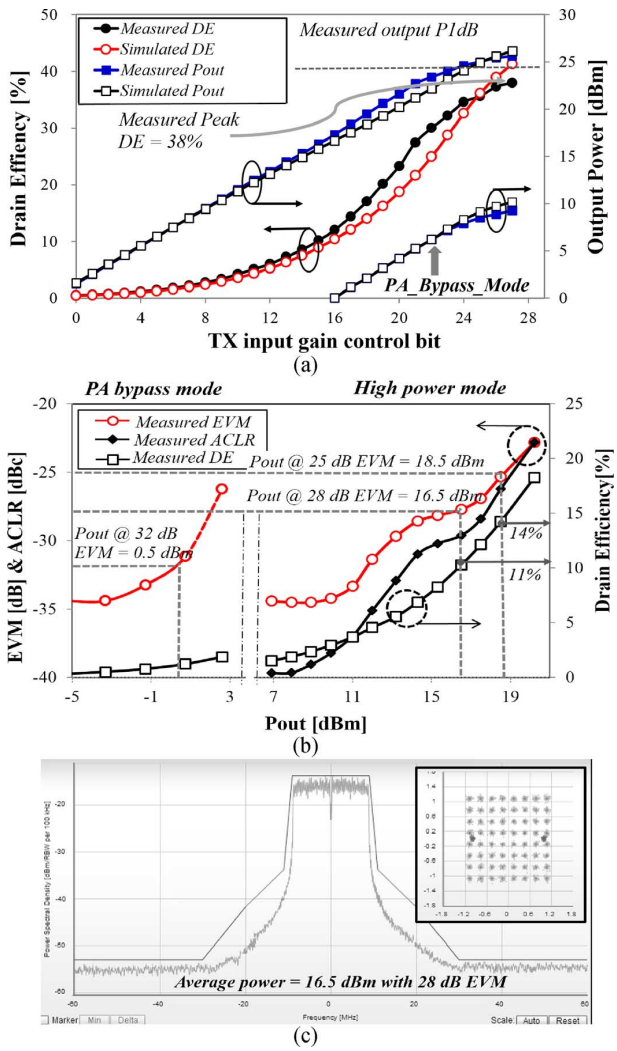

Fig. 5. Measurement results: (a) output power and drain efficiency performances of PA on-mode and bypass mode with a continuous wave of 2.445 GHz, (b) EVM, ACLR, and drain efficiency performances of both modes with WLAN 802.11g 54 Mbps 64-QAM OFDM signal, and (c) measured spectrum and constellation error at 16.5 dBm output power.

power was adjusted by using an analog variable gain amplifier and RF PGA, and the measurement was performed with a continuous wave single tone at a center frequency of 2.445 GHz. The fabricated PA achieves a 1-dB compression output power of 24.6 dBm with a peak DE of 38%. In addition, the PA performance shows a close agreement between the simulated and measured results by achieving a small signal gain of 37 dB.

TABLE I
COMPARISON OF WLAN CMOS PAS (WITHOUT DPD)

	Ref. [5]	Ref. [6]	This work
Small signal gain	33.5 dB	22 dB	37 dB
Peak PAE	37.6%	34.9%	38% (DE)
Pout at -25dB EVM	24 dBm	24 dBm	18.5 dBm
PAE at -25dB EVM	14%	14%	14% (DE)
Size	6 mm^2	6 mm^2	0.54 mm^2
Technology (CMOS)	65nm	65nm	40nm

Finally, to verify the linear characteristic of the fabricated PA, the OFDM signal with a 20 MHz channel bandwidth of 802.11g WLAN was applied. Fig. 5(b) shows the measured error vector magnitude (EVM) and the DE characteristics of the high power mode and the PA bypass mode according to the output power level. The maximum output power satisfying the 802.11g linearity specifications with the EVM of −25 dB was 18.5 dBm with a DE of 14%. The output spectrum mask and constellation error at 16.5 dBm output power are shown in Fig. 5(c). The PA consumes the quiescent current of 101 mA (35 mA in the DA stage and 66 mA in the HPA) from the 3.3 V supply voltage. The performance of the designed PA is compared to other state-of-the-art linear CMOS PAs in Table I [6]. By using the proposed scheme in this work, the PA was achieved good efficiency in a small area.

IV. CONCLUSION

This paper presents a two stage highly efficient and linear CMOS power amplifier using a standard 40 nm CMOS process. The fabricated power amplifier demonstrates suitable linearity, low current consumption, and enhanced average efficiency for 802.11g WLAN application. High performance results can be obtained from a destructive summation of nonlinear factors caused by the un-even biasing technique. In addition, the PA can be implemented in a small area since the un-even biasing strategy does not require any additional area. As a result, the PA can be integrated in a SoC chipset and can operate appropriately for use in 802.11g WLAN systems.

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