A Design of Power Divider With Negative Group Delay Characteristics

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***Abstract*—In this letter, the design of power divider with negative group delay (NGD) characteristics is presented. From an analysis, the NGD associated with different transmission paths is found to be identical and obtained by loading resistor connected short-circuited coupled lines with an open-circuited isolation port. The proposed structure is validated by constructing a two-way microstrip line power divider with equal power division ratio, which is centered at 2.14 GHz. The measured results show excellent agreement with simulations and theoretically predicated results. From the measurement, the group delays and magnitudes of S-parameters between the different transmission paths are determined as -1.16 ns, -9.29 dB, -1.17 ns, and -9.30 dB. The measured input/output return losses and isolation at center frequency are higher than 28.92 dB, 26.76 dB, and 42.2 dB.**

***Index Terms*—Coupled line, microstrip line, negative group delay (NGD), power divider.**

I. Introduction

POWER dividers are key components in microwave circuits and have been widely used for various applications in wireless communication and radar systems such as high power amplifiers, mixers, and antenna feeding networks [1], [2]. The different aspects of the power dividers have been studied in the past decades, including unequal and tunable power division ratio, bandwidth enhancement, circuit miniaturization, and multi-band operation [3]–[6]. However, the investigation of the group delay in these circuits is lacking. Moreover, the conventional power dividers can provide only positive group delay [7].

In recent years, there has been an increasing amount of research on active/passive negative group delay (NGD) circuits at microwave frequencies [8]–[13], which have been applied in various applications. It is crucial to minimize the time mismatch between the envelope and the RF paths in supply modulated power amplifiers to minimize the nonlinearity [14]. Therefore, the research that can demonstrate the power divider with NGD characteristics through different transmission paths would be promising for the compensating group delay in the supply modulated power amplifiers. In this letter, the microstrip line power divider with the specified NGD is studied systematically and completely including its analysis and realization configuration.

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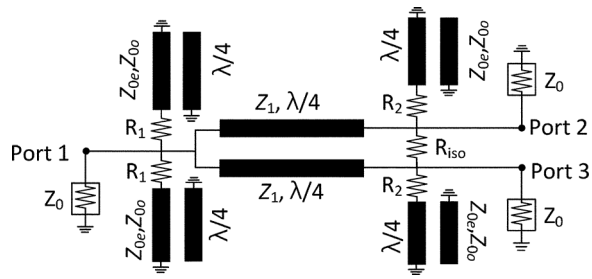

Fig. 1. Proposed circuit diagram of the power divider with negative group delay.

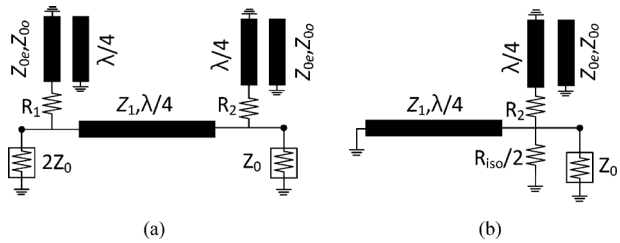

Fig. 2. (a) Even- and (b) odd-mode decomposition of the proposed power divider.

II. Mathematical Analysis

The schematic of the proposed power divider with negative delay is shown in Fig. 1, which consists of $\lambda/4$ series transmission lines loaded with shunt resistor connected $\lambda/4$ short-circuited coupled lines. Since the structure is symmetrical, the even- and odd-mode analyses are performed to analyze and determine the circuit values of the proposed circuit [15]. The even- and odd-mode equivalent circuits are shown in Figs. 2(a) and 2(b). The scattering parameters of the power divider can be expressed in terms of the even- and odd-mode scattering parameters as

$$S_{11}(f) = S_{11e}(f) \tag{1a}$$

$$S_{21}(f) = S_{12}(f) = S_{31}(f) = S_{13}(f) = \frac{S_{21e}(f)}{\sqrt{2}} \tag{1b}$$

$$S_{22}(f) = S_{33}(f) = \frac{S_{22e}(f) + S_{22o}(f)}{2} \tag{1c}$$

$$S_{23}(f) = S_{32}(f) = \frac{S_{22e}(f) - S_{22o}(f)}{2}. \tag{1d}$$

For zero reflection from all three ports ($S_{ii} = 0$) and infinite isolation between ports 2 and 3 ($S_{23} = 0$) at the center frequency (f_0), the following relations can be found:

$$R_1 = 2R_2 \tag{2a}$$

$$Z_1 = \sqrt{\frac{2R_1R_2Z_0^2}{(R_1 - 2R_2)Z_0 + R_1R_2 - 2Z_0^2}} \tag{2b}$$

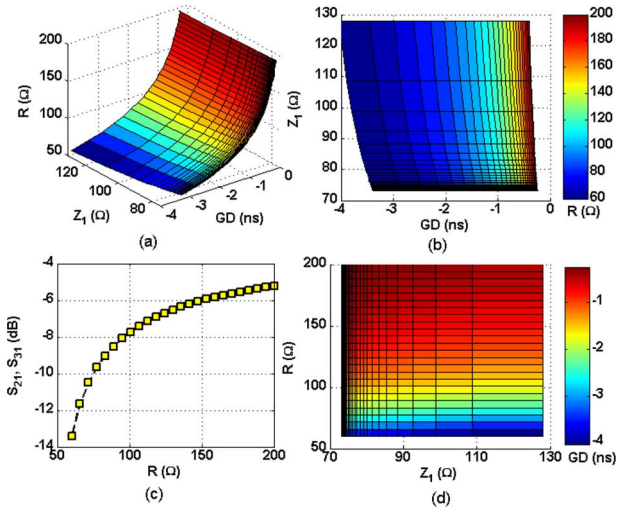

Fig. 3. Calculated group delay (GD), magnitude S_{21}, S_{31}, Z_1, and R for zero reflection coefficients and infinite isolation with $Z_c = 600\ \Omega$ and $C_{eff=} -15$ dB at $f_0 = 2.14$ GHz: (a) 3-D plot, (b) GD according to Z_1 with color bar representing values of R, (c) magnitude of S_{21}, S_{31} according to R, and (d) relation between R and Z_1 with color bar denoting different GDs.

$$R_{iso} = \frac{(R_1 + 2Z_0)Z_1^2}{Z_0 R_1} \tag{2c}$$

where Z_1 and Z_0 are the characteristics impedance of the series line and reference port impedance, respectively.

Furthermore, the magnitude of transmission coefficient and group delays (GDs) of different transmission paths at f_0 are found as (3) assuming $R_1 = 2R$ and $R_2 = R$

$$S_{21}|_{f=f_0} = S_{31}|_{f=f_0} = \left|\frac{2Z_0R^2Z_1}{(2RZ_0+R^2+Z_0^2)Z_1^2+2R^2Z_0^2}\right| \tag{3a}$$

$$\tau_{21}|_{f=f_0} = \tau_{31}|_{f=f_0} = -\frac{3}{4f_0}\left\{\frac{Z_c}{2RC_{eff}} - \frac{\begin{bmatrix}(R+Z_0)(2RC_{eff}Z_0+Z_1Z_c)\\ Z_1+2RZ_0^2Z_c\end{bmatrix}}{C_{eff}\begin{bmatrix}2R(2Z_0+R)Z_1^2\\ +2Z_0^2(Z_1^2+2R^2)\end{bmatrix}}\right\} \tag{3b}$$

where C_{eff} and Z_c are the coupling coefficient and equivalent characteristic impedance, respectively, of the shunt-connected short-circuited coupled lines. The Z_c of the short-circuited coupled lines [15] can be expressed as

$$Z_c = \frac{2Z_{0e}}{\frac{Z_{0e}}{Z_{0o}} - 1} = Z_{0e}\frac{1 - C_{eff}}{C_{eff}} = Z_{0o}\frac{1 + C_{eff}}{C_{eff}} \tag{4}$$

where Z_{0e} and Z_{0o} are the even- and odd-mode impedances of the short-circuited coupled lines. As seen from (4), very high characteristic impedance Z_c can be obtained if the ratio of Z_{0e} to Z_{0o} is close to unity or C_{eff} becomes very small.

For illustrative understanding and design, the calculated GDs, Z_1 according to R are shown in Fig. 3 for zero reflections from three ports and infinite isolation. In this calculation, the Z_c and C_{eff} of the short-circuited coupled lines are assumed as 600 Ω and -15 dB, respectively. From 3-D plot shown in Fig. 3(a), the amount of GD and Z_1 are proportional to R. The variation of GD according to Z_1 is shown in Fig. 3(b), where color bar denotes values of R. As seen from this figure, the value of Z_1 becomes low value as GD moved toward higher negative value. The magnitude of transmission losses with respect to R is illustrated in Fig. 3(c). From this figure, it can be inferred that more

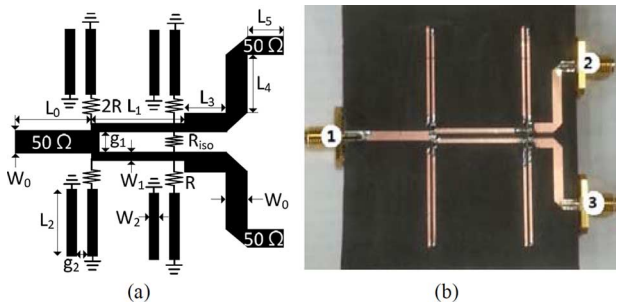

Fig. 4. (a) Simulation layout and (b) a photograph of fabricated circuit.

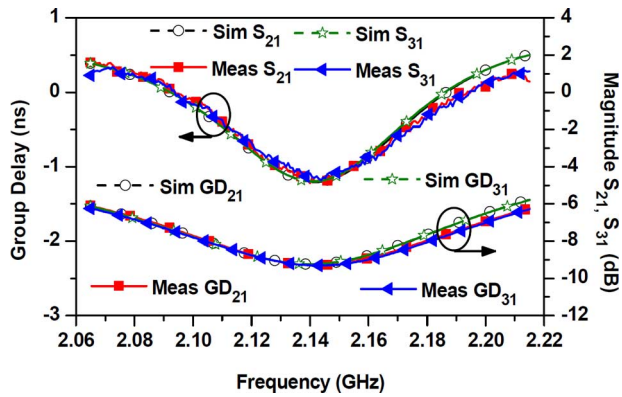

Fig. 5. Simulated and measured S-parameter and group delay characteristics.

TABLE I
PHYSICAL DIMENSIONS OF FABRICATED CIRCUIT (UNITS: MILIMETERS). REFER TO FIG. 4(A).

W_0	L_0	W_1	L_1	g_1	W_2	L_2	g_2	L_3	L_4	L_5
2.4	24	0.94	27.4	1.8	0.8	26.3	0.76	5	14.1	4

negative GD induces more insertion loss delivering a trade-off to the designer [10]. Similarly, the relation between R and Z_1 is illustrated in Fig. 3(d) for different GDs.

The circuit parameters of the proposed power divider for the specified GD can be found by using parametric analysis. Therefore, the design steps of the proposed circuit are summarized as follows.

(a) First, specify f_0, maximum required GD ($\tau_{\rm req}$), characteristic impedance Z_c, and C_{eff} of the short- circuited coupled lines.
(b) Calculate Z_1, R_1, R_2, and R_{iso} using (2) assuming the value of R.
(c) After obtaining Z_1 for the assumed R, calculate GD ($\tau_{\rm cal}$) at f_0 using (3b).
(d) Compare $\tau_{\rm cal}$ with $\tau_{\rm req}$.
(e) If $|\tau_{\rm cal} - \tau_{\rm req}| \le 0.001$, R is a proper value for the specified $\tau_{\rm req}$. If this condition is not satisfied, then change R and repeat steps (b) to (d).
(f) After obtaining the final values of R, Z_1, Z_c, and C_{eff}, calculate Z_{0e} and Z_{0o} of the short-circuited coupled lines using (4).
(g) Finally, obtain the width, length, and spacing of the coupled lines according to substrate information and optimize the physical dimensions using EM-simulator.

III. SIMULATION AND MEASUREMENT RESULTS

For the experimental verification, we designed and fabricated the proposed microstrip line power divider for the specified

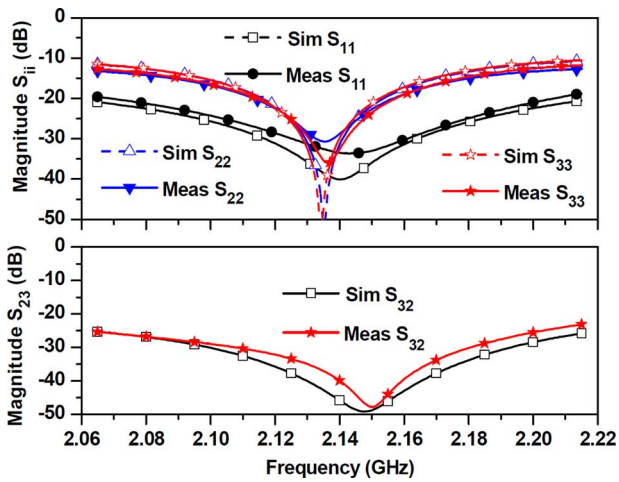

Fig. 6. Simulated and measured return loss and isolation characteristics.

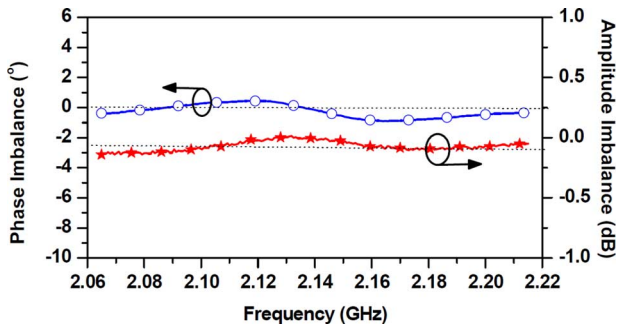

Fig. 7. Measured amplitude and phase imbalance characteristics.

GD of -1.2 ns at f_0 of 2.14 GHz. According to the specified GD, the circuit parameters of the proposed power divider can be obtained using the design procedure described in the previous Section II. Therefore, the calculated circuit parameters are given as $Z_c = 400\ \Omega$, $C_{eff} = -13.57$ dB, $Z_{0e} = 106.1\ \Omega$, $Z_{0o} = 69.33\ \Omega$, $R = 80\ \Omega$, $Z_1 = 90.58\ \Omega$, and $R_{iso} = 266.6\ \Omega$. The circuit is fabricated on a Rogers RT/Duriod 5880 substrate with a dielectric constant (ε_r) of 2.2 and a thickness (h) of 31 mils. The circuit was simulated and optimized using ANSYS HFSS 2014. The EM simulation layout and fabricated circuit are shown in Fig. 4. The physical dimensions of the fabricated power divider are presented in Table I after optimization.

The simulated and measured GDs and magnitudes are shown in Fig. 5. The measured results have small deviations from simulations due to etching tolerances of even- and odd-mode impedances of the coupled lines and R. From the measurement, the insertion losses are $|S_{21}| = 9.29$ dB and $|S_{31}| = 9.30$ dB, while the GDs are $\tau_{21} = -1.16$ ns and $\tau_{31} = -1.17$ ns at $f_0 = 2.143$ GHz. Similarly, the bandwidth (BW) of transmission coefficients, which is defined as 3 dB variation from the center frequency S_{21}, is 150 MHz. Due to the tradeoff between maximum achievable NGD, insertion loss, and BW, the appropriate parameter to compare performances of circuits is a NGD-BW product [10]. Therefore, the NGD-BW products for the different transmission paths are determined as 0.174 and 0.175, respectively. The BW of the NGD power divider may be enlarged by cascading the number of sections [10], [15] with slightly different center frequencies [11], [13]. The measured return losses are $|S_{11}| = 30.38$ dB, $|S_{22}| = 26.76$, and $|S_{33}| = 28.99$ dB at f_0 as shown in Fig. 6. The measured isolation ($|S_{23}|$) at f_0 is -42.18 dB and the 15 dB return loss bandwidth is about 150 MHz.

The measured amplitude imbalance and phase differences between the two output ports are shown in Fig. 7. It can be seen that the maximum amplitude imbalance of ± 0.1 dB and the phase imbalance of $\pm 1^\circ$ are observed over the 15 dB return loss bandwidth.

IV. Conclusion

A power divider with negative group delay characteristics is proposed, investigated, and fabricated in this letter. The simulated and measured results show its merits of negative group delay, good return, and high isolation. This circuit can be employed as a feeding network of antenna arrays for performance improvement by compensating group delay and minimizing beam-squint. In addition, the proposed power divider is promising for application in dynamic power supply or envelope tracking power amplifier to minimize the time-mismatch between the envelope and the RF signal paths.

References

[1] H. R. Ahn and I. Wolff, "General design equations, small-sized impedance transformer, and their application to small-sized three-port 3 dB power dividers," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 7, pp. 1277–1288, Jul. 2001.

[2] H. R. Ahn and S. Nam, "3 dB power dividers with equal complex termination impedances and design methods for controlling isolation circuits," *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 11, pp. 3872–3883, Nov. 2013.

[3] B. Li, X. Wu, and W. Wu, "A 10:1 unequal wilkinson power divider using coupled lines with two shorts," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 12, pp. 789–791, Dec. 2009.

[4] H. R. Ahn and S. Nam, "Wideband microstrip coupled-line ring hybrids for high power-division ratios," *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 5, pp. 1768–1780, May 2013.

[5] Y. Wu, Y. Liu, and Q. Xue, "An analytical approach for a novel coupled-line dual-band wilkinson power divider," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 2, pp. 286–294, Feb. 2011.

[6] C. Miao, J. Yang, G. Tian, X. Zheng, and W. Wu, "Novel sub-miniaturized wilkinson power divider based on small phase delay," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 10, pp. 662–664, Oct. 2014.

[7] M. J. Chik and K. K. M. Cheng, "Group delay investigation of rat-race coupler design with tunable power dividing ratio," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 5, pp. 324–326, May 2014.

[8] S. Lucyszyn, I. D. Robertson, and A. H. Aghvami, "Negative group delay synthesizer," *IET Electron. Lett.*, vol. 29, no. 9, pp. 798–800, Apr. 1993.

[9] M. Kandic and G. E. Bridges, "Bilateral gain-compensated negative group delay circuit," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 6, pp. 308–310, Jun. 2011.

[10] M. Kandic and G. E. Bridges, "Asymptotic limits of negative group delay in active resonator based distributed circuits," *IEEE Trans. Circuits Syst.-I*, vol. 58, no. 8, pp. 1727–1735, Aug. 2011.

[11] G. Chaudhary and Y. Jeong, "Low signal attenuation negative group delay network topologies using coupled lines," *IEEE Microw. Theory Tech.*, vol. 62, no. 10, pp. 2316–2324, Oct. 2014.

[12] C. T. M. Wu and T. Itoh, "Maximally flat negative group delay circuit: a microwave transmission line approach," *IEEE Trans. Microw. Theory Tech.*, vol. 62, no. 6, pp. 1330–1342, Jun. 2014.

[13] H. Choi, Y. Jeong, C. D. Kim, and J. S. Kenney, "Efficiency enhancement of feedforward amplifiers by employing a negative group delay circuit," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 5, pp. 1116–1125, May 2010.

[14] B. Kim, J. Moon, and I. Kim, "Efficiently amplified," *IEEE Microw. Mag.*, vol. 11, no. 5, pp. 87–100, Aug. 2010.

[15] H. R. Ahn, *Asymmetric Passive Components in Microwave Integrated Circuits*. New York: Wiley, 2006.