Synthesis of Reflection-Type Coupled Line All-Pass Circuit With Arbitrary Prescribed Wideband Flat Group Delay

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***Abstract*—In this letter, the analytical design method of a reflection-type coupled line all-pass circuit with arbitrary predefined wideband flat group delay (GD) is presented. The proposed circuit consists of 90° hybrid and coupled lines with a short-circuited load. The proposed structure is simple and does not require any iterative process to obtain optimum circuit parameters. Theoretical and experimental results are provided for validation of the proposed structure. The prototype circuits were fabricated at a center frequency of 2.5 GHz with 2 and 4 ns flat GD responses. The measurement results agreed well with the simulation and theoretical predicted results.**

***Index Terms*—Cancelation circuit, coupled line, real-time analog signal processing, wideband flat group delay (GD) response.**

I. Introduction

MICROWAVE circuits that control group delay (GD) dispersion have a wide range of applications including signal cancellation in feed-forward amplifier [1], self-interference cancellation in-band full duplex [2], and real-time radio analog signal processing (R-ASP) such as spectrum sniffing, real-time Fourier transformer, pulse compression, and chirp waveform generation [3].

Various types of GD circuits including transmission type and reflection type have been presented [4]–[10]. In [4]–[6], lumped element *LC* resonators were used to design circuit with the prescribed GD response. Similarly, the synthesis of a reflection-type circuit and transmission-type coupled line section all-pass circuit with an arbitrary prescribed GD was presented in [7] and [8]. However, these works are limited to narrowband GD. Some efforts have been made to design wideband GD circuits [9], [10]. In [10], shunt- and step-impedance lines were used to overcome the narrowband GD response of conventional structures. Similarly, microwave circuits with the monotonous GD response were described in [11] by cascading all-pass circuits. However, these works require an iterative procedure to obtain optimum circuit parameters, and they may suffer from implementation limitations due to unrealizable circuit parameters.

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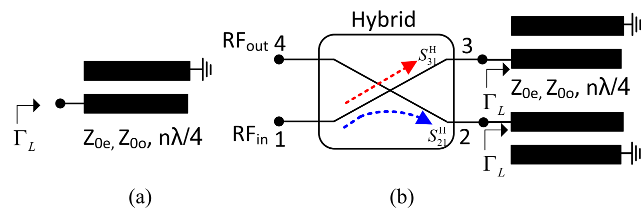

Fig. 1. Proposed structure of reflection-type all-pass circuit with wideband GD response. (a) One-port circuit. (b) Two-port circuit using 90° hybrid.

This letter introduces a reflection-type circuit with an arbitrary prescribed wideband flat GD response based on a coupled line resonator to overcome the narrowband weakness of previously reported circuits. In addition, the circuit parameters of the proposed structure can be found analytically and do not require an iterative method.

II. Design Equations

Fig. 1(a) shows the proposed structure of a reflection-type GD circuit which consists of a coupled line with short-circuited termination. The even- and odd-mode impedances of the coupled line are denoted by Z_{0e} and Z_{0o}, respectively. The reflection coefficient of circuit shown in Fig. 1(a) can be found as (1)

$$\Gamma_L = 1\angle \pi + 2\tan^{-1}\left\{\frac{1}{2Z_p Z_0}\left(Z_p^2 \cot\frac{n\pi f}{2f_0} - 2Z_m^2 \csc\frac{n\pi f}{f_0}\right)\right\} \quad (1)$$

where

$$Z_p = Z_{0e} + Z_{0o}, \quad Z_m = Z_{0e} - Z_{0o}, \quad n = 1, 3, 5, \ldots \quad (2)$$

Here, Z_0, f, and f_0 are the reference port impedance, and the operating and the design center frequency, respectively. Similarly, the length of the coupled line is $n\lambda/4$ at f_0, where n is an odd number. From (1), the GD of reflective circuit shown in Fig. 1(a) can be found as

$$\tau_L^{\mathrm{cl}} = \frac{nZ_p Z_0}{f_0}\,\frac{\left(Z_p^2 \csc^2\frac{n\pi f}{2f_0}\sin^2\frac{n\pi f}{f_0} - 4Z_m^2\cos\frac{n\pi f}{f_0}\right)}{Z_p^2 Z_0^2 \sin^2\frac{n\pi f}{f_0} + \left(Z_p^2\cot\frac{n\pi f}{2f_0}\sin\frac{n\pi f}{f_0} - 2Z_m^2\right)^2}. \quad (3)$$

As seen from (2) and (3), the GD depends on Z_{0e} and Z_{0o} of the coupled lines. Therefore, an arbitrary specified flat GD response can be obtained by selecting appropriate Z_{0e} and Z_{0o}. It is difficult to find the exact solutions of Z_{0e} and Z_{0o} from (3) such that the GD is a wideband flat GD response. Therefore, the numerical simulation was used to find the values

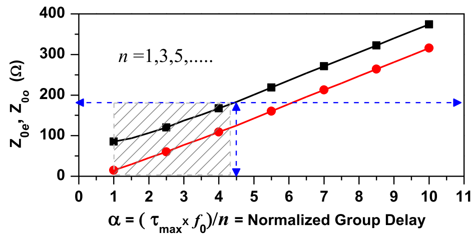

Fig. 2. Synthesized Z_{0e} and Z_{0o} for arbitrary specified normalized GD. The polynomial coefficients: $a_0 = 63.1708$, $a_1 = 17.5560$, $a_2 = 2.6414$, $a_3 = -0.1298$, $b_0 = -13.1656$, $b_1 = 26.9725$, $b_2 = 1.1067$, and $b_3 = -0.0520$.

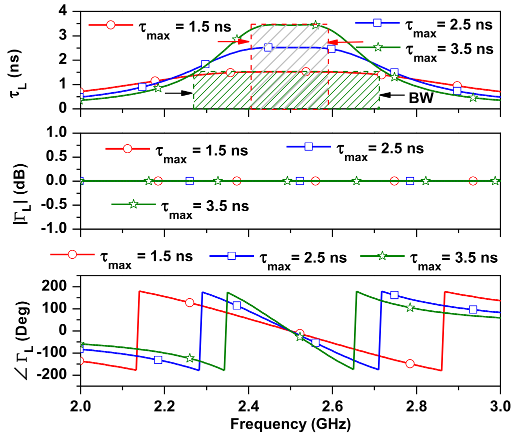

Fig. 3. Calculated responses of the proposed reflection-type all-pass circuit.

TABLE I

CALCULATED CIRCUIT PARAMETERS WITH SPECIFIED GDs

f_0 (GHz)	τ_{max} (ns)	n =1		n =3	
		Z_{0e} (Ω)	Z_{0o} (Ω)	Z_{0e} (Ω)	Z_{0o} (Ω)
2.50	1.50	159.3056	100.8021	88.9895	22.1777
2.50	2.50	244.3860	185.9477	110.0365	47.3603
2.50	3.50	332.0621	272.7396	133.6255	73.6286

of Z_{0e} and Z_{0o} so that the GD response is flat over a wideband frequency. The extracted Z_{0e} and Z_{0o} are shown in Fig. 2. Based on the extracted values, the solutions of Z_{0e} and Z_{0o} as a function of normalized GD ($\alpha = \tau_{max} \times f_0/n$) can be found by using the curve fitting method as

$$Z_{0e} = a_0 + a_1\alpha + a_2\alpha^2 + a_3\alpha^2$$
$$Z_{0o} = b_0 + b_1\alpha + b_2\alpha^2 + b_3\alpha^2. \quad (4)$$

The values of Z_{0e} and Z_{0o} become very high when α is larger than 5. The values of Z_{0e} and Z_{0o} can be easily realized by decreasing α with higher n for the same GD, however, the circuit size increases.

Based on analysis, described above, the calculated magnitude and GD response of the proposed structure are shown in Fig. 3. The calculated circuit parameters are given in Table I. As shown in Fig. 3, the GD bandwidth (BW), which is defined as the BW of flat τ_{max} (refer to Fig. 3), decreases as τ_{max} increases. However, the magnitudes remain the same for every specified GD. Similarly, to show the variation of the flat GD fractional BW (FBW = BW/f_0 × 100%) with increasing τ_{max}, the graph is plotted and shown in Fig. 4. Fig. 4 shows that FBW decreases when $\tau_{max} \times f_0$ increases. Therefore, a tradeoff exists between τ_{max} and FBW.

The reflection termination units can be combined to form two-port network by using hybrid coupler, as shown in Fig. 1(b). Assume, the coupled and through responses of the hybrid coupler in Fig. 1(b) are S_{21}^H and S_{31}^H, respectively. The S-parameters of two-port network combining two reflection termination units by the hybrid are expressed as [4]

$$S_{11} = \left[\left(S_{21}^H\right)^2 + \left(S_{31}^H\right)^2\right]\Gamma_L = R^H\Gamma_L$$
$$S_{21} = 2S_{21}^H S_{31}^H \Gamma_L = T^H\Gamma_L. \quad (5)$$

The combined two-port GD circuit would exhibit perfect matching ($S_{11} = 0$) and transmission ($S_{21} = 1$), respectively, only if the hybrid coupler exhibits the S-parameters such that $|R^H| = |(S_{21}^H)^2 + (S_{31}^H)^2| = 0$ and $|T^H| = |2S_{21}^H S_{31}^H| = 1$. However, these requirements are practically limited in BW, any hybrid coupler implementation will affect magnitude and GD responses of overall combined two-port circuit. Therefore, designer should choose wideband hybrid coupler with flat transmission magnitude and high return loss (more than 20-dB return loss) over wide operating band. The effect of hybrid on GD response of combined two-port network may be quantified by adding GD of hybrid to GD of coupled line reflection terminations. Since the GD introduced by hybrid can be considered constant overall BW of combined two-port GD circuit, the overall GD of combined circuit is expressed as

$$\tau_{21} = \tau_L^{cl} + \tau^H = \tau_L^{cl} + \text{const.} \quad (6)$$

where $\tau_L^{cl}$is given in (3) and τ^H is GD of hybrid. Equation (6) quantifies that the hybrid is essentially transparent to reflective coupled line termination GD circuit at its coupled and through ports.

The design steps to find the optimum circuit parameters of the proposed circuit with arbitrary specified wideband flat GD response can be summarized as follows.

1) Specify f_0 and maximum GD (τ_{max}) at f_0 and n.
2) Calculate normalized GD $\alpha = \tau_{max} \times f_0/n$.
3) Obtain values of Z_{0e} and Z_{0o} using (4) corresponding to α.
4) Obtain width, length, and spacing of coupled line corresponding to Z_{0e} and Z_{0o} and substrate information.
5) Convert one-port termination network into two-port network by using hybrid coupler. Finally, optimize the physical dimensions of combined circuit by using simulator.

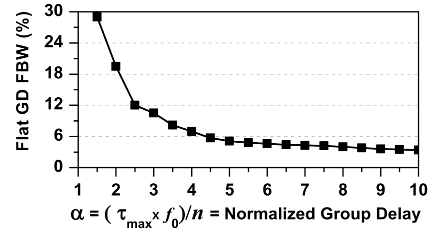

Fig. 4. Variation of flat GD FBW as a function of normalized GD.

III. IMPLEMENTATION AND EXPERIMENTAL PERFORMANCES

For experimental demonstration, a prototype was fabricated at f_0 of 2.50 GHz on an RT/Duroid 5880 substrate with a dielectric constant (ε_r) of 2.2 and thickness (h) of 0.787 mm. The physical dimensions of the fabricated circuits were optimized using ANSYS HFSS 15. The goal of the designed circuits were to achieve a GD of 2 and 4 ns under the assumption

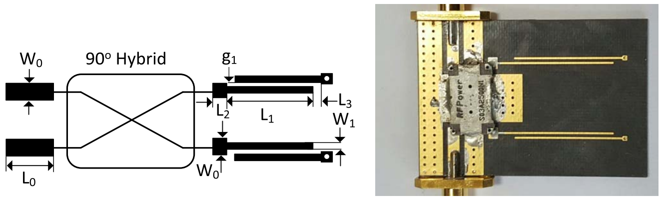

Fig. 5. (a) Layout of designed circuit and (b) photograph of fabricated prototype I. Physical dimensions: $W_0 = 2.4$, $L_0 = 10$, $W_1 = 0.25$, $L_1 = 23.42$, $L_2 = 2$, $L_3 = 1.72$, and $g_1 = 0.72$ (Units: millimeters).

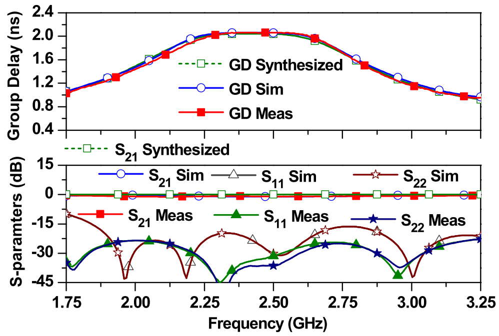

Fig. 6. Simulation and measured results of the fabricated prototype I with $n = 1$.

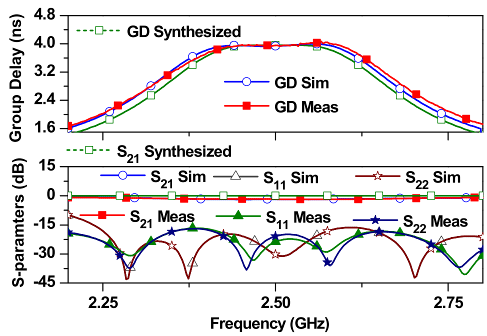

Fig. 7. Simulation and measured results of fabricated prototype II with $n = 3$.

of a termination port impedance Z_0 of 50 Ω and 0.4 ns GD of a 90° hybrid coupler and associated input–output feed lines.

As described in Section II, the calculated circuit parameters for the GD of 2 ns at $f_0 = 2.5$ GHz and $n = 1$ are given as $Z_{0e} = 167.350$ Ω and $Z_{0o} = 109.1036$ Ω, respectively. A quadrature surface mount 90° hybrid S03A2500N1 from ANAREN was used in this work. The layout and physical dimensions of the designed circuit are shown in Fig. 5(a). A photograph of the fabricated circuit is shown in Fig. 5(b).

Fig. 6 shows simulation and measured results of the fabricated prototype I. From the measurement, the maximum achievable GD is 2.02 ns which extends from 2.36 to 2.62 GHz. Therefore, the BW of flat GD is 260 MHz. Similarly, the measured $|S_{21}|$, $|S_{11}|$, and $|S_{22}|$ at f_0 are determined as −1.15, −28.5, and −29.5 dB, respectively.

To demonstrate the prototype for higher GD, the circuit was designed for GD of 4 ns at $f_0 = 2.5$ GHz and $n = 3$, and calculated parameters are given as $Z_{0e} = 136.1038$ Ω and $Z_{0o} = 76.3082$ Ω assuming 0.4 ns GD of hybrid. Fig. 7 shows the measured and simulation results of prototype II. The measured GD is 4.02 ns which extends from 2.40 to 2.62 GHz. Similarly, the measured $|S_{21}|$, $|S_{11}|$, and $|S_{22}|$ at f_0 are determined as −1.69, −23.8, and −20.93 dB, respectively.

TABLE II

PERFORMANCE COMPARISON

	f_0 (GHz)	S_{21max} (dB)	τ_{max} (ns)	FBW (%)	Method	Technology
[4]	1.0	<-30	10.0	2	Analytical	MMIC
[5]	0.911	<-2.68	3.93	0.60	Analtytical	Microstrip
[6]	2.14	<-5.9	4.0	2.803	Analytical	Microstrip
[9]	2.10	<-6.5	6.0	9.52	Iterative	Microstrip
[10]	0.50	<-1.5	2.30	40*	Iterative	Microstrip
This work	**2.50/2.50**	**<-1.15/-1.69**	**2.0/4.0**	**10.4/8.4**	**Analytical**	**Microstrip**

FBW = Fractional bandwidth of flat group delay, * = Ideal 1-port simulated result

The performances of the proposed circuit are compared with a state-of-the-arts circuit and are shown in Table II. As seen from Table II, the proposed work provides wide flat GD BW and does not require any complicated iterative method to obtain the optimum circuit parameters.

IV. CONCLUSION

In this paper, we demonstrate the design of a reflection-type all-pass circuit with arbitrary specified wideband flat GD response. Analytical design equations are provided to calculate the optimum circuit parameters for specified GD and design center frequency. Therefore, the proposed circuit does not require an iterative method. For experimental validation, the prototypes were fabricated at a center frequency of 2.50 GHz.

From the experimental results, it is confirmed that the proposed structure provides a flat wideband GD response and is applicable to various RF/microwave circuits and systems such as wideband self-interference cancellation in-band full duplex and R-ASP.

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