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Reflection-Type Topologies With Arbitrary Wideband Flat Group Delays Using Coupled Lines

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ABSTRACT This paper presents the analytical design techniques of several reflection-type group delay (GD) circuits (types-I–III) with arbitrarily prescribed wideband flat GD responses using λ/4-coupled lines. The type-I GD circuit consists of the λ/4 transmission lines and an open-circuited coupled line with a short-circuited load, whereas type-II consists of a short-circuited coupled line with an open-circuited load. For a compact circuit size, the type-III circuit is realized by a parallel combination of the open-circuited and short-circuited coupled lines. To obtain the arbitrarily prescribed response of wideband flat GD, closed-form analytical design equations are provided. An analytical analysis shows that the wideband flat GD response can be obtained by controlling the appropriate even- and odd-mode impedances of the coupled lines. For an experimental validation of the proposed structures, prototypes of the three GD circuits were designed and fabricated at the center frequency of 2.5 GHz. To realize a higher GD response over a wideband bandwidth, a number of reflection-type GD circuit units are cascaded and measured. The measurement results agree soundly with the simulation and theoretical prediction results.

INDEX TERMS Analog radio signal processing, arbitrary wideband flat group delay response, coupled lines, reflection-types, signal cancellation.

I. INTRODUCTION

Microwave group delay (GD) circuits have various applications in modern wireless communication systems including the AM/PM cancellation of predistortion linearizer [1], the radio frequency (RF) self-interference cancellation of the in-band full duplex radio [2], the signal cancellation in feed-forward amplifier [3], and real-time analog radio-signal processing (R-ASP) [4]–[6]. To enhance the cancellation bandwidth in RF communication systems, wideband GD circuits are highly essential components for the matching of the GD between the referential and cancellation paths.

The realization of GD circuits requires an efficient control of the phase characteristics, and these circuits can be classified into reflection- and transmission-types. The transmission-type GD circuit was realized using a multi-section coupler-based super-conductive delay [7], a cascading of all pass networks [8], [9], and the non-commensurate coupled lines using the multi-conductor transmission line (TL) technique [10]. These structures, however, require genetic-optimization techniques to implement the final structures. Similarly, wideband all-pass GD circuits have been synthesized through the usage of and non-uniform commensurate C- and D-sections [11], [12], and a multilayer broadside coupled line GD circuit for analog signal processing [13]. These works, however, require iterative design procedures to map the arbitrary prescribed GD problem from the bandpass to the low pass domain, and then again back to the bandpass domain for the attainment of the optimum circuit parameters. Similarly, a transversal filter structure for which a distributed amplifier has been utilized to realize GD circuit [14] that requires complex iterative procedures to obtain a large number of tap coefficients for the specified GD response.

In contrast to the transmission-type, reflection-type GD circuits are widely used and can be realized by terminating the coupled and through ports of a 3-dB hybrid coupler with a one-port reflective GD circuit, and the overall GD response of the resultant two-port network is addition of the GD responses of the hybrid and one-port reflective circuits [15]–[17]. One-port reflective GD circuits typically include chirped dispersive delay lines at microwave frequencies, and these circuits are realized using spatial impedance profiles, however, this approach is limited to specific implementation types [18]. Similarly, a coupled-resonator network approach

was utilized to design the GD equalizers using optimization procedures [19], [20]. A narrow-band one-port circuit with an arbitrarily prescribed GD response was synthesized in [21]; later, this technique was improved and applied to a design of reflective GD circuits that is based on shunt stubs, stepped-impedance lines [22], alternating K/J-inverters, and $\lambda/4$ TL resonators [23], [24]. However, iterative procedures are required for these techniques to transform the prescribed GD problem from the bandpass domain to the low-pass domain using a one-port ladder network, and again, to transform the synthesized low-pass network back to the bandpass domain, for the implementation in a specific technology.

This paper presents the realization of reflection-type GD circuits with an arbitrarily prescribed wideband flat GD response based on an exact analytical synthesis technique. The proposed circuits are based on the synthesis of one-port coupled lines, which do not require any transformative procedures for the attainment of the circuit parameters for the specified flat GD response. Three reflection-type GD circuits are proposed, synthesized and experimentally demonstrated. To realize a high GD response with the wideband bandwidth, a number of reflection-type GD circuits can be cascaded.

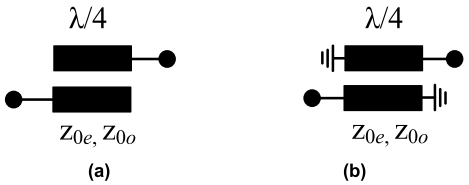

FIGURE 1. Two-port coupled line circuits: (a) the coupled and through ports are open-circuited and (b) the coupled and through ports are short-circuited.

II. MATHEMATICAL ANALYSIS

Fig. 1 shows the structures of the $\lambda/4$ coupled line [25], where z_{0e} and z_{0o} denote the normalized even- and odd-mode impedances with respect to the port impedance Z_0 of coupled line, respectively. Assuming $z_c = \sqrt{z_{0e}z_{0o}}$, the normalized z_{0e} and z_{0o} of the coupled line can be using (1) as follows:

$$z_{0e} = z_c\sqrt{\frac{1+C}{1-C}}, \tag{1a}$$

$$z_{0o} = z_c\sqrt{\frac{1-C}{1+C}}, \tag{1b}$$

$$C = \frac{z_{0e}-z_{0o}}{z_{0e}+z_{0o}}, \tag{1c}$$

where C is the coupling coefficient of the coupled line [25]. The normalized z-parameters of the coupled line with open-circuited coupled and the through ports, shown in Fig. 1(a), can be expressed as (2) in terms of the z_c and C as follows:

$$[z] = \begin{bmatrix} -j\dfrac{z_c}{\sqrt{1-C^2}}\cot\dfrac{\pi f}{2f_0} & -j\dfrac{z_cC}{\sqrt{1-C^2}}\csc\dfrac{\pi f}{2f_0} \\ -j\dfrac{z_cC}{\sqrt{1-C^2}}\csc\dfrac{\pi f}{2f_0} & -j\dfrac{z_c}{\sqrt{1-C^2}}\cot\dfrac{\pi f}{2f_0} \end{bmatrix} \tag{2}$$

where, f and f_0 are the operating and design center frequencies, respectively. Similarly, the normalized y-parameters the coupled line, where the coupled and through ports are short-circuited, and are shown in Fig. 1(b), can be expressed as (3) in terms of the z_c and C as follows:

$$[y] = \begin{bmatrix} -j\dfrac{1}{z_c\sqrt{1-C^2}}\cot\dfrac{\pi f}{2f_0} & -j\dfrac{C}{z_c\sqrt{1-C^2}}\csc\dfrac{\pi f}{2f_0} \\ -j\dfrac{C}{z_c\sqrt{1-C^2}}\csc\dfrac{\pi f}{2f_0} & -j\dfrac{1}{z_c\sqrt{1-C^2}}\cot\dfrac{\pi f}{2f_0} \end{bmatrix}. \tag{3}$$

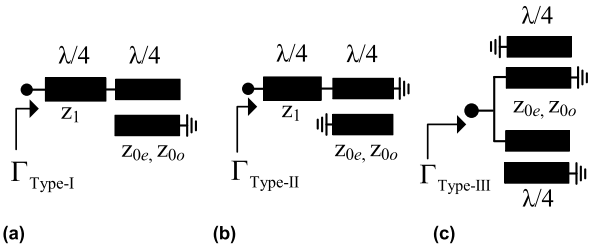

FIGURE 2. Proposed one-port reflective wideband group delay circuits: (a) type-I, (b) type-II, and (c) type-III.

A. WIDEBAND FLAT GROUP DELAY (GD) CIRCUIT: ONE-PORT REFLECTIVE TYPE-I

Fig. 2(a) shows the proposed structure of the reflective type-I wideband GD circuit that consists of the $\lambda/4$ coupled line and a TL with the normalized characteristic impedance of z_1. The reflection coefficient of this circuit is expressed as (4), as follows:

$$\Gamma^c_{\text{Type-I}} = \frac{x_2 - jx_1}{x_2 + jx_1} = 1\angle 2\tan^{-1}\left(\frac{x_2}{x_1}\right), \tag{4}$$

where

$$x_1 = \left(2z_1 + \frac{2z_c}{\sqrt{1-C^2}}\right)\cos^2\frac{\pi f}{2f_0} - \frac{2z_cC^2}{\sqrt{1-C^2}} \tag{5a}$$

$$x_2 = \frac{2z_cz_1}{\sqrt{1-C^2}}\left(\cos^2\frac{\pi f}{2f_0} - C^2\right)\cot\frac{\pi f}{2f_0} - z_1^2\sin\frac{\pi f}{f_0} \tag{5b}$$

Using the reflection-coefficient phase, the GD of the one-port reflective type-I circuit is calculated using (6).

$$\tau_{\text{Type-I}} = -\frac{1}{2\pi}\frac{d\angle\Gamma^c_{\text{Type-I}}}{df} = \frac{1}{\pi}\frac{x_1'x_2 - x_1x_2'}{x_1^2 + x_2^2}, \tag{6}$$

where

$$x_1' = -\frac{\pi}{f_0}\left(z_1 + \frac{z_c}{\sqrt{1-C^2}}\right)\sin\frac{\pi f}{f_0}, \tag{7a}$$

$$x_2' = -\frac{\pi}{f_0}\left\{\frac{z_cz_1}{\sqrt{1-C^2}}\left(\begin{matrix}2\cos^2\dfrac{\pi f}{2f_0} + \cot^2\dfrac{\pi f}{2f_0} \\ -C^2\csc^2\dfrac{\pi f}{2f_0}\end{matrix}\right) + z_1^2\cos\frac{\pi f}{f_0}\right\}. \tag{7b}$$

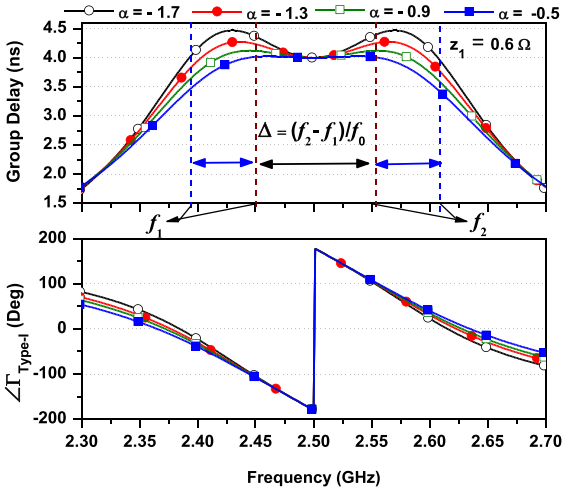

FIGURE 3. Calculated response of the reflective type -I wideband flat group delay circuit with $\tau = 4$ ns at $f_0 = 2.5$ GHz and different α.

From (6), it is evident that the wideband flat GD can be obtained if the appropriate z_c and C are chosen. For this purpose, the GD at $f = f_0$ can be further simplified as (8) using (6).

$$\tau_{f=f_0}^{\text{Type-I}} = \frac{z_c z_1 C^2 + z_1^2\sqrt{1-C^2}}{2f_0 z_c C^2} \tag{8}$$

From (8), it is noted that the GD at $f = f_0$ depends on the z_1, C, and z_c. Therefore, the z_c value can be expressed in terms of the GD and C using (9).

$$z_c = \frac{z_1^2\sqrt{1-C^2}}{C^2\left(2f_0\tau_{f=f_0}^{\text{Type-I}} - z_1\right)}. \tag{9}$$

where z_1 can be chosen arbitrarily. In addition, it is evident from (9) that, the value of z_c is only real positive if $z_1 < 2f_0\tau_{f=f_0}^{\text{Type-I}}$.

To obtain real positive z_c from (9), the relations among C, the specified GD and f_0 should become evident. The expression of C that relates to GD and f_0 can be empirically written using (10).

$$C\,(dB) = -20\log\left(f_0\tau_{f=f_0}^{\text{Type-I}}\right) + \alpha, \tag{10}$$

where α is a factor that provides an extra degree of freedom to control the C, which resulting in a variation of the GD ripple. The in-band GD ripples ($\Delta\tau_{ripple}$) is defined using (11).

$$\Delta\tau_{rippple} = \frac{\tau_{\max} - \tau_{f=f_0}}{\tau_{avg}} = \frac{\tau_{\max} - \tau_{f=f_0}}{0.5\left(\tau_{\max} + \tau_{f=f_0}\right)}, \tag{11}$$

where $\tau_{\max}$ is the maximum GD at passband edge frequency.

To validate the analytical-design equations, Fig. 3 shows the calculated GD and the phase response of reflective type-I GD circuit with different α. The design specification and the calculated circuit parameters are shown in Table 1. In these calculations, the GD at f_0 is fixed at 4 ns. As can be seen from Fig. 3, the $\Delta\tau_{ripple}$ decreased as α was increased.

TABLE 1. Calculated parameters of the reflective type-I group delay circuit with $z_1 = 0.6\ \Omega$ and different α values.

Group delay specification : $\tau_{f=f_0}^{\text{Type-I}} = 4$ ns and $f_0 = 2.5$ GHz				
α	-1.7	-1.3	-0.9	-0.5
$\Delta\tau_{ripple}$ (%)	11.08	6.5936	2.9935	0.6237
Δ (%)	8.6	7.80	6.60	4.80
C (dB)	21.70	-21.30	-20.90	-20.5
z_c (Ω)	2.7354	2.4939	2.2737	2.0728
z_{0e} (Ω)	2.9404	2.7188	2.4888	2.2787
z_{0o} (Ω)	2.5191	2.2877	2.2787	1.8855

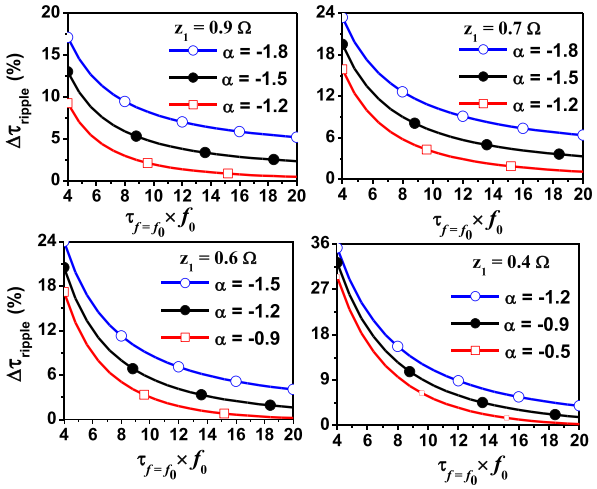

FIGURE 4. Calculated in-band group delay of type-I circuit with different α and z_1.

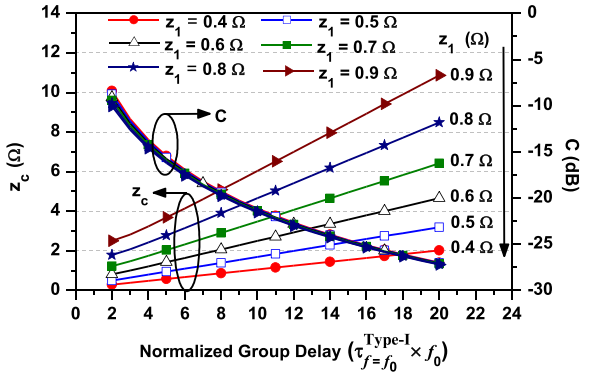

FIGURE 5. Calculated z_c and C for the flat wideband group delay characteristics of the reflective type-I with $\alpha = -0.8$.

In addition, the flat GD bandwidth which is defined as the bandwidth when GD is flat within acceptable $\Delta\tau_{ripple}$, was decreased when the GD response approaches toward the flat.

To investigate the effect of the α selection, Fig. 4 shows the calculated $\Delta\tau_{ripple}$. As observed from this figure, the $\Delta\tau_{ripple}$ was decreased as the α was increased. In general, a high α is preferable for the minimum $\Delta\tau_{ripple}$.

Similarly, to investigate the effect of the selection of the z_1, Fig. 5 shows the design graph for the provision of the

relationship between the z_c, C and z_1 for the arbitrary GD and f_0. In these calculations, the normalized GD ($\tau_{f=f_0} \times f_0$) was chosen so that the designer can obtain the circuit parameters for any arbitrary specifications. From this graph, the z_c was increased and C was decreased as the GD was increased. It is also clear from this graph that the practically realizable circuit parameters of the coupled lines can be obtained by appropriately selecting the z_1. When the GD approaches a high value, the designer should select a low z_1. Specifically, a low z_1 is preferable for a high GD and practically realizable coupled lines.

To calculate the GD bandwidth with the minimum $\Delta\tau_{ripple}$, the cut-off frequencies where the GD is approximately equal to the GD at f_0 should be found, as shown in Fig. 3. The GD fractional bandwidth (Δ) can be mathematically calculated as (12).

$$\Delta = \frac{f_2 - f_1}{f_0} = f\left(z_1, z_c, C, \tau_{f_0}, f_0\right), \tag{12}$$

where f_1, and f_2 are lower, and upper cut-off frequencies in between which the GD is within the desired GD at f_0 as shown in Fig. 4. Since it is complicated to find f_1 and f_2 by analytically using (6), a numerical method was used in MATLAB to find the Δ for mathematical simplicity. Based on the MATLAB numerical analysis, Fig. 6 shows the calculated Δ for different z_1 and α values. As GD was increased, the Δ was decreased. In addition, the Δ was slightly higher when the α is small, however, a small α increases the $\Delta\tau_{ripple}$.

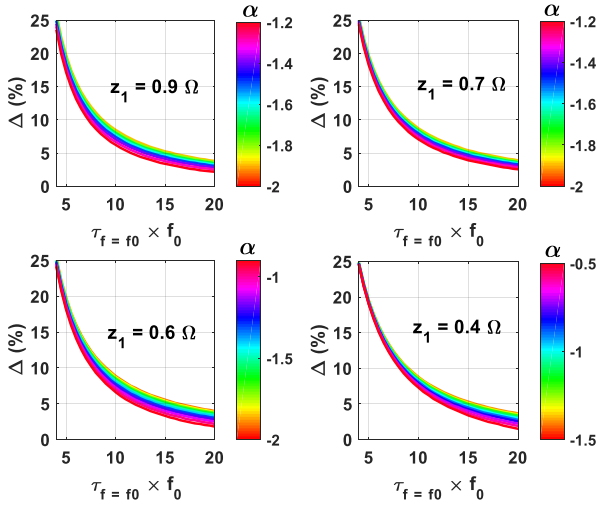

FIGURE 6. Calculated group delay fractional bandwidth of the type-I circuit for different z_1 and α values. Color bar represents the α.

B. WIDEBAND FLAT GROUP DELAY CIRCUIT: ONE-PORT REFLECTIVE TYPE-II

In terms of complementarity of the type-I GD circuit, the short-circuited coupled line GD circuit was studied, and its schematic is depicted in Fig. 2(b). The proposed reflective type-II wideband GD circuit consists of the $\lambda/4$ short-circuited coupled lines and the TL with the normalized characteristic impedance of z_1.

Using the y-parameters of the short-circuited coupled lines that are shown in (3), the reflection coefficient of this circuit is expressed by (13), as follows:

$$\Gamma^{c}_{\text{Type-II}} = \frac{x_3 - jx_4}{x_3 + jx_4} = 1\angle - 2\tan^{-1}\left(\frac{x_4}{x_3}\right), \tag{13}$$

where

$$x_3 = \left(\frac{2}{z_1} + \frac{2}{z_c\sqrt{1-C^2}}\right)\cos^2\frac{\pi f}{2f_0} - \frac{2C^2}{z_c\sqrt{1-C^2}} \tag{14a}$$

$$x_4 = \frac{1}{z_1^2}\sin\frac{\pi f}{f_0} + \frac{2}{z_c z_1\sqrt{1-C^2}}\left(C^2 - \cos^2\frac{\pi f}{2f_0}\right)\cot\frac{\pi f}{2f_0} \tag{14b}$$

Like the type-I circuit, the GD of the reflective type-II circuit that is shown in Fig. 2(b) was calculated using (15), as follows:

$$\tau_{\text{Type-II}} = -\frac{1}{2\pi}\frac{d\angle\Gamma_{\text{Type-II}}}{df} = \frac{1}{\pi}\frac{x_3x_4' - x_3'x_4}{x_3^2 + x_4^2}, \tag{15}$$

where

$$x_3' = -\frac{\pi}{f_0}\left(\frac{1}{z_1} + \frac{1}{z_c\sqrt{1-C^2}}\right)\sin\frac{\pi f}{f_0}, \tag{16a}$$

$$x_4' = -\frac{\pi}{f_0}\left\{\frac{1}{z_1^2}\cos\frac{\pi f}{f_0} - \frac{1}{z_c z_1\sqrt{1-C^2}} \times \left(\begin{matrix} 2\cos^2\frac{\pi f}{2f_0} + \cot^2\frac{\pi f}{2f_0} \\ -C^2\csc^2\frac{\pi f}{2f_0}\end{matrix}\right)\right\}. \tag{16b}$$

It becomes evident from (15) and (16) that, the GD response of the type-II circuit depends on the z_1, z_c and C. Here, the z_1 can be chosen arbitrarily, but the wideband flat GD can be obtained by selecting the appropriate z_c and C. Furthermore, the z_c can be expressed in terms of the GD and the C by applying $f = f_0$ in (15) as shown in the following formula (17):

$$z_c = \frac{\left(2f_0\tau^{\text{Type-II}}_{f=f_0}z_1 - 1\right)z_1C^2}{\sqrt{1-C^2}} \tag{17}$$

An examination of (17) showed that the value of z_c is only real positive if $2f_0\tau^{\text{Type-II}}_{f=f_0}z_1 > 1$. Therefore, the C that can provide the wideband flat GD in the proposed circuit is empirically written using (18), as follows:

$$C\,(dB) = -20\log\left(f_0\tau^{\text{Type-II}}_{f=f_0}\right) + \beta \tag{18}$$

where β is a factor which provides a degree of freedom for the control of the $\Delta\tau_{ripple}$.

Fig. 7 shows the calculated response of the reflective type-II GD circuit based on the analytical design equations. Table 2 shows the calculated circuit parameters with their design specifications wherein the GD at f_0 is fixed at 4 ns. In contrast to the open-circuited coupled line GD circuit, the z_1 should be high in this circuit. Like the type-I circuit,

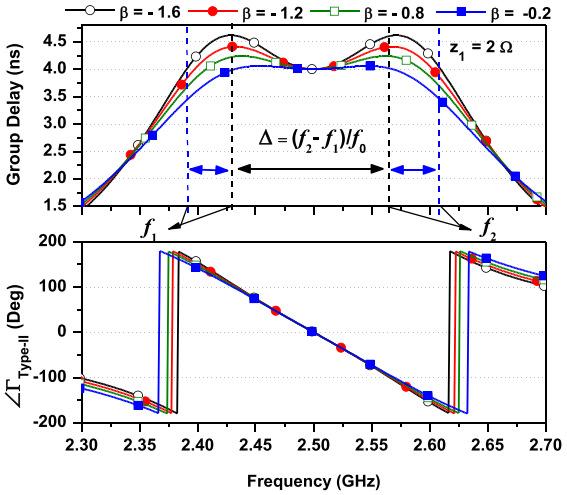

FIGURE 7. Synthesized results of the reflective type-II wideband flat group delay circuit with $\tau = 4$ ns at $f_0 = 2.5$ GHz and different β.

TABLE 2. Calculated parameters of reflective type-II Group Delay Circuit With $z_1 = 0.6\ \Omega$ and different β values.

Specification : $\tau_{f=f_0}^{\text{Type-II}} = 4$ ns and $f_0 = 2.5$ GHz				
β	-1.6	-1.2	-0.80	-0.20
$\Delta\tau_{ripple}$ (%)	14.3883	9.8192	5.8719	1.5222
Δ (%)	8.7	8.20	7.40	5.40
C (dB)	-21.60	-21.20	-20.80	-20.20
z_c (Ω)	0.5415	0.5939	0.6515	0.7485
z_{0e} (Ω)	0.5886	0.6481	0.7139	0.8256
z_{0o} (Ω)	0.4982	0.5443	0.5946	0.6786

the $\Delta\tau_{ripple}$ here is controlled by the varying of the C of the coupled line with aid of β. The flat GD bandwidth was increased with increase of the $\Delta\tau_{ripple}$. In addition, the GD approaches toward flat status through the increasing of β.

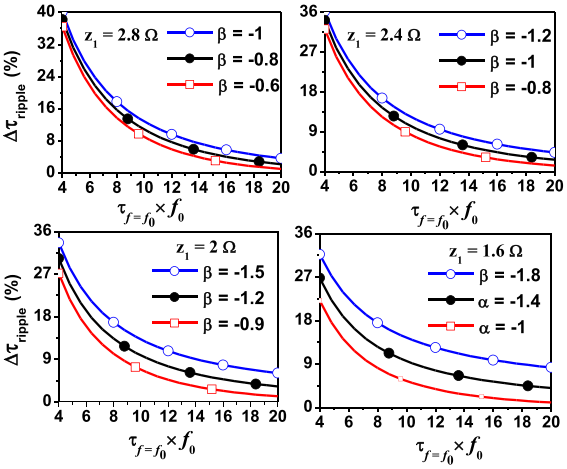

FIGURE 8. Calculated in-band group delay ripple of the reflective type-II circuit with different z_1 and β values.

For the investigation of the effect of β selection, Fig. 8 shows the calculated $\Delta\tau_{ripple}$ of the type-II circuit with different z_1 values. As can be seen from this figure, the

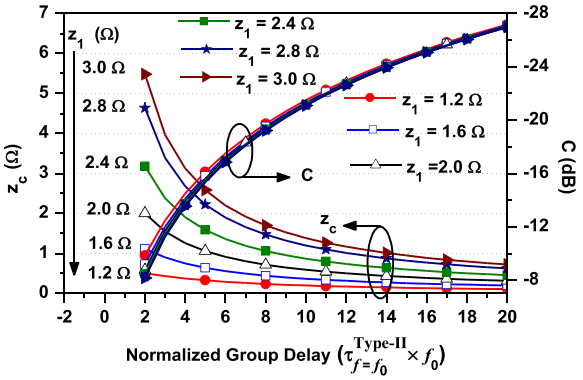

FIGURE 9. Calculated z_c and C for the flat wideband group delay characteristics of the reflective type-II circuit with $\beta = -0.8$.

$\Delta\tau_{ripple}$ can be minimized by increasing the β. In general, a higher β is preferable for obtaining minimum $\Delta\tau_{ripple}$.

To investigate the appropriate selection of z_1, Fig. 9 shows the design graph that depicts the calculated z_c and C for different z_1 values. From this graph, the C notably becomes low for the higher normalized GD, however, a higher z_1 is preferable for a higher GD because of the practically realizable circuit parameters of the coupled lines.

Like the type-I circuit, the Δ of type-II circuit with the minimum $\Delta\tau_{ripple}$ can be determined by finding the lower and upper cut-off frequencies where the GD is approximately equal to the GD at f_0, as shown in Fig. 7. For mathematical simplicity, MATLAB was used to calculate Δ from (15). Fig. 10 shows the calculated Δ for different of z_1 and β values. From these graphs, the Δ was decreased as GD was increased, and the Δ for the small β values is slightly higher.

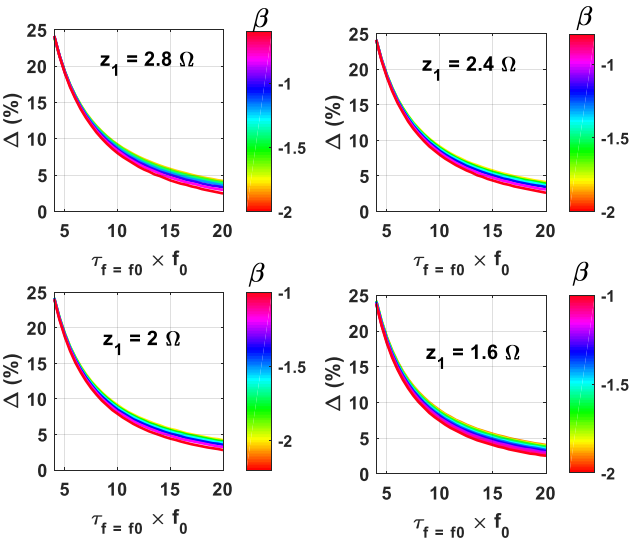

FIGURE 10. Calculated in-band group delay fractional bandwidth of the type-II circuit.

C. WIDEBAND FLAT GROUP DELAY CIRCUIT: ONE-PORT REFLECTIVE TYPE-III

The reflective type-I and type-II circuits consist of the λ/4 TL and coupled line that increase the overall circuit size.

To miniaturize the circuit, another structure is studied and depicted in Fig. 2(c). The proposed reflective type-III structure consists of λ/4 open-circuited and short-circuited coupled lines that are connected in parallel, thereby reducing the circuit size by 50% compared with the type-I and type-II circuits.

By using the normalized z-parameters of the open-circuited coupled lines and the y-parameters of short-circuited coupled lines, the reflection coefficient of this circuit is determined by (19), as follows:

$$\Gamma^{c}_{\text{Type-III}} = \frac{x_6 - jx_5}{x_6 + jx_5} = 1\angle -2\tan^{-1}\frac{x_5}{x_6}, \tag{19}$$

where

$$x_5 = \sin^2\frac{\pi f}{f_0} - \frac{4}{1-C^2}\left(\cos^2\frac{\pi f}{2f_0} - C^2\right)^2, \tag{20a}$$

$$x_6 = \frac{2z_c}{\sqrt{1-C^2}}\left(\cos^2\frac{\pi f}{2f_0} - C^2\right)\sin\frac{\pi f}{f_0}. \tag{20b}$$

Furthermore, the GD of the reflective type-III circuit was calculated using (21), as follows:

$$\tau_{\text{Type-III}} = -\frac{1}{2\pi}\frac{d\angle\Gamma_{\text{Type-III}}}{df} = \frac{1}{\pi}\frac{x_5'x_6 - x_5x_6'}{x_5^2 + x_6^2}, \tag{21}$$

where

$$x_5' = \frac{\pi}{f_0}\left\{\sin\frac{2\pi f}{f_0} + \frac{4}{1-C^2}\sin\frac{\pi f}{f_0}\left(\cos^2\frac{\pi f}{2f_0} - C^2\right)\right\}, \tag{22a}$$

$$x_6' = \frac{\pi}{f_0}\frac{z_c}{\sqrt{1-C^2}}\left(\begin{matrix}2\cos^2\frac{\pi f}{2f_0}\cos\frac{\pi f}{f_0} \\ -2C^2\cos\frac{\pi f}{f_0} - \sin^2\frac{\pi f}{f_0}\end{matrix}\right). \tag{22b}$$

As observed from (21) and (22), the GD response depends on the z_c and C; therefore, the flat wideband GD can be obtained by properly selecting the z_c and C. To determine appropriate z_c and C for a flat GD response, the z_c expression can be determined in terms of the GD and C using (23) by applying $f = f_0$ in (20) - (22), as follows:

$$z_c = \frac{2\tau^{\text{Type-III}}_{f=f_0} \times f_0 C^2}{\sqrt{1-C^2}}. \tag{23}$$

The relation between the C, GD and f_0 of the type-III circuit that provides the flat GD response over a wide bandwidth can be empirically written using (24), as follows:

$$C\ (dB) = \delta - 20\log\left(\sqrt{\tau^{\text{Type-III}}_{f=f_0} \times f_0}\right) \tag{24}$$

where δ is a factor that controls the $\Delta\tau_{ripple}$.

Fig. 11 shows the calculated GD responses of the type-III circuit with different δ values. The design specification and calculated circuit parameters are given in Table 3. As observed from Fig. 11, the GD bandwidth was increased with the decreasing C of the coupled lines. Like type-I and type-II circuits, the $\Delta\tau_{ripple}$ was decreased and approached being flat as δ was increased.

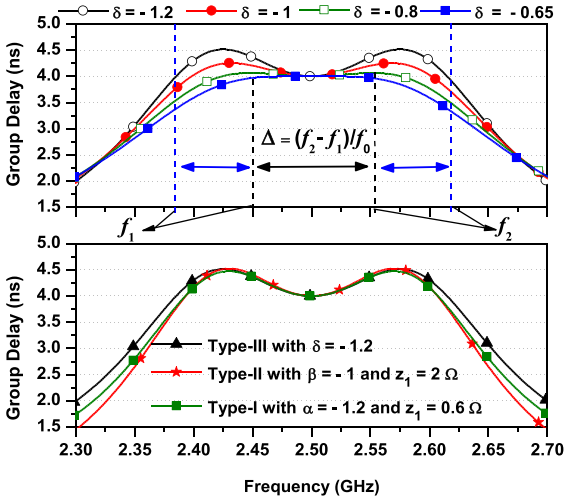

FIGURE 11. Calculated responses of the reflective type-III wideband flat group delay circuit with $\tau = 4$ ns at $f_0 = 2.5$ GHz and different δ values and compared with other types of group delay circuits.

TABLE 3. Calculated parameters of reflective type-III group delay circuit.

Specification : $\tau^{\text{Type-III}}_{f=f_0} = 4$ ns and $f_0 = 2.5$ GHz				
δ	-1.20	-1	-0.80	-0.65
$\Delta\tau_{ripple}$ (%)	12.0567	6.1254	1.5989	0.0158
Δ (%)	9.20	8.20	6.30	3.60
C (dB)	-11.20	-11	-10.80	-10.650
z_c (Ω)	1.5782	1.6558	1.7373	1.8013
z_{0e} (Ω)	2.0938	2.2121	2.3377	2.4371
z_{0o} (Ω)	1.1895	1.2394	1.2912	1.3313

Fig. 11 also shows the comparison of the GD responses of type-I, type-II, and type-III circuits. As noted from this figure, the GD responses of all of the circuits are almost the same. The advantages of the type-III circuit are a compact circuit size and a slightly wider GD bandwidth compared to type-I and type-II circuits.

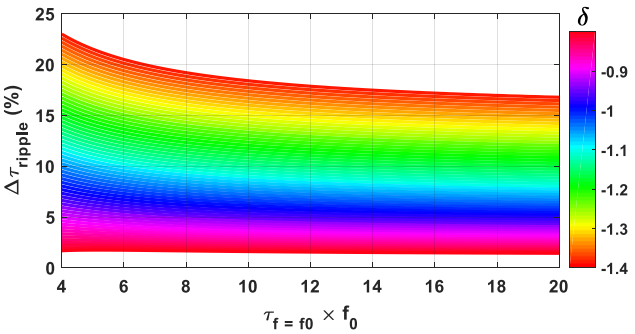

FIGURE 12. Calculated z_C and C for the flat wideband group delay characteristics of the reflective type-III circuit.

Fig. 12 shows the calculated $\Delta\tau_{ripple}$ of the type-III circuit with different δ values. As can be seen from the figure, the $\Delta\tau_{ripple}$ can be minimized by increasing the δ. In general, a higher δ is preferable for the minimum $\Delta\tau_{ripple}$.

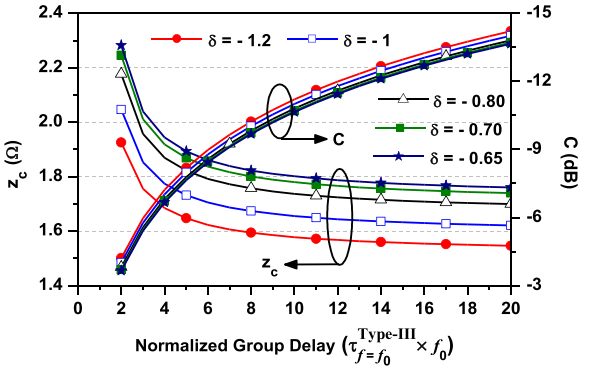

FIGURE 13. Calculated z_c and C for the flat wideband group delay characteristics of the reflective type-III circuit.

Fig. 13 shows the computed z_c and C with the normalized GD for different δ values. As depicted in this figure, the values of C and z_c were decreased with the increasing of the normalized GD. In addition, the z_c became higher as the δ was decreased. Since the $\Delta\tau_{ripple}$ depends on the δ, the GD response can be designed with a specified $\Delta\tau_{ripple}$.

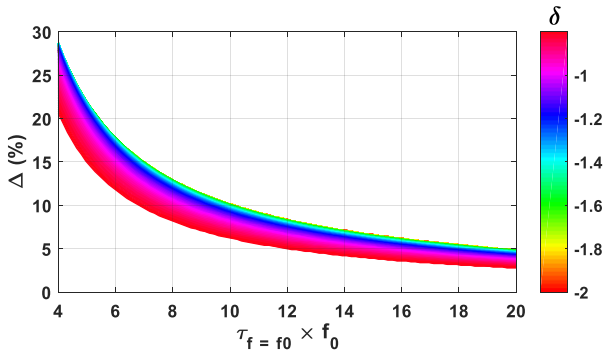

FIGURE 14. Calculated in-band group fractional bandwidth of the type-III circuit.

When the z_c and C are determined based on a design specification (such as the GD at f_0 with the $\Delta\tau_{ripple}$), it is possible to calculate the GD fractional bandwidth by finding the cut-off frequencies from (21) using MATLAB. Fig. 14 shows the computed Δ for different δ values. As observed from this graph, the variation of Δ is almost like those of the type-I and type-II circuits.

III. IMPLEMENTATION OF TWO-PORT NETWORKS USING HYBRID COUPLER

The reflection termination units can be combined to form a two-port network by using a hybrid coupler as shown in Fig. 15. The assumption of the coupled and through responses of the hybrid coupler in Fig. 15 are S_{21}^H and S_{31}^H, respectively. The S-parameters of the two-port hybrid network combined with the two reflection termination units are expressed by [16].

$$S_{11} = \left[\left(S_{21}^H\right)^2 + \left(S_{31}^H\right)^2\right]\Gamma_i^c = R^H\Gamma_i^c,$$
$$S_{21} = 2S_{21}^H S_{31}^H\Gamma_i^c = T^H\Gamma_i^c \quad (25)$$

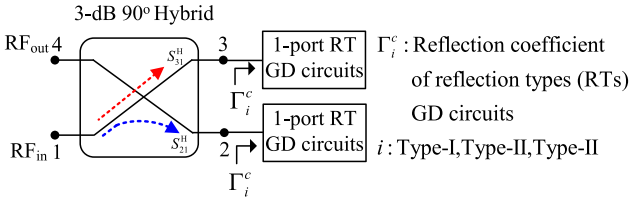

FIGURE 15. Two-port configuration of the combined reflective-type wideband group delay circuits.

The combined two-port GD circuit would exhibit a perfect matching ($S_{11} = 0$) and transmission ($S_{21} = 1$), but only if the hybrid coupler exhibited the S-parameters such that $|R^H| = |(S_{21}^H)^2 + (S_{31}^H)^2| = 0$ and $|T^H| = |2S_{21}^H S_{31}^H| = 1$, respectively. Since the bandwidths of requirements are practically limited, any hybrid coupler implementation will affect the magnitude and GD responses of the overall combined two-port circuit. Therefore, the designer should choose a wideband hybrid coupler with a flat transmission magnitude and a high return loss of more than 20 dB over a wide operating band. The effect of the hybrid on the GD response of the combined two-port network may be quantified by adding the GD of hybrid to the GD of the coupled line reflection terminations. Since hybrid introduced GD can be considered constant over the bandwidth of the combined two-port GD circuit, the overall GD of the combined circuit is expressed by (26), as follows:

$$\tau_{21} = \tau_i^c + \tau^H = \tau_i^c + \text{const.}, \quad (26)$$

where τ_i^c is the GD of the reflective type of the GD circuits, whereas τ^H is the GD of the hybrid. The expression (26) shows that the hybrid is essentially transparent to the reflective coupled line termination GD circuit at its coupled and through ports.

Based on the analysis and discussion in the previous sections, the design method of the proposed GD circuits is summarized as follows:

a) Specify the center frequency (f_0), GD, and minimum in-band GD ripple ($\Delta\tau_{\text{ripple}}$).
b) Specify value of the z_1 in cases of type-I and type-II circuits. Type-I: $0.4 \le z_1 \le 0.9\ \Omega$ (refer to Fig. 5). Type-II: $1.6 \le z_1 \le 2.4\ \Omega$ (refer to Fig. 9).
c) Attainment of the values of factors (α, β and δ) for the specified $\Delta\tau_{ripple}$. The values of the α, β and δ can be estimated using Fig. 4, Fig. 8, and Fig. 12, respectively.
d) Calculate the C and z_c using (9) - (10) for type-I, (17) - (18) for type-II, and (23) - (24) for type-III circuit.
e) Calculate the overall magnitude/GD responses using (4) - (7) for type-I, (13) - (16) for type-II, and (19) - (22) for type-III circuit.
f) Calculate the Δ using (6) for type-I, (15) for type-II and (21) for type-III circuit. Alternatively, Refer Fig. 6, Fig. 10 and Fig. 14 for type-I, -II and -III circuits, respectively.

g) Obtain physical dimensions: length, width, and spacing of coupled line and TL using ADS LinCal for the specified substrate.
h) Convert the one-port to the two-port network using a hybrid coupler and finally, optimize the physical dimensions using a EM simulator.

IV. EXPERIMENTAL DEMONSTRATION AND RESULTS

For the experimental demonstration, prototypes were designed for GD of 4 ns at $f_0 = 2.5$ GHz and fabricated on RT/Duroid 5880 substrate with a dielectric constant (ε_r) of 2.20 and thickness (h) of 0.787 mm. The simulation was performed co-simulation using ANSYS HFSS 15 and ADS 2016. In these works, ANAREN hybrid coupler S03A2500N1was used.

A. RESULTS OF WIDEBAND REFLECTIVE TYPE-I GROUP DELAY CIRCUIT

Assuming hybrid with GD = 0.2 ns, the reflective type-I circuit is designed for a GD of 3.8 ns with an $\Delta\tau_{\text{ripple}}$ of 6%. Using design method that is previously described, the calculated circuit parameters for the given specification are determined as $z_1 = 0.55\ \Omega$, $z_c = 2.0469\ \Omega$, $C = -21.0967$ dB, $z_{0e} = 2.2360\ \Omega$, and $z_{0o} = 1.8738\ \Omega$. These circuits are renormalized with respect to the port impedance of 50 Ω for the implementation on the specified substrate. The physical dimensions were obtained using ADS LinCal and they were optimized using a co-simulation between the HFSS and ADS software packages. Fig. 16 shows the layout and a photograph of the fabricated circuit.

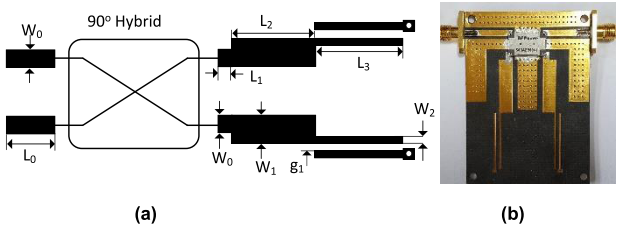

FIGURE 16. (a) Layout and (b) photograph of fabricated reflective type-I circuit. Physical dimensions: $L_0 = 10$, $L_1 = 3$, $L_2 = 22.2$, $L_3 = 21.9$, $W_1 = 5.10$, $W_2 = 0.6$, $g_1 = 1.35$. (Unit: millimeter).

Fig. 17 shows the simulated and measured GDs and S-parameter magnitudes of type-I circuit. The measurement results agree well with the simulation results. From the measurement, the GD and the insertion loss are determined as $\tau_{f=f_0}^{Type-I} = 3.98$ ns and $|S_{21}| = -1.63$ dB, respectively. In addition, the maximum GD is flat over frequency range of 2.41 to 2.63 GHz with the $\Delta = 8.8$ %. The return losses in overall measured bandwidth are greater than −21 dB.

B. RESULTS OF THE WIDEBAND REFLECTIVE TYPE-II GROUP DELAY CIRCUIT

Similar to the type-I circuit, a prototype of the type-II circuit was designed and fabricated at $f_0 = 2.5$ GHz with a GD of 4 ns and a $\Delta\tau_{ripple}$ of 3.2%. The calculated circuit parameters of the designed circuit are given as $z_1 = 2.3\ \Omega$,

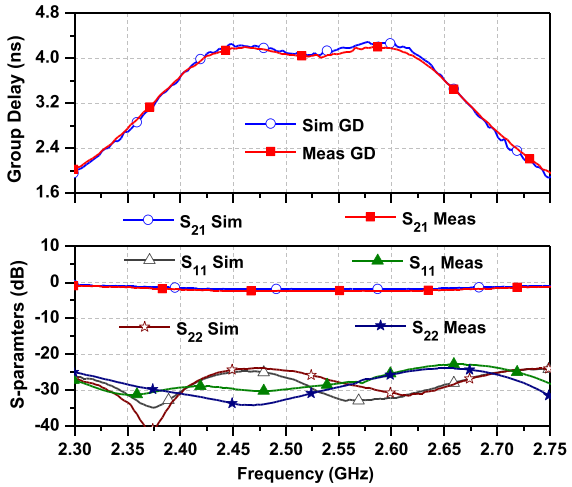

FIGURE 17. Simulated and measured results of reflective type-I group delay circuit.

$z_c = 0.9747\ \Omega$, $C_{eff} = -20.0545$ dB, $z_{0e} = 1.0769\ \Omega$ and $z_{0o} = 0.8822\ \Omega$. Fig. 18(a) shows the layout and physical dimensions of the designed circuit while photograph of fabricated circuit is presented in Fig. 18(b).

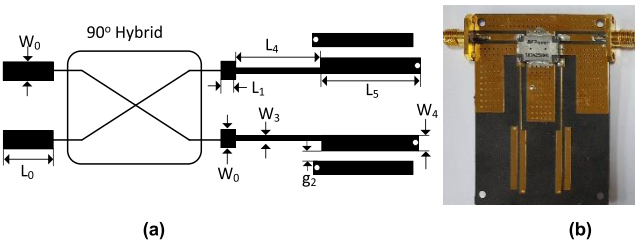

FIGURE 18. ((a) Layout and (b) photograph of fabricated reflective type-II circuit. Physical dimensions: $L_0 = 10$, $L_1 = 3$, $L_4 = 22$, $L_5 = 22$, $W_3 = 0.4$, $W_4 = 2$, and $g_2 = 1.06$. (Unit: millimeter).

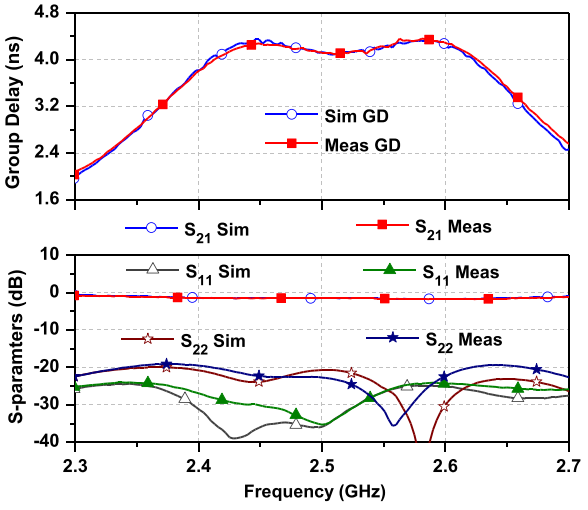

FIGURE 19. Simulated and measured group delay and magnitude of reflective type-II circuit.

Fig. 19 shows the simulated and measured GDs and S-parameter magnitudes. The measured GD and magnitude at $f_0 = 2.5$ GHz were determined as $\tau^{\text{Type-II}} = 4.10$ ns

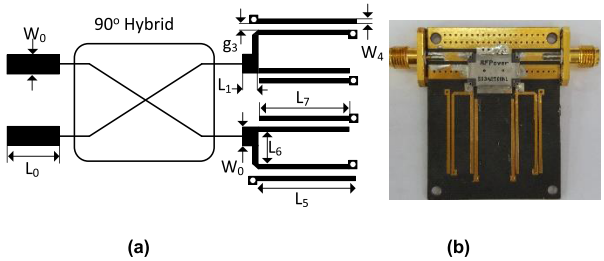

FIGURE 20. (a) Layout and (b) photograph of fabricated reflective type-III circuit. Physical dimensions: $L_0 = 10$, $L_5 = 21.5$, $L_6 = 4.40$, $L_7 = 22$, $W_0 = 21$, $W_4 = 0.82$, and $g_3 = 0.37$. (Unit: millimeter).

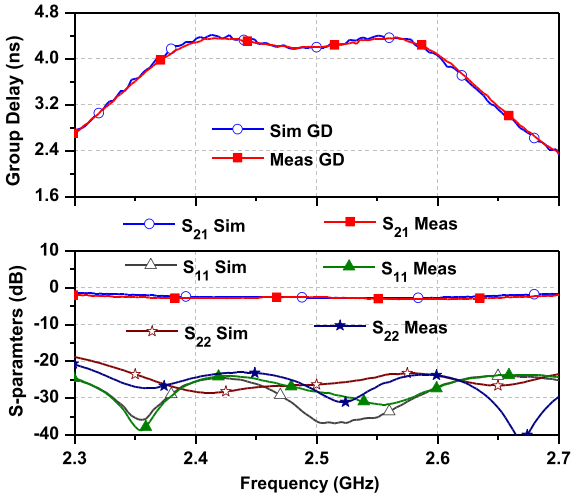

FIGURE 21. Simulated and measured results of reflective type-III group delay circuit.

and $|S_{21}| = -1.47$ dB, respectively. In addition, the measured flat GD fractional bandwidth is given as 8.7%. Similarly, the measured input and output return losses at f_0 are $|S_{11}| = -21.28$ dB and $|S_{22}| = -23.75$ dB, respectively.

C. RESULTS OF WIDEBAND REFLECTIVE TYPE-III GROUP DELAY CIRCUIT

For experimental validation of the type-III circuit, a prototype was designed and fabricated at $f_0 = 2.5$ GHz with a GD of 4 ns and a $\Delta\tau_{ripple}$ of 3.5%. The calculated circuit parameters for the given specification were obtained as $z_{0e} = 2.0938\ \Omega$, and $z_{0o} = 1.1895\ \Omega$. Fig. 20 shows the layout and a photograph of circuit type-III with physical dimensions.

Fig. 21 shows the measured and simulated S-parameters and GDs. From the experiment, the GD is 4.20 ns at f_0 and $\Delta\tau_{ripple}$ is 3.52%. In addition, the flat GD fractional bandwidth of the fabricated the type-II circuit is 8.4%. Similarly, the measured S-parameters at the f_0 are $|S_{21}| = -2.05$ dB, $|S_{11}| = -26.29$ dB, and $|S_{22}| = -28.33$ dB, respectively.

D. RESULTS OF COMBINED CIRCUITS FOR PRESCRIBED HIGHER FLAT GROUP DELAY

The higher flat GD response can be realized by a cascading sufficient number of combined reflective-type circuits

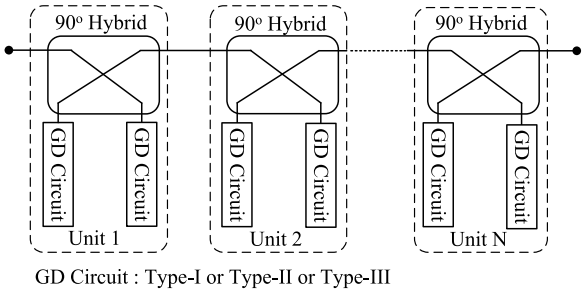

FIGURE 22. Wideband group delay circuit from a cascading of the N units of reflective type circuits.

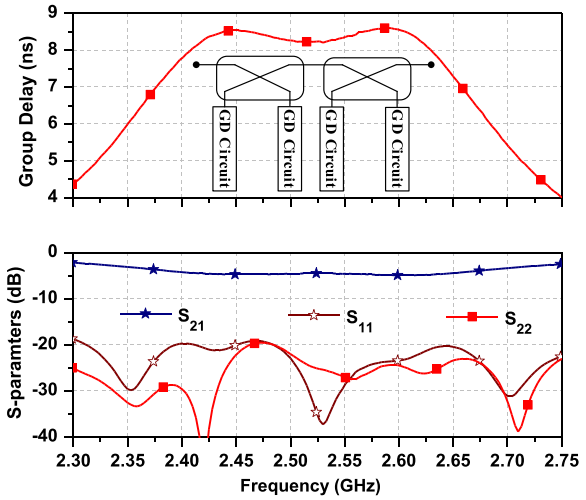

FIGURE 23. Wideband group delay circuit from a cascading of the N units of reflective-type circuits.

TABLE 4. Performance comparison.

	f_0 (GHz)	S_{21max} (dB)	τ_{max} (ns)	Δ (%)	Method
[13]	1.60	<-10	8.5	0.625	Iterative
[15]	1.0	<-30	10.0	2	Analytical
[16]	2.14	<-5.9	4.0	2.803	Analtytical
[17]	2.50	<-1.69	4	8.40	Analytical
[22]	0.5	<-1.5	2.30	40*	Iterative
[24]	2.10	<-1.5	6	9.52	Iterative
This work^{I}	**2.50**	**<-1.63**	**4.0**	**8.8**	**Analytical**
This work^{II}	**2.50**	**<-1.47**	**4.10**	**8.7**	**Analytical**
This work^{III}	**2.50**	**<-2.05**	**4.20**	**8.4**	**Analytical**
This work^{IV}	**2.50**	**<-3.56**	**8.22**	**8.4**	**Analytical**

Δ = Fractional bandwidth of flat group delay, * = Ideal simulated result

as shown in Fig. 22, and this contribute the GD at center frequency to form overall GD response. To avoid an imbalance, each of the combined GD circuits should be identical.

For the experimental demonstration, two units of the reflective type-I circuit with a GD of 4.10 ns were cascaded

and measured. Fig. 23 shows the experiment results of the cascaded two units of the reflective type-I circuits, which provides the GD at $f_0 = 2.5$ is 8.22 ns with the $\Delta\tau_{ripple} = 3.46\%$ and the $\Delta = 8.4\%$. The measured S-parameters at f_0 are given as $|S_{11}| = -31.2$ dB, $|S_{22}| = -24.78$ dB and $|S_{21}| = -3.56$ dB.

Table 4 shows the performance comparison of the proposed work with the state-of-art works. As can be seen from this table, the proposed work provides a wideband flat GD and a GD enhancement capability. In addition, the proposed structures are very simple and transformative (bandpass to low-pass domain and then, back to bandpass domain) processes are not required to calculate circuit parameters.

V. CONCLUSION

This work consists of presentation of the reflection-type wideband flat group delay circuits (type-I, type-II, and type-III) for which coupled lines are used. The analytical design equations that were used for calculation of the circuit parameters with arbitrarily specified group delay are supplied. For the experimental validation, the prototypes of wideband group delay circuits were fabricated at the center frequency of 2.5 GHz. To obtain a higher group delay with the wideband bandwidth, a number of reflection-type GD circuit units were cascaded. The experiment results indicate that the proposed structures can provide a wideband flat group delay response, and are applicable to various RF/microwave circuits, such as the wideband analog RF self-interference cancellation, the RF amplifier linearization, and real-time analog radio signal processing.

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