Arbitrary Prescribed Wideband Flat Group Delay Circuits Using Coupled Lines

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***Abstract*— This paper presents the analytical design of transmission-type arbitrary prescribed wideband flat group delay (GD) circuits (type-I and type-II) using λ/4 coupled lines. The GD circuit type-I consists of two sections of coupled lines, whereas the GD circuit type-II consists of λ/4 transmission lines (TLs) at input and output, in addition to coupled lines. The additional λ/4 TLs at input–output ports in GD circuit type-II provide more freedom to obtain larger GD, as compared to type-I, without fabrication difficulties. The analytical analysis shows that the wideband flat GD response can be obtained by selecting the appropriate even- and odd-mode impedances of coupled lines and the characteristic impedance of TLs. To obtain the arbitrary prescribed wideband flat GD response, the closed-form analytical design equations are provided. For experimental validation of the proposed structures, prototypes of GD circuits (type-I and type-II) are designed and fabricated at the center frequency of 2 GHz. The measurement results agree well with the simulation and theoretical predicted results.**

***Index Terms*— Analog radio-signal processing, arbitrary wideband flat group delay (GD) response, coupled lines, signal cancellation, transmission-type circuit.**

I. Introduction

MICROWAVE circuits/filters that provide the desired group delay (GD) response with respect to frequency have various applications in communication systems including real-time analog radio-signal processing, RF self-interference cancellation in-band full-duplex radio, and signal cancellation in feed-forward amplifier [1]–[5]. The GD can be investigated by examining the frequency-dependent phase variation of transmitting scattering parameter, which can be mathematically defined as

$$\tau_g = -\frac{d\varphi}{d\omega}. \tag{1}$$

The flat GD in filters can be achieved by two approaches. The first one is to use an external all-pass GD circuits cascaded with a filter [6]–[21], which can increase circuit size and insertion loss. All-pass GD circuits can be categorized into reflection and transmission types.

Reflection-type all-pass GD circuits can be realized by terminating coupled and through ports of a 3-dB hybrid coupler with one-port GD circuit, and the GD response of resulting two-port network is added up GD responses of the hybrid and one-port terminating circuit [6], [7]. A coupled-resonator network approach was utilized to design the GD equalizers using optimization procedures in [8] and [9]. A narrowband one-port circuits with an arbitrary prescribed GD response was synthesized in [10]. Later, this technique was improved and applied to the design of reflective GD circuits based on shunt stubs and stepped-impedance lines [11], alternating K/J inverters and $\lambda/4$ transmission line (TL) resonators [12], [13]. However, these techniques require complex iterative procedures for transformation of the prescribed GD problem from band-pass domain to the low-pass domain using a one-port ladder network, and again, the transformation of the synthesized low-pass network back to the band-pass domain, for implementation in a specific technology.

Transmission-type all-pass GD circuits are realized using multisection coupler-based superconductive delay [14], cascading of all-pass networks [15], [16], and noncommensurate coupled lines by multiconductor TL technique [17]. However, this structure requires genetic optimization technique to implement final structure. Similarly, wideband all-pass GD circuits were synthesized by using uniform and nonuniform commensurate C- and D-sections [18], [19], multilayer broadside coupled lines GD circuit for analog signal processing [20]. However, these works require an iterative design procedure to map arbitrary prescribed GD problem from band-pass domain to low-pass domain and again back to band-pass domain for obtaining the optimum circuit parameters. Similarly, the transmission-type GD lines had been realized by employing a transversal filter structure, were realized with the reverse of a distributed amplifier [21], and required complex iterative procedures to obtain a large number of tap coefficients for specified GD response.

The second approach is to design self-equalized or linear-phase filters which can be achieved by imposing linear-phase requirement in addition to the amplitude requirement [22]–[27]. However, these techniques require cross-coupling among nonadjacent resonators to produce more than one signal path or controlling sign of cross-coupling to place the transmission zeros on the right half plane. In addition, it is also difficult to specify and design arbitrarily prescribed flat GD filters directly in band-pass domain using these techniques.

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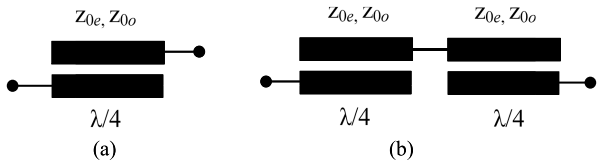

Fig. 1. (a) Coupled line and (b) proposed structure of wideband GD circuit type-I.

Fig. 2. Equivalent circuits of the proposed GD circuit type-I under (a) even- and (b) odd-mode excitations.

In this paper, arbitrarily prescribed wideband flat GD circuits are presented based on coupled lines. This paper shows an alternative way to realize flat GD filters which are very simple and do not require any cross-coupling among non-adjacent resonators or controlling sign of cross-coupling or any kind of transformation to obtain the required circuit parameters. The closed-form analytical design equations are provided to obtain the required circuit parameters for the arbitrarily prescribed wideband flat GD response without any optimization procedure.

II. Mathematical Analysis

Fig. 1(a) shows the structure of $\lambda/4$ coupled lines, where the coupled and through ports are open circuited [28]. The even- and odd-mode impedances of coupled line are normalized with port impedance Z_0 and denoted by z_{0e} and z_{0o}, respectively. Assuming $z_c = \sqrt{z_{0e} z_{0o}}$, normalized z_{0e} and z_{0o} are expressed as follows [28], [29]:

$$z_{0e} = z_c \sqrt{\frac{1 + C_{\text{eff}}}{1 - C_{\text{eff}}}} \qquad z_{0o} = z_c \sqrt{\frac{1 - C_{\text{eff}}}{1 + C_{\text{eff}}}} \tag{2}$$

$$C_{\text{eff}} = \frac{z_{0e} - z_{0o}}{z_{0e} + z_{0o}} \tag{3}$$

where C_{eff} is coupling coefficient of the coupled line. The z-parameters of the coupled lines shown in Fig. 1(a) can be expressed in terms of z_c and C_{eff} as

$$[z] = \begin{bmatrix} -j\dfrac{z_c}{\sqrt{1 - C_{\text{eff}}^2}} \cot \dfrac{\pi f}{2 f_0} & -j\dfrac{z_c C_{\text{eff}}}{\sqrt{1 - C_{\text{eff}}^2}} \csc \dfrac{\pi f}{2 f_0} \\ -j\dfrac{z_c C_{\text{eff}}}{\sqrt{1 - C_{\text{eff}}^2}} \csc \dfrac{\pi f}{2 f_0} & -j\dfrac{z_c}{\sqrt{1 - C_{\text{eff}}^2}} \cot \dfrac{\pi f}{2 f_0} \end{bmatrix} \tag{4}$$

where f and f_0 are the operating and the design center frequency, respectively. Based on z-parameters, the input impedance of coupled lines with termination load z_L can be calculated as

$$z_{\text{in}} = z_{11} - \frac{z_{12} z_{21}}{z_{22} + z_L}. \tag{5}$$

A. Wideband Flat Group Delay Circuit Type-I

Fig. 1(b) shows the proposed structure of the wideband GD circuit type-I. Since the structure is symmetrical, the even- and odd-mode analyses can be applied to find S-parameters. From the equivalent circuit of the even-mode excitation shown in Fig. 2(a), the even-mode input impedance can be expressed as (6) using (4) and (5), with $z_L = \infty$

$$z_{\text{ine}}^{\text{Type-I}} = -j \frac{z_c}{\sqrt{1 - C_{\text{eff}}^2}} \cot \frac{\pi f}{2 f_0}. \tag{6}$$

Similarly, Fig. 2(b) shows the equivalent odd-mode excitation circuit. The odd-mode input impedance of the subcircuit shown in Fig. 2(b) can be determined as (7) by using (4) and (5), with $z_L = 0$

$$z_{\text{ino}}^{\text{Type-I}} = -j \frac{z_c}{\sqrt{1 - C_{\text{eff}}^2}} \left(\cot \frac{\pi f}{2 f_0} - 2 C_{\text{eff}}^2 \csc \frac{\pi f}{f_0} \right). \tag{7}$$

The S-parameters of the wideband GD circuit type-I shown in Fig. 1(b) can be found as (8) using (6) and (7)

$$\begin{aligned} S_{11\_\text{Type-I}} &= S_{22\_\text{Type-I}} \\ &= \frac{z_{\text{ine}}^{\text{Type-I}} z_{\text{ino}}^{\text{Type-I}} - 1}{\left(z_{\text{ine}}^{\text{Type-I}} + 1\right)\left(z_{\text{ino}}^{\text{Type-I}} + 1\right)} \\ &= \frac{x_3}{(1 - j x_1)(1 - j x_2)} \end{aligned} \tag{8}$$

$$\begin{aligned} S_{21\_\text{Type-I}} &= S_{12\_\text{Type-I}} \\ &= \frac{z_{\text{ine}}^{\text{Type-I}} - z_{\text{ino}}^{\text{Type-I}}}{\left(z_{\text{ine}}^{\text{Type-I}} + 1\right)\left(z_{\text{ino}}^{\text{Type-I}} + 1\right)} \\ &= \frac{j 2 x_4}{(1 - j x_1)(1 - j x_2)} \end{aligned} \tag{9}$$

where

$$x_1 = \frac{z_c}{\sqrt{1 - C_{\text{eff}}^2}} \left(\cot \frac{\pi f}{2 f_0} \sin \frac{\pi f}{f_0} - 2 C_{\text{eff}}^2 \right) \tag{10}$$

$$x_2 = \frac{z_c}{\sqrt{1 - C_{\text{eff}}^2}} \cot \frac{\pi f}{2 f_0} \tag{11}$$

$$x_3 = \frac{z_c^2}{1 - C_{\text{eff}}^2} \left(\cot^2 \frac{\pi f}{2 f_0} \sin \frac{\pi f}{f_0} - C_{\text{eff}}^2 \cot \frac{\pi f}{2 f_0} \right) - \sin \frac{\pi f}{f_0} \tag{12}$$

$$x_4 = \frac{2 z_c}{\sqrt{1 - C_{\text{eff}}^2}} \left(\cot \frac{\pi f}{2 f_0} \sin \frac{\pi f}{f_0} - C_{\text{eff}}^2 \right). \tag{13}$$

Similarly, the GD of the circuit type-I can be calculated as

$$\tau_{\text{Type-I}} = -\frac{1}{2\pi} \frac{d \angle S_{21\_\text{Type-I}}}{df} = \frac{z_c \sqrt{1 - C_{\text{eff}}^2}}{4 f_0} \left(\frac{x_5}{x_6} + \frac{1}{x_7} \right) \tag{14}$$

where

$$x_5 = \csc^2 \frac{\pi f}{2 f_0} \sin^2 \frac{\pi f}{f_0} - 4 C_{\text{eff}}^2 \cos \frac{\pi f}{f_0} \tag{15}$$

$$x_6 = \left(1 - C_{\text{eff}}^2\right) \sin^2 \frac{\pi f}{f_0} + z_c^2 \left(\cot \frac{\pi f}{2 f_0} \sin \frac{\pi f}{f_0} - 2 C_{\text{eff}}^2 \right)^2 \tag{16}$$

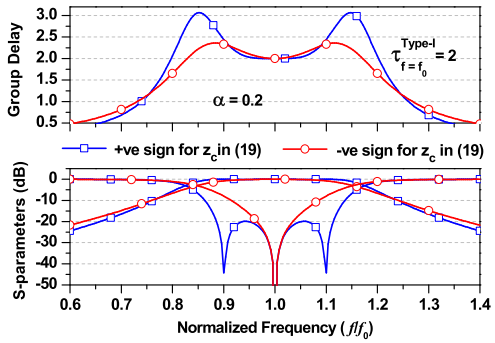

Fig. 3. Calculated results of the wideband flat GD circuit type-I.

$$x_7 = \sin^2\frac{\pi f}{2f_0}\left(1 - C_{\text{eff}}^2\right) + z_c^2\cos^2\frac{\pi f}{2f_0}. \tag{17}$$

As seen from (14)–(17), the GD depends on z_c and C_{eff} of the coupled lines. Further, the GD at f_0 can be simplified as

$$\tau_{f=f_0}^{\text{Type-I}} = \frac{1 - C_{\text{eff}}^2 + z_c^2 C_{\text{eff}}^2}{4f_0 z_c C_{\text{eff}}^2\sqrt{1 - C_{\text{eff}}^2}}. \tag{18}$$

An arbitrarily specified flat GD response can be obtained by selecting appropriate z_c and C_{eff}. For this purpose, we need to solve the value of z_c using (18). Therefore, the solution of z_c in terms of specified GD and C_{eff} can be found as

$$z_c = \sqrt{1 - C_{\text{eff}}^2}\left(2f_0\tau_{f=f_0}^{\text{Type-I}} \pm \sqrt{\left(2f_0\tau_{f=f_0}^{\text{Type-I}}\right)^2 - 1/C_{\text{eff}}^2}\right). \tag{19}$$

As noted from (19), z_c has two unique solutions, and the values are real and positive if

$$C_{\text{eff}}(\text{dB}) = \alpha - 20\log\left(2f_0\tau_{f=f_0}^{\text{Type-I}}\right) \tag{20}$$

where α is a positive factor which provides a degree of freedom to control C_{eff} and GD ripples. In this paper, in-band GD ripple ($\Delta\tau_{\text{ripple}}$) is defined as

$$\Delta\tau_{\text{ripple}} = \frac{\tau_{\max} - \tau_{f=f_0}}{\tau_{f=f_0}} \times 100\%. \tag{21}$$

Here, $\tau_{\max}$ is the maximum GD at passband-edge frequency. The required value of C_{eff} can be obtained using (20) for the specified GD with acceptable $\Delta\tau_{\text{ripple}}$.

Based on the above analytical analysis, Fig. 3 shows the calculated magnitudes/GD responses for circuit type-I. Table I gives the calculated circuit parameters. As shown in Fig. 3, z_c with a positive sign in (19) provides the wideband return loss characteristics with three poles; however, the GD at band edge has a high peak. Similarly, it is observed that GD is flat over the wideband when negative sign assigned in (19) for the solution of z_c. However, return loss is slightly narrow due to only one pole.

Similarly, Fig. 4 shows the calculated magnitude/GD responses with a variation of α. In the case of positive sign in (19), $\Delta\tau_{\text{ripple}}$ at in-band and band-edge frequencies are increased as α increased; however, impedance matching decreases. On the contrary, when α increased, $\Delta\tau_{\text{ripple}}$ is decreased and GD approaches toward flat in the case of the negative sign in (19).

TABLE I
CALCULATED CIRCUIT PARAMETERS OF CIRCUIT TYPE-I WITH POSITIVE AND NEGATIVE SIGNS IN (19)

Group delay specification : $\tau_{f=f_0}^{\text{Type-I}} = 2$ and $\Delta\tau_{\text{ripple}} = \frac{\tau_{\max} - \tau_{f=f_0}}{\tau_{f=f_0}} \times 100\%$				
Parameters	Case 1: +ve sign in (12)		Case 2: -ve sign in (12)	
$\Delta\tau_{\text{ripple}}$ (%)	53.18	67.89	17.94	1.88
$\Delta_{\text{Type-I}}$ (%)	40.25	43.5	34	21
α	0.2	0.85	0.2	0.80
C_{eff} (dB)	-11.8412	-11.1912	-11.8412	-11.2412
z_c (Ω)	4.6873	5.4661	3.0465	2.2690
z_{0e} (Ω)	6.0890	7.2542	3.9576	3.0061
z_{0o} (Ω)	3.6082	4.1187	2.3452	1.7126

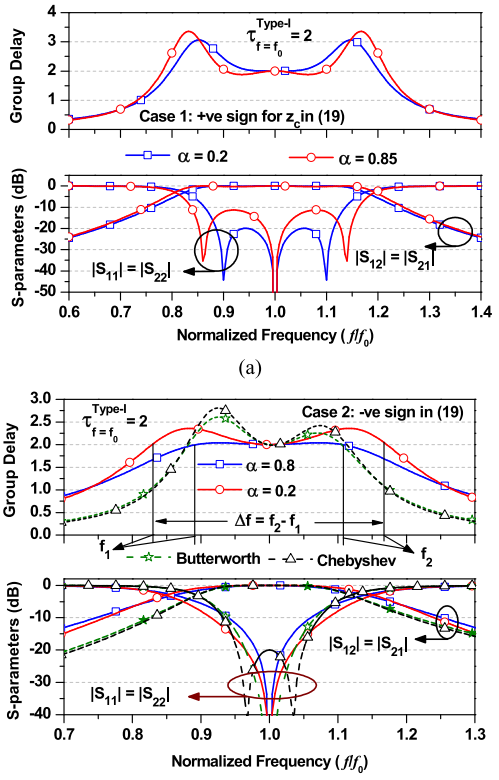

Fig. 4. Calculated GD/magnitude response of the proposed circuit type-I with different α and according to (a) positive sign (case 1) and (b) negative sign (case 2) in (19) for the solution of z_c. Here, f_1 and f_2 are lower and upper cutoff frequencies when passband-edge GD approximately equals to GD at f_0.

Meanwhile, the return loss bandwidth decreases, therefore, a tradeoff occurs between wideband flat GD and return loss. Also, it is concluded from this analysis that for wideband flat GD response and minimum $\Delta\tau_{\text{ripple}}$, the negative sign in (19) is preferable.

Fig. 4(b) also shows the comparison results of the proposed circuit with conventional Butterworth and Chebyshev filters for the same GD at f_0 and return loss bandwidth specification. As shown in Fig. 4(b), the proposed circuit can provide the flat GD response as compared to conventional filters.

To investigate the effect of selecting α, Fig. 5(a) shows the calculated $\Delta\tau_{\text{ripple}}$ from (14) and (21) using MATLAB when

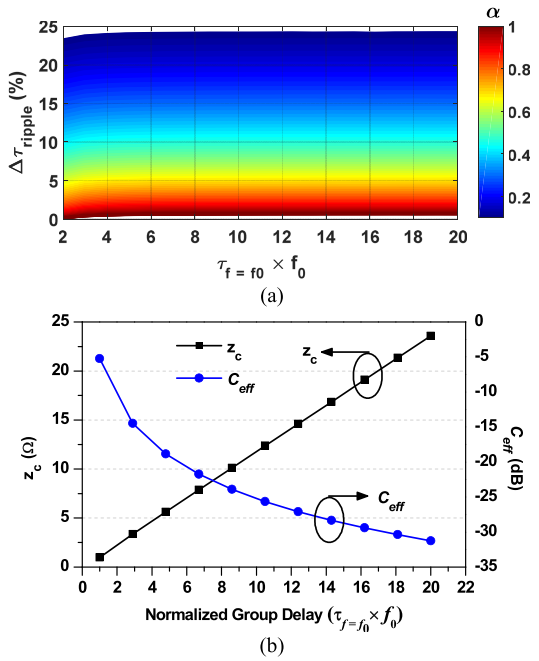

Fig. 5. (a) Calculated in-band GD ripples from (14) and (21) using MATLAB for different α. (b) Circuit parameters of wideband flat GD of circuit type-I with a negative sign in (19) and $\alpha = 0.8$.

negative sign is selected in (19). As observed from Fig. 5(a), the $\Delta\tau_{\text{ripple}}$ is decreased as α increased. In general, higher α is preferable for minimum $\Delta\tau_{\text{ripple}}$.

Fig. 5(b) shows design graphs to calculated circuits parameters for specified flat GD. As seen from this graph, the z_c increases and C_{eff} decreases as the GD increases. Therefore, the circuit type-I could have difficulty in practical realization in single-layer PCB technology for higher GD. This problem can be solved by circuit type-II which will be discussed in later section in detail.

Based on the above analysis, the negative sign in (19) is preferable for minimum $\Delta\tau_{\text{ripple}}$. Once z_c and C_{eff} are determined for the specified GD at f_0 and minimum $\Delta\tau_{\text{ripple}}$, we should find the cutoff frequencies where the GD is approximately equal to GD at f_0, as shown in Fig. 4(b). Using (14), the GD fractional bandwidth of type-I circuit ($\Delta_{\text{Type-I}}$) can be calculated as

$$\Delta_{\text{Type-I}} = \frac{f_2 - f_1}{f_0} = f\,(z_c, C_{\text{eff}}) \tag{22}$$

where f_1 and f_2 are lower and upper cutoff frequencies in between which the GD is equal to desired GD at f_0, as shown in Fig. 4. Since it is complicate to find f_1 and f_2 using (14), analytically, we used numerical method in MATLAB by sweeping frequency to find $\Delta_{\text{Type-I}}$ for mathematical simplicity. Fig. 6 shows the calculated $\Delta_{\text{Type-I}}$ for different α. As GD is increased, $\Delta_{\text{Type-I}}$ decreased. In addition, $\Delta_{\text{Type-I}}$ is slightly higher when α is small; however, the small α increases $\Delta\tau_{\text{ripple}}$. The design steps to calculate circuit parameters of circuit type-I with specified GD can be described with the flowchart shown in Fig. 7.

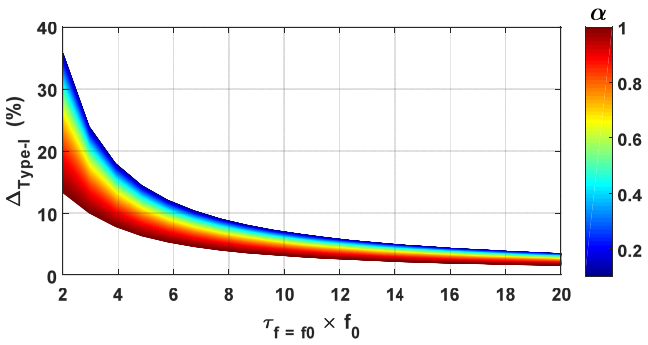

Fig. 6. Calculated GDs fractional bandwidth ($\Delta_{\text{Type-I}}$) of type-I circuit for different α. Color bar represents different α values.

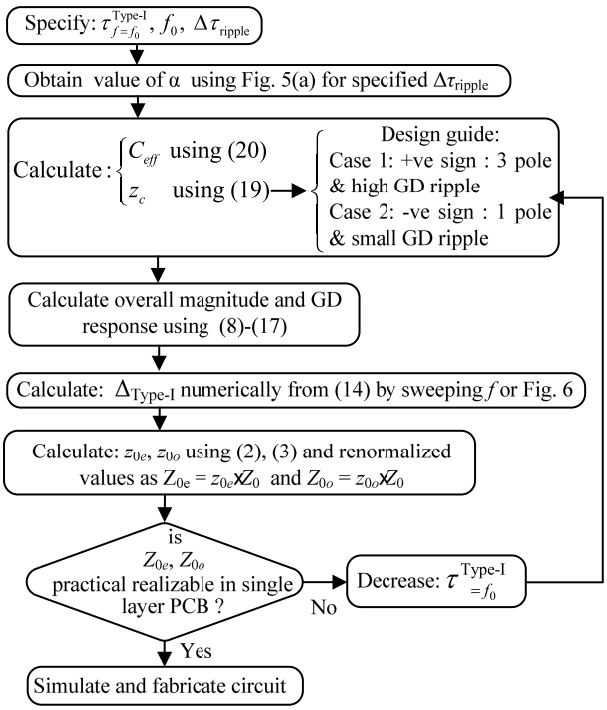

Fig. 7. Design flowchart to calculate circuit parameters of wideband GD circuit type-I.

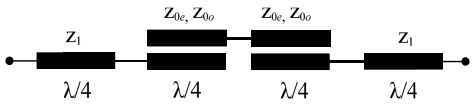

Fig. 8. Proposed structure of the wideband GD circuit-II.

B. Wideband Flat Group Delay Circuit Type-II

To overcome the limitation of wideband GD circuit type-I, $\lambda/4$ TLs with a characteristic impedance of z_1 are added at the input and output ports of GD circuit type-I, and Fig. 8 shows the proposed structure. Due to $\lambda/4$ TLs, the proposed circuit type-II provides the extra degree of freedom, so that realizable circuit parameters can be obtained for high GD. Fig. 9 shows the equivalent circuits of the proposed circuit type-II under even- and odd-mode excitations. Therefore, the even- and odd-mode impedances of circuit type-II can be obtained from Fig. 9

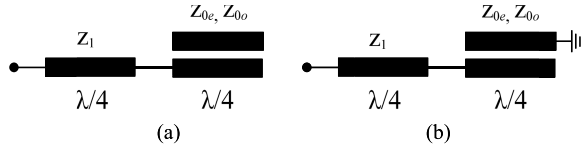

Fig. 9. Equivalent circuits of the proposed GD circuit type-II under (a) even- and (b) odd-mode excitations.

and are expressed as (23) and (24), shown at the bottom of this page.

The S-parameter of circuit type-II can be found as (25) and (26) by using (23) and (24)

$$\begin{aligned} S_{11\_\text{Type-II}} &= S_{22\_\text{Type-II}} \\ &= \frac{z_{\text{ine}}^{\text{Type-II}} z_{\text{ino}}^{\text{Type-II}} - 1}{\left(z_{\text{ine}}^{\text{Type-II}} + 1\right)\left(z_{\text{ino}}^{\text{Type-II}} + 1\right)} \\ &= \frac{x_9 x_{11} - x_8 x_{10}}{(x_8 - j x_9)(x_{10} + j x_{11})} \end{aligned} \tag{25}$$

$$\begin{aligned} S_{21\_\text{Type-II}} &= S_{12\_\text{Type-II}} \\ &= \frac{z_{\text{ine}}^{\text{Type-II}} - z_{\text{ino}}^{\text{Type-II}}}{\left(z_{\text{ine}}^{\text{Type-II}} + 1\right)\left(z_{\text{ino}}^{\text{Type-II}} + 1\right)} \\ &= \frac{j(x_9 x_{10} + x_8 x_{11})}{(x_8 - j x_9)(x_{10} + j x_{11})} \end{aligned} \tag{26}$$

where

$$x_8 = \cot\frac{\pi f}{2f_0} \tag{27}$$

$$x_9 = \frac{z_1}{z_1\sqrt{1 - C_{\text{eff}}^2} + z_c}\left(z_c \cot^2\frac{\pi f}{2f_0} - z_1\sqrt{1 - C_{\text{eff}}^2}\right) \tag{28}$$

$$x_{10} = 2\left(z_1\sqrt{1 - C_{\text{eff}}^2} + z_c\right)\cos^2\frac{\pi f}{2f_0} - 2z_c C_{\text{eff}}^2 \tag{29}$$

$$\begin{aligned} x_{11} = {} & z_1^2\sqrt{1 - C_{\text{eff}}^2}\sin\frac{\pi f}{f_0} - 2z_c z_1 \cos^2\frac{\pi f}{2f_0}\cot\frac{\pi f}{2f_0} \\ & + 2z_c z_1 C_{\text{eff}}^2 \cot\frac{\pi f}{2f_0}. \end{aligned} \tag{30}$$

Finally, the GD of circuit type-II can be expressed as (31) by using (26)–(30)

$$\begin{aligned} \tau_{\text{Type-II}} &= -\frac{1}{2\pi}\frac{d\angle S_{21\_\text{Type-II}}}{df} = -\frac{1}{2\pi}\frac{d\angle S_{12\_\text{Type-II}}}{df} \\ &= \frac{1}{2\pi}\left(\frac{x_8' x_9 - x_8 x_9'}{x_8^2 + x_9^2} + \frac{x_{10} x_{11}' - x_{10}' x_{11}}{x_{10}^2 + x_{11}^2}\right) \end{aligned} \tag{31}$$

where

$$x_8' = -\frac{\pi}{2f_0}\csc^2\frac{\pi f}{2f_0} \tag{32}$$

$$x_9' = \frac{\pi}{f_0}\frac{z_1}{z_1\sqrt{1 - C_{\text{eff}}^2} + z_c}\left(-z_c \cot\frac{\pi f}{2f_0}\csc^2\frac{\pi f}{2f_0}\right) \tag{33}$$

$$x_{10}' = -\frac{\pi}{f_0}\left(z_1\sqrt{1 - C_{\text{eff}}^2} + z_c\right)\sin\frac{\pi f}{f_0} \tag{34}$$

$$x_{11}' = \left\{\begin{array}{l} \dfrac{\pi z_1^2\sqrt{1 - C_{\text{eff}}^2}}{f_0}\cos\dfrac{\pi f}{f_0} - \dfrac{\pi z_c z_1 C_{\text{eff}}^2}{f_0}\csc^2\dfrac{\pi f}{2f_0} \\ + \dfrac{\pi z_c z_1}{f_0}\cot^2\dfrac{\pi f}{2f_0} + \dfrac{2\pi z_c z_1}{f_0}\cos^2\dfrac{\pi f}{2f_0} \end{array}\right\}. \tag{35}$$

Furthermore, the GD at f_0 can be simplified in the following equation:

$$\tau_{f=f_0}^{\text{Type-II}} = \frac{1}{4f_0}\left(\frac{\begin{array}{l} z_c^2 C_{\text{eff}}^2 + z_1 z_c\sqrt{1 - C_{\text{eff}}^2}C_{\text{eff}}^2 \\ + z_1^3\sqrt{1 - C_{\text{eff}}^2}C_{\text{eff}}^2 z_c + z_1^4\left(1 - C_{\text{eff}}^2\right) \end{array}}{z_1^2\sqrt{1 - C_{\text{eff}}^2}C_{\text{eff}}^2 z_c}\right). \tag{36}$$

As seen from (31)–(36), the circuit type-II has more degree of freedom in circuit parameters (such as z_1) than that of type-I; therefore, the limitation in the practical implementation of type-I for higher GD can be overcome with the proposed structure of type-II. The additional TLs mean that z_{0e} and z_{0o} can be reduced to a lower value for higher GD.

The required value of z_c with specified flat GD can be found by solving (36) in terms of C_{eff} and GD at f_0 as

$$z_c = \frac{z_1}{2}\sqrt{1 - C_{\text{eff}}^2}\left(b \pm \sqrt{b^2 - 4z_1^2/C_{\text{eff}}^2}\right) \tag{37}$$

where

$$b = 4f_0\tau_{f=f_0}^{\text{Type-II}} z_1 - z_1^2 - 1. \tag{38}$$

From (37), the value of z_c is real and positive only if

$$C_{\text{eff}}(\text{dB}) = \beta + 20\log\left(\frac{2z_1}{b}\right) \tag{39}$$

where β is a positive factor that controls the $\Delta\tau_{\text{ripple}}$. Like the circuit type-I, the β must be positive value which will provide a degree of freedom to control $\Delta\tau_{\text{ripple}}$. The required value of C_{eff} can be calculated using (39) when a designer specifies GD at f_0 and z_1. In addition, z_c has two unique solutions depending on positive and negative sign in (37).

$$z_{\text{ine}}^{\text{Type-II}} = \frac{j z_1}{z_1\sqrt{1 - C_{\text{eff}}^2} + z_c}\left(z_1\sqrt{1 - C_{\text{eff}}^2}\tan\frac{\pi f}{2f_0} - z_c\cot\frac{\pi f}{2f_0}\right) \tag{23}$$

$$z_{\text{ino}}^{\text{Type-II}} = j\frac{z_1^2\sqrt{1 - C_{\text{eff}}^2}\sin\frac{\pi f}{f_0} - 2z_c z_1\cos^2\frac{\pi f}{2f_0}\cot\frac{\pi f}{2f_0} + 2z_c z_1 C_{\text{eff}}^2\cot\frac{\pi f}{2f_0}}{\left(2z_1\sqrt{1 - C_{\text{eff}}^2} + 2z_c\right)\cos^2\frac{\pi f}{2f_0} - 2z_c C_{\text{eff}}^2} \tag{24}$$

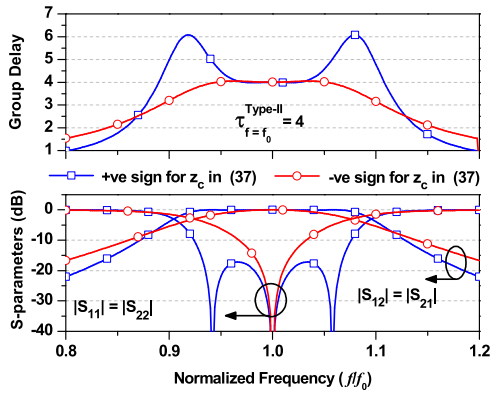

Fig. 10. Synthesized magnitude/GD response of circuit type-II.

Fig. 10 shows the calculated magnitude/GD responses of circuit type-II. As like the circuit type-I, the solution of z_c with a positive sign in (37) provides wide return loss characteristics with three poles; however, peaks occur in GD characteristics at band-edge frequencies. These peaks in GD can be minimized by obtaining a solution of z_c with a negative sign in (37), as shown in Fig. 10. However, only one pole occurs at the center frequency when the GD is flat. In general, the negative sign in (37) is preferable for wideband flat GD with minimum ripple.

Fig. 11(a) shows the synthesized magnitude/GD response of type-II with different C_{eff} and positive sign in (37) for the solution of z_c. As shown in Fig. 11(a), ripples in GD at in-band and band-edge frequencies increase as β increases. However, the return loss bandwidth increases with the decrease of maximum achievable return loss magnitude.

Similarly, Fig. 11(b) shows the calculated magnitude/GD responses of type-II with different β and negative sign in (37) for the solution of z_c. The responses of the proposed circuit type-II are also compared with conventional Butterworth and Chebyshev filter response for the same GD at f_0 and return loss bandwidth specification. The value of $\Delta\tau_{\text{ripple}}$ is decreased and approached toward flat GD characteristics as β increases in the proposed circuit. However, the return loss bandwidth slightly decreases. Therefore, a tradeoff occurs between wideband flat GD and return loss bandwidth.

To investigate the effect of selecting β, Fig. 12 shows numerically calculated $\Delta\tau_{\text{ripple}}$ of circuit type-II with different z_1 and β using (21) and (31) in MATLAB. As shown in Fig. 12, $\Delta\tau_{\text{ripple}}$ can be minimized by increasing the value of β. In general, higher β is preferable for minimum $\Delta\tau_{\text{ripple}}$.

Fig. 13 shows the design graph to calculate the circuit parameters of circuit type-II with specified GD. From this graph, the value of z_c increases and C_{eff} decreases as GD increases. It is also clear from this graph that practical realizable circuit parameters of coupled lines can be obtained by appropriately selecting z_1. Specifically, the low z_1 is preferable for high GD and practical realizable z_c and C_{eff}.

Like the type-I circuit, once the circuit parameters such as z_1, z_c, and C_{eff} are determined based on specifications (GD, f_0, and $\Delta\tau_{\text{ripple}}$), we sweep frequency in (31) under condition $\tau_{\text{Type-II}} = \tau_{f=f_0}^{\text{Type-II}}$, as shown in Fig. 11, for finding

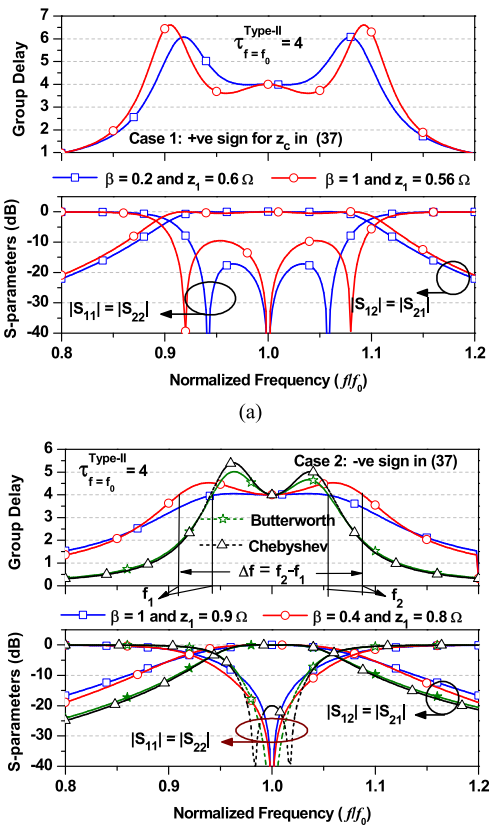

Fig. 11. Calculated results of wideband flat GD circuit type-II with different β and according to (a) positive sign (case 1) and (b) negative sign (case 2) in (37) for the solution of z_c. Here, f_1 and f_2 are lower and upper cutoff frequencies when passband-edge GD approximately equals to GD at f_0.

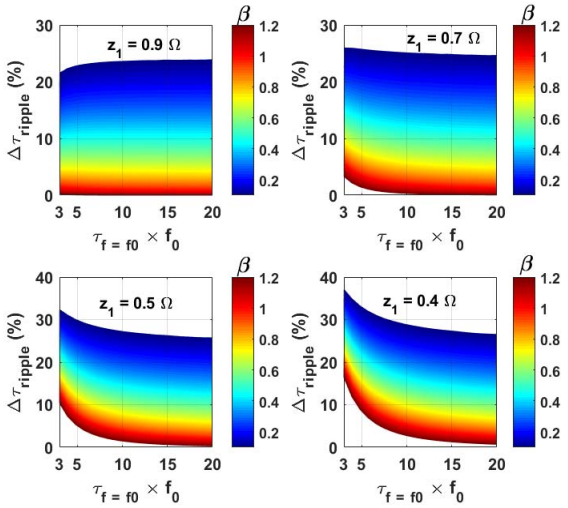

Fig. 12. Calculated in-band group ripples of type-II circuit from (21) and (31) using MATLAB for different z_1 and β with a negative sign in (37). Color bar represents different β values.

lower and upper cutoff frequencies. Finally, the GD fractional bandwidth ($\Delta_{\text{Type-II}}$) can be found as

$$\Delta_{\text{Type-II}} = \frac{f_2 - f_1}{f_0} = f\,(z_1, z_c, C_{\text{eff}}) \tag{40}$$

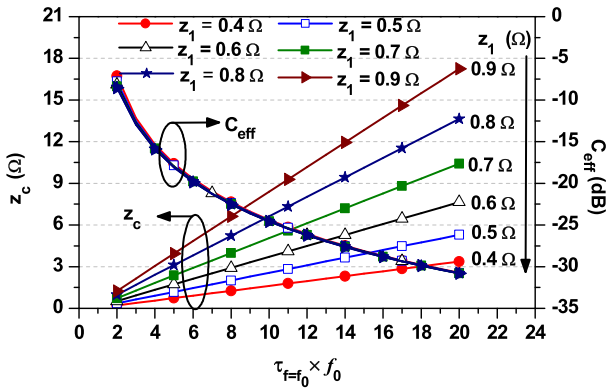

Fig. 13. Calculated z_c and C_{eff} for flat wideband GD characteristics of circuit type-II with $\beta = 0.9$ and negative sign in (37).

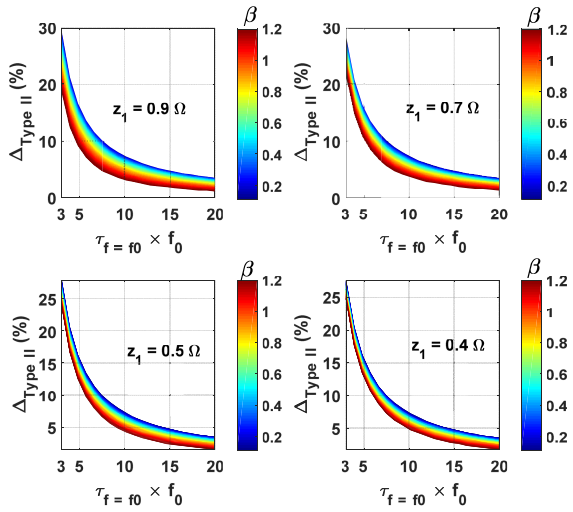

Fig. 14. Calculated GD fractional bandwidth ($\Delta_{\text{Type-II}}$) of type-II circuit for different β and z_1. Color bar represents different β values.

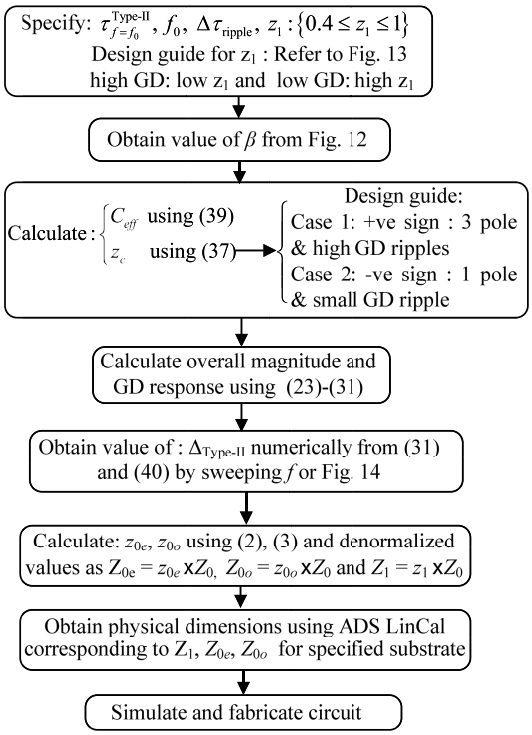

Fig. 15. Design flowchart to calculate circuit parameters of wideband GD circuit type-II.

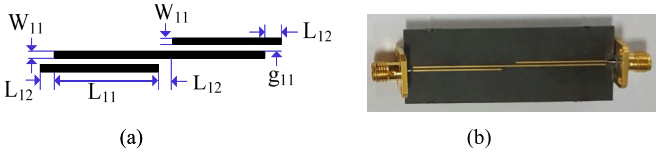

Fig. 16. (a) Layout of the wideband flat GD circuit-I with physical dimensions. (b) Photograph of the fabricated circuit. Physical dimensions: $L_{11} = 28.6$, $L_{12} = 3.9$, $L_{12} = 2.5$, $W_{11} = 0.43$, and $g_{11} = 0.48$ (unit: mm).

where f_1 and f_2 are lower and upper cutoff frequencies in between which the GD is within the desired GD at f_0.

Fig. 14 shows the calculated $\Delta_{\text{Type-II}}$ for different values of z_1 and β. From these graphs, Δ is decreased as GD increases. And Δ is slightly higher with small β. As like the type-I, Fig. 15 summarizes the design steps to calculate circuit parameters of circuit type-II with specified GD and the minimum $\Delta\tau_{\text{ripple}}$.

III. Implementation and Results

For experimental demonstration, prototypes of GD circuit type-I and type-II were designed and fabricated on RT/Duroid 5880 substrate with a dielectric constant (ε_r) of 2.20 and a thickness (h) of 0.787 mm. In this paper, we designed prototype circuits for flat (minimum ripples) GD. The simulation was performed using ANSYS HFSS 15.

A. Results of Wideband Flat Group Delay Circuit Type-I

For experimental validation, we set the design goal of circuit type-I as $\tau^{\text{Type-I}}_{f=f_0} = 1$ ns at $f_0 = 2$ GHz with acceptable $\Delta\tau_{\text{ripple}}$ of less than 1.3%. Using design flowchart shown in Fig. 7, the calculated circuit parameters for given specification are determined as $\alpha = 0.85$, $z_c = 2.2239\ \Omega$, $C_{\text{eff}} = -11.1912$ dB, $z_{0e} = 2.9514\ \Omega$, and $z_{0o} = 1.6757\ \Omega$. Using these circuit parameters, the calculated $\Delta_{\text{Type-I}}$ of the designed circuit is given as 19.1%. The renormalized circuit parameters of coupled lines with respect to 50-Ω port impedances are $Z_{0e} = 147.5699\ \Omega$ and $Z_{0o} = 83.7849\ \Omega$. Fig. 16(a) shows the layout and physical dimensions while Fig. 16(b) shows a photograph of fabricated circuit. In this layout, small length L_{12} is added for connecting port. For minimizing the effect of L_{12}, the same length is also added in another side of coupled lines [30].

Fig. 17 shows the simulated and measured GDs and S-parameter magnitudes. The measurement results agree well with simulation and theoretical predicated results. From the measurement, the GD and magnitude of transmission coefficient at $f_0 = 2$ GHz are determined as $\tau^{\text{Type-I}}_{f=f_0} = 0.998$ ns and $|S_{21}| = -0.42$ dB, respectively. In addition, the GD is flat in frequency extending from 1.78 to 2.15 GHz, with flat GD fractional bandwidth of 18.5%. Similarly, the input and output return losses at f_0 are measured as $|S_{11}| = -26.87$ dB and $|S_{22}| = -32.32$ dB, respectively.

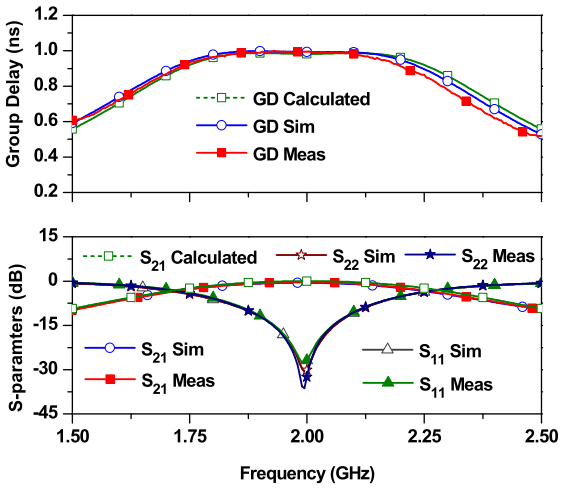

Fig. 17. Simulation and measured results of GD circuit type-I.

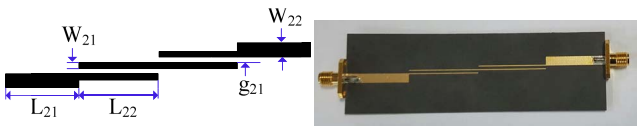

Fig. 18. (a) Layout of the wideband flat GD circuit type-II with physical dimensions. (b) Photograph of the fabricated circuit.

B. Results of Wideband Flat Group Delay Circuit Type-II

For experimental validation of circuit type-II, the prototype circuit was designed and fabricated at $f_0 = 2$ GHz with $\tau_{f=f_0}^{\text{Type-II}} = 2.5$ ns and $\Delta\tau_{\text{ripple}} \leq 2\%$. Assuming $z_1 = 0.72\ \Omega$, the calculated circuit parameters for the given specification are obtained as $\beta = 1.1$, $z_c = 2.4240\ \Omega$, and $C_{\text{eff}} = -17.9321$ dB using the proposed design method described previously. The calculated $\Delta_{\text{Type-II}}$ of the design circuit is given as 10.1% using above circuit parameters (z_1, z_c, and C_{eff}). The renormalized circuit parameters of designed prototype are $Z_1 = 36\ \Omega$, $Z_{0e} = 137.6923\ \Omega$, and $Z_{0o} = 106.6857\ \Omega$. Fig. 18 shows the layout and photograph of the fabricated circuit type-II. The physical dimensions of fabricated circuit are given as $L_{21} = 24.90$, $L_{22} = 28.2$, $W_{21} = 0.38$, $W_{22} = 3.80$, and $g_{21} = 1.17$ (unit: mm).

Fig. 19(a) shows the measured and simulated S-parameters and GDs. These results show that the measurement results are in good agreement with the simulation and theoretical predicated values. From experiment, the GD is 2.498 ns at f_0 and flat GD extends from 1.90 to 2.10 GHz. Therefore, the flat GD fractional bandwidth of the fabricated circuit type-II is 10%, which is slightly narrower than that of circuit type-I because of higher GD than circuit type-I. Similarly, the measured S-parameters at $f_0 = 2$ GHz are determined as $|S_{21}| = -0.89$ dB, $|S_{11}| = -28.18$ dB, and $|S_{22}| = -26.28$ dB.

To demonstrate the prototype for higher GD, an extra circuit was designed for GD of 4 ns at $f_0 = 2$ GHz with $\Delta\tau_{\text{ripple}} \leq 8\%$. Assuming $z_1 = 0.4\ \Omega$, the calculated parameters are given as $\beta = 0.9$, $z_{0e} = 1.4215\ \Omega$, and $z_{0o} = 1.2201\ \Omega$. Once circuit parameters are obtained,

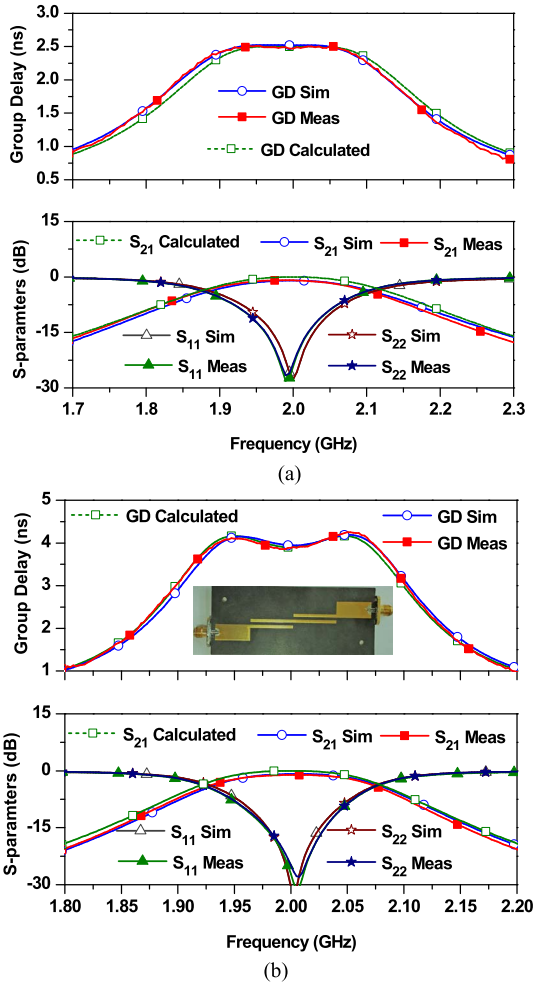

Fig. 19. Simulation and measured results of type-II circuit with GD of (a) 2.5 and (b) 4 ns.

TABLE II
CALCULATED CIRCUIT PARAMETERS OF CIRCUIT TYPE-I WITH POSITIVE AND NEGATIVE SIGNS IN (37)

Group delay specification : $\tau_{f=f_0}^{\text{Type-II}} = 4$ and $\Delta\tau_{\text{ripple}} = \frac{\tau_{\max} - \tau_{f=f_0}}{\tau_{f=f_0}} \times 100\%$				
Parameters	Case 1: +ve sign in (22)		Case 2: -ve sign in (22)	
$\Delta\tau_{\text{ripple}}$ (%)	52.07	65.81	1.22	13.12
$\Delta_{\text{Type-II}}$ (%)	21.81	23.98	10.59	17.73
β	0.2	1	1	0.4
C_{eff} (dB)	-16.5349	-15.6848	-15.8951	-16.4709
z_c (Ω)	2.9630	3.0696	3.0560	3.1043
z_{0e} (Ω)	3.4430	3.6234	3.5928	3.6112
z_{0o} (Ω)	2.5499	2.6005	2.5995	2.6685
z_1 (Ω)	0.60	0.56	0.90	0.80

$\Delta_{\text{Type-II}}$ of circuit is estimated as 7.3% using (31) and (40). Fig. 19(b) shows the measured and simulation results of prototype. The measured GD is 3.96 ns which extends from 1.93 to 2.074 GHz with $\Delta = 7.20\%$. Similarly, the measured $|S_{21}|$, $|S_{11}|$, and $|S_{22}|$ at f_0 are determined as -1.10, -27.2, and -24.94 dB, respectively.

Table III shows performance comparison of the proposed work with state of the arts. As seen from Table III, the proposed work provides wide flat GD. In addition, the proposed

TABLE III
PERFORMANCE COMPARISON

	f_0 (GHz)	S_{21max} (dB)	τ_{max} (ns)	Δ (%)	Method	Cross-Coupling/ No. of Resonators
[6]	1.0	<-30	10.0	2	Analytical	x
[7]	2.14	<-5.9	4.0	2.803	Analtytical	x
[11]	0.50	<-1.5	2.30	40*	Analytical	x
[13]	2.10	<-6.5	6.0	9.52	Iterative	x
[21]	1.93	<-2.5	16**	0.25	Iterative	Yes/6
[23]	0.947	<-1.5	15**	4.20	Iterative	Yes/6
[24]	5.0	<-1.5	4.0***	4.0	CM/iterative	Yes/4
[25]	10	<-1.5	7.0***	0.8	CM/iterative	Yes/4
This work	**2.0/2.0/ 2.0**	**<-0.42/-0.89/ <-1.10**	**1.0/2.5/ 4.0**	**18.5/10/ 7.20**	**Analytical /Iterative**	**No/2**

Δ= Fractional bandwidth of flat group delay, * = Ideal simulated result
** = Waveguide linear phase filter, *** = SIW filters,
CM = Coupling matrix synthesis, [6]-[21]: All-pass group delay circuits,
[23]-[25]: linear phase filters

structure is very simple and does not require cross-coupling or controlling sign of cross-coupling.

IV. CONCLUSION

In this paper, we present transmission-type wideband flat GD circuits using coupled lines. The analytical design equations are obtained using symmetrical even- and odd-mode analyses. The circuit parameters for arbitrarily specified flat GD are obtained analytically and do not require any optimization procedures. In addition, the proposed circuits are very simple to design and provide a wideband flat GD without any cross-coupling or controlling sign of cross-coupling. For experimental validation of the proposed structures, the prototypes of wideband GD circuits are fabricated at the center frequency of 2 GHz. The experimental results indicate that the proposed structures provide a wideband flat GD response and are applicable to various RF/microwaves circuits such as wideband analog RF self-interference cancellation, RF amplifier linearization, and real-time analog radio-signal processing.

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