ELectronics EXpress

IEICE Electronics Express, Vol.16, No.7, 1–5

LETTER

A design of source-degenerated CMOS active negative group delay circuit using bonding wire

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Abstract This paper presents a design of CMOS source-degenerated active negative group delay (NGD) circuit by using bonding wire for a compact circuit size. The proposed circuit consists of two cascaded MOSFETs where parallel *RLC* resonator circuits are connected to the source of the MOSFETs. To reduce the size, the parallel *RLC* resonators are implemented with bonding wires and pads. For experimental verification, two-stage NGD circuits with slightly different center frequencies were designed. The measurement results show that the NGD bandwidth, group delay, and gain are 100 MHz, −2.5 ns, and 3 dB, respectively. The measured input/output return losses are higher than 8 dB and 14 dB, respectively, at the center frequency of 1.88 GHz.

Keywords: CMOS integrated circuits, negative group delay (NGD), wire bonding

Classification: Microwave and millimeter-wave devices, circuits, and modules

1. Introduction

Recently, interesting research on the negative group delay (NGD) concept has led to its experimental and applicable validation through its realization in electronic circuits [1]. The NGD occurs at a range of frequencies where the absorption or signal attenuation (SA) is maximum [2, 3]. Therefore, low SA NGD circuits are essential for wireless communication. The NGD circuits have been widely used in practical applications of communication systems, such as shortening or reducing delay lines, enhancing efficiency of feedforward linear amplifier, enhancing bandwidth of feedback amplifier, minimizing beam-squint in phased array antennas systems, realization of non-Foster reactive elements [4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15].

Various structures of passive microwave NGD circuits using lumped RLC and distributed resonators were presented in [16, 17, 18, 19, 20, 21, 22, 23]. The main drawback of passive NGD circuits is their inherent SA, which can be overcome by using a general-purpose gain amplifier; however, this will decrease the overall NGD. In [24, 25, 26, 27, 28, 29], active NGD circuits were presented at the VHF and UHF ranges which occupied large circuit area. Since RFIC CMOS technology is a good candidate among the circuit miniaturization methods, a research on the implementation of active NGD circuits using CMOS technology is essential.

In contrary to conventional active NGD circuits which were implemented using RLC circuit at input/output ports, this paper presents the design and implementation of the active NGD circuit in CMOS process using source-degeneration structure for compact circuit size. The proposed work utilizes the bonding pads and wires to implement the source-degeneration NGD circuit that results in a compact chip size. In addition, the proposed circuit provides wide NGD bandwidth and an improved passband SA.

2. Design equations

Fig. 1(a) shows the proposed structure of the NGD circuit which consists of MOSFET with a series-feedback parallel RLC resonator connected to the source. This source-degeneration structure can have the higher NGD value than conventional structures [25, 26, 27, 28]. The overall Z-parameters of the proposed circuit can be obtained by just adding the individual Z-parameters of MOSFET and the resonator, as shown in Fig. 1(b). So the overall Z-matrix of the proposed NGD circuit can be expressed as (1).

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} v_1^a + v_1^b \\ v_2^a + v_2^b \end{bmatrix} = \begin{bmatrix} Z_{11}^a + Z_{11}^b & Z_{12}^a + Z_{12}^b \\ Z_{21}^a + Z_{21}^b & Z_{22}^a + Z_{22}^b \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \quad (1)$$

where Z-parameters of FET and *RLC* feedback resonator are defined in terms of voltage (v_i) and current (i_j) as shown in (2).

$$Z_{ij}^{a,b} = \left. \frac{v_i^{a,b}}{i_j^{a,b}} \right|_{i_k=0 \text{ for } k \neq j} \quad (2)$$

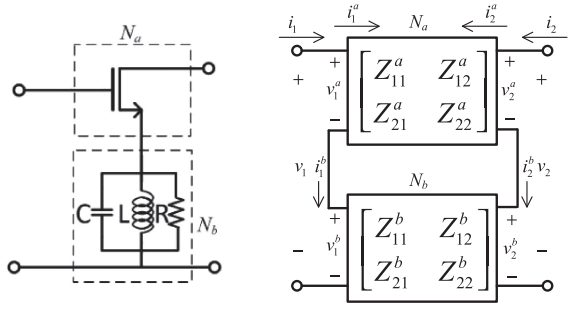

Fig. 1. (a) Basic structure of the proposed NGD circuit and (b) the series-connected Z-parameter.

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DOI: 10.1587/elex.16.20190010
Received January 11, 2019
Accepted January 31, 2019
Publicized March 14, 2019
Copyedited April 10, 2019

Using (1), the overall Z-matrix of the proposed NGD circuit can be represented as (3).

$$Z^{NGD} = \begin{bmatrix} Z_{11}^{NGD} & Z_{12}^{NGD} \\ Z_{21}^{NGD} & Z_{22}^{NGD} \end{bmatrix} = \begin{bmatrix} Z_{11}^{\mathrm{FET}} + Z_L & Z_{12}^{\mathrm{FET}} + Z_L \\ Z_{21}^{\mathrm{FET}} + Z_L & Z_{22}^{\mathrm{FET}} + Z_L \end{bmatrix}, \quad (3)$$

where Z_{11}^{FET}, Z_{12}^{FET}, Z_{21}^{FET}, and Z_{22}^{FET} are the Z-parameters of the MOSFET. Furthermore, the value of Z_L is given as (4).

$$Z_L = \frac{\omega RL}{\omega L + jR(\omega^2 LC - 1)} \quad (4)$$

where R, L, and C are resistance, inductance, and capacitance of parallel RLC feedback resonator, respectively. To analyze the group delay of the proposed NGD circuit, the Z-matrix should be transformed to the S-matrix by using the well-known relation as (5) [30].

$$S^{NGD} = h[Z^{NGD} + z]^{-1}[Z^{NGD} - z]h^{-1} \quad (5)$$

where

$$z = \begin{bmatrix} Z_0 & 0 \\ 0 & Z_0 \end{bmatrix}, \; h = \begin{bmatrix} \sqrt{Z_0} & 0 \\ 0 & \sqrt{Z_0} \end{bmatrix}, \; h^{-1} = \begin{bmatrix} \frac{1}{\sqrt{Z_0}} & 0 \\ 0 & \frac{1}{\sqrt{Z_0}} \end{bmatrix} \quad (6)$$

and Z_0 is termination port impedance. From (5), the GD can be calculated by using phase of transmission coefficient ($\angle S_{21}$) as shown in (7)

$$\tau = -\frac{1}{2\pi}\frac{d\angle S_{21}}{df}, \quad (7)$$

where f is an operating frequency. Since the final analytical expressions of the GD and the transmission magnitude of the proposed NGD circuit are overly complicated, the MATLAB tool was used to analyze the effect of the circuit parameters. For this purpose, the Z-parameters of MOSFET were first extracted using Cadence Tool and then imported to MATLAB and finally, the overall magnitude and GD were calculated by varying the RLC feedback resonator parameters.

Fig. 2 shows the GDs variations with the R, L, and C where the MOSFET size is W/L = 0.11/100 µm at 1.88 GHz with the extracted Z-parameters as: $Z_{11}^{FET} = 133 + j476.5\,\Omega$, $Z_{12}^{FET} = 50.03 - j3.17\,\Omega$, $Z_{21}^{FET} = 561.9 + j7290.61\,\Omega$, and $Z_{22}^{FET} = 229.4 - j15.6\,\Omega$. As shown in Fig. 2(a), low R and high C provide higher NGD when L is fixed. Similarly, higher NGD requires a low L and R as shown in Fig. 2(b).

Based on the parametric analysis, the simulated transmission coefficient (S_{21}) magnitude and GD responses are shown in Fig. 3 for different R values. As shown in this figure, the GD moves toward higher negative value as the R decreases, however, the gain and the NGD bandwidth (bandwidth when GD < 0) are decreased. Therefore, in this work, a small R is selected to obtain high NGD, and 2-stage NGD structure is used to compensate for the SA of the NGD and to enhance the gain.

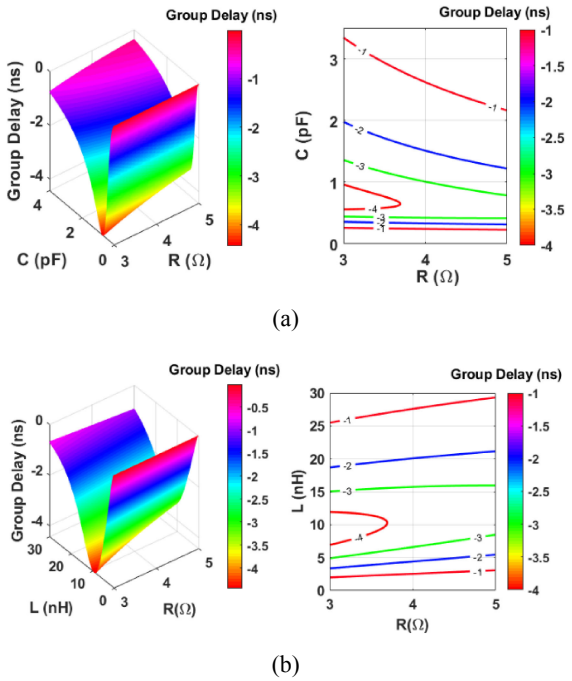


Fig. 2. Calculated group delay (NGD defined as GD < 0) at 1.88 GHz according to different conditions of: (a) R and C variation and (b) R and L variation.

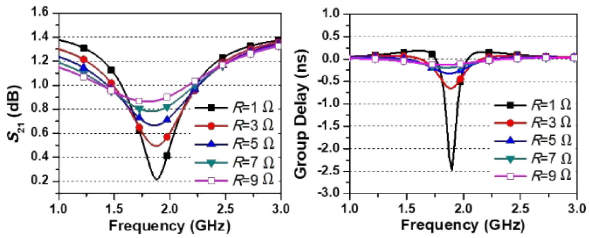


Fig. 3. Simulation results with L = 2 nH, C = 3.58 pF and different R, (a) magnitude of |S21| and (b) group delay.

In the CMOS process, the spiral inductor occupies a large chip area and has a high insertion loss due to the parasitic resistance. Therefore, in this work, inductor was implemented using bonding wire instead of the spiral inductor to obtain a compact size. In addition, Q-factor of inductor implemented by bonding wire is high and adequate for NGD circuit because of small parasitic resistance. The series-feedback RLC resonator in CMOS process can be implemented using the bonding wire (L_b with small resistance R_b) and metal-insulator-metal (MIM) capacitor C_b, as shown in Fig. 4. The equivalent circuit of bonding wire consists of the series R_b and L_b, as shown in Fig. 4. This circuit can be equivalently converted to the parallel RLC. The conversion relation between the circuit parameters of original RLC resonator and the modified resonator is given by (8).

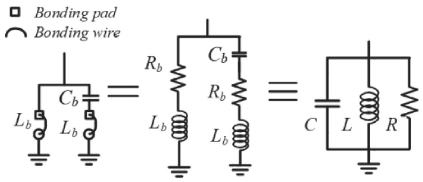


Fig. 4. Proposed series-feedback resonator and its equivalent transformation model.

$$R = \frac{x_1 x_3 + 2\omega C R_b x_2}{x_1^2 + x_2^2}, \tag{8a}$$

$$C = \frac{C_b R_b x_1}{x_1^2 + x_2^2}, \tag{8b}$$

$$L = \frac{x_2 x_3}{\omega_0 (x_1^2 + x_2^2)} \tag{8c}$$

where

$$x_1 = R_b - 2\omega_0^2 L_b C_b \tag{9a}$$

$$x_2 = \omega_0 C R_b^2 - \omega_0^3 L_b^2 C_b + \omega L_b \tag{9b}$$

$$x_3 = 1 - 2\omega_0^2 L_b C_b \tag{9c}$$

3. Experimental results

For the experimental verification, the proposed active NGD circuit with GD of −2.5 ns was designed and implemented in CMOS technology at an operating center frequency (f_0) of 1.88 GHz for advanced wireless service (AWS-2) and the broadband personal communication service (PCS). The parameters of *RLC* feedback resonator shown in Fig. 4 are summarized as $R = 1\,\Omega$, $C = 3.58$ pF and $L = 2$ nH. The MOSFET size is W/L = 0.11/85 µm. The chip was implemented in the standard 0.11 µm RF CMOS process.

In this work, the bonding wire with approximately length of 1 mm was implemented to realize 2 nH inductor at 1.88 GHz by using hand-controlled bonding machine because the bonding wire is generally used in CMOS circuit package. Therefore, the NGD circuit occupies very small circuit area. To implement exact value of inductor with bonding wire, we performed EM simulation of bonding wire including the parasitic components of pad.

Fig. 5(a) shows a circuit diagram of the designed CMOS active NGD circuit which consists of 2-stage MOSFET and series-feedback resonators implemented with the bonding wires and 70 fF MIM capacitors. Similarly, an additional MIM capacitor is attached between the first and second stage MOSFETs for an inter-stage matching. Generally, L- or T-type matching networks are used to match the input/output impedances of MOSFET with port impedances. Even though these matching networks can provide the impedance matching gain, they cause a positive GD and slightly degrade the overall NGD. Therefore, in this work, circuit parameters of shunt-series *RLC* input/output matching networks are given as 50 Ω, 1 nH, and 7 pF, respectively. Although these matching networks sacrifice the matching gain, they are compatible with the input and output ports and also provide

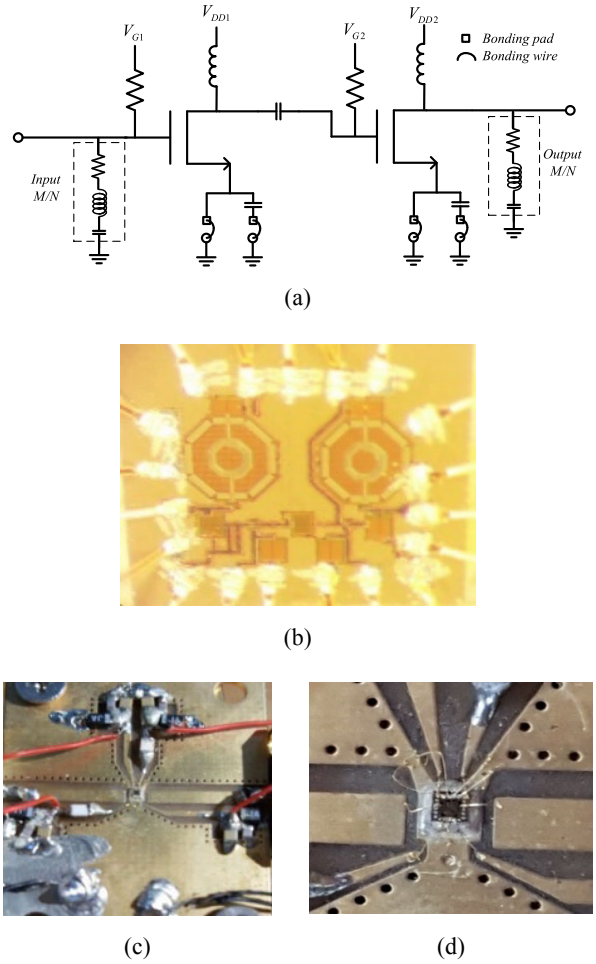
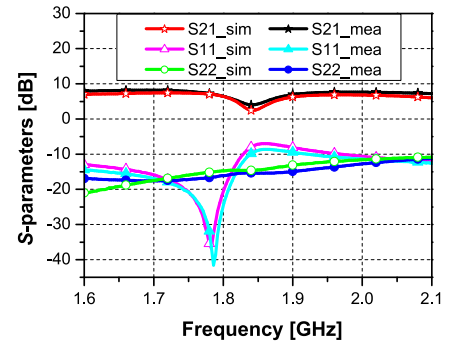


Fig. 5. (a) Schematic, (b) photograph of die, (c) evaluation PCB board and (b) bonding wire connection of the proposed NGD circuit.

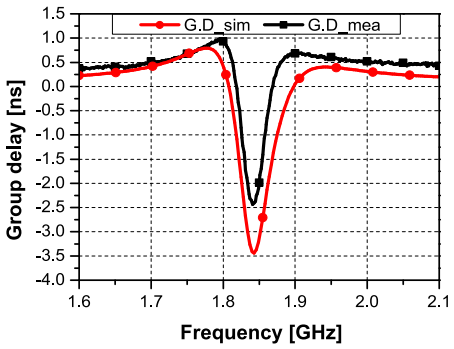
a small NGD [4]. Fig. 5(b)–(d) shows the photograph of the fabricated NGD circuit. The circuit size is 1200 × 1250 µm^2 including the wire bonding pad. The Cadence tool was used for the simulation.

The fabricated NGD circuit was measured at an input power level of −10 dBm. Fig. 6(a) shows the simulated and measured *S*-parameter characteristics. The measured $|S_{11}|$, $|S_{21}|$, and $|S_{22}|$ at f_0 are −8 dB, 3 dB, and −14 dB, respectively. As observed from Fig. 6(a), the proposed circuit provided the 2.8 dB gain at f_0. Similarly, Fig. 6(b) shows the simulated and measured GDs of the designed NGD circuit. From the measurement, the maximum achievable GD is −2.5 ns at f_0 with NGD frequency bandwidth (FBW, where GD < 0 ns) of 100 MHz. Each MOSFET consumed 13 mA at 1.2 V DC supply voltage. The measured output 1-dB compression point is 3 dBm. There is a slight mismatch between the simulated and measured results due to additional parasitic components in the layout. Additionally, since the wire bonding was undertaken manually, the wire bonding inductance is not exactly the same as the simulated inductance, thereby causing a deviation of the measurement results from the simulation.

The NGD occurs at specific frequency band where absorption or insertion loss is maximum; therefore, high NGD and bandwidth can be achieved by accepting increase



(a)



(b)

Fig. 6. Simulated and measured results of the proposed NGD circuit: (a) S-parameters and (b) group delay.

Table I. Performance comparison

	f_0 [GHz]	S_{21} [dB]	GD_{max} [ns]	Size [mm^2]	NGD FBW	Process	FoM [ns/mm]
[25]	1.05	3	−1.16	176.9	0.38	Dis.**	0.046
[26]	2.05	1	−0.92	176.9	0.29	Dis.**	0.022
[27]	1.03	1.68	−2.3	520	0.29	Dis.**	0.035
[28]	19.5	−7.9	−0.083	0.033	0.67	CMOS	0.123
This work	**1.88**	**2.8**	**−2.5**	**1.5**	**0.05**	**CMOS**	**0.141**

NGD FBW: NGD fractional bandwidth = NGD BW (GHz)/f_0 (GHz)

amount of insertion loss. Therefore, the figure of merit (FoM) can be defined as (10) by considering GD, magnitude of $|S_{21}|$, NGD frequency bandwidth (FBW, where GD < 0 ns), and circuit size.

$$\text{FoM} = \frac{\text{GD}_{\max}|_{f=f_0}\ (\text{ns}) \times \text{NGD FBW} \times 10^{\frac{S_{21dB}}{20}}}{\sqrt{\text{Size (mm}^2)}} \quad (10)$$

As shown in Table I, the electrical performances of the fabricated NGD circuit were compared with state-of-art NGD circuits. The proposed circuit provided the highest NGD, a smaller circuit size, and the highest FoM. To the authors' best knowledge, this is the first trial to implement active NGD circuit using CMOS technology.

4. Conclusion

In this paper demonstrated a design of CMOS active NGD circuit using 2-stage cascade MOSFET and series-feedback *RLC* resonators. The source connected resonators were implemented with bonding wire and MIM capacitor for the compact size. For the experimental verification, the proposed circuit was implemented in the CMOS process compact at a center frequency of 1.88 GHz. The proposed circuit can provide the NGD as well as an adequate gain; therefore, the designed circuit is applicable for the positive delay compensation in various RF/microwave circuits and systems as well as realization of non-Foster reactive elements. Also this circuit is easy to apply to a CMOS transceiver system.

Acknowledgments

This research was supported by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2016R1D1A1A09918818) and in part by Korean Research Fellowship Program through the National Research Foundation of Korea (NRF) funded by ministry of Science and ICT (2016H1D3A1938065).

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