Wafer-Level-Packaged *X*-Band Internally Matched Power Amplifier Using Silicon Interposer Technology

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***Abstract*— In this letter, we propose a wafer-level-packaged (WLP) *X*-band internally matched power amplifier (IMPA) using silicon interposer technology. The proposed WLP IMPA consists of a fully embedded commercial GaN HEMT transistor (TR) embedded in the silicon wafer and matching networks. The proposed IMPA enhanced the output power and efficiency compared with the conventional quasi-monolithic microwave integrated circuit (MMIC) high power amplifiers (HPAs) due to removal of bonding wires between matching networks and TR. Further, it provided a high level of integration and reduces the manufacturing cost associated with the silicon interposer technique. For experimental validation, the proposed WLP IMPA was designed and fabricated at 10.2 GHz for military radar application. The results show that the output power and drain efficiency at saturation point were 48.54 dBm (71.45 W) and 50.29%, respectively, based on the pulse signal test (100-μs pulsewidth and 10% duty). The dimensions of the fabricated WLP IMPA were 7.5 mm × 5.8 mm × 0.12 mm.**

***Index Terms*— Embedded transistor (TR), integrated passive device (IPD), internally matched, power amplifier (PA), silicon interposer.**

I. Introduction

THE power amplifier (PA) is the most widely used circuit in radio frequency wireless communication and military radar systems. As the requirements for high power/efficiency in commercial and military PA designs increase, the GaN technology has been widely adopted due to its high output power density, breakdown voltage, efficiency, and other advantages. In addition, the PA size is also an important design issue for the minimization of the physical size of the integrated system and circuit. Various studies have been conducted to fulfill these requirements.

One of the candidate technologies satisfying these criteria involves GaN-on-SiC [1]–[3]. This technology evolved from the conventional GaAs monolithic microwave integrated circuit (MMIC). The GaAs has been replaced by the GaN for the fabrication of transistor (TR) on the SiC substrate. In addition, the SiC substrate exhibits excellent heat dissipation for high output power and efficiency of PA. Therefore, GaN-on-SiC is suited for the design of high-efficiency and high-power MMIC PA and displays high levels of integration. However, since the GaN device is compatible with SiC, the processing difficulty is higher compared with the conventional MMIC technology and the manufacturing cost is higher than the Si substrate.

The quasi-MMIC technology involves a PA using a commercial GaN TR and passive matching circuits connected by bonding wires. This technology yields high output power, efficiency, and integration levels. However, the performances are degraded by the increment of bonding wire insertion loss as the operating frequency increases [4], and the bonding wire limits the packaging of PA. In particular, as the output power of TR increases, the number of pads on the gate and drain increases. Accordingly, the insertion increment cannot be neglected according to the number of bonding wires. Moreover, the manufacturing cost is also increased due to the additional process for circuit arrangement and bond wiring [5], [6].

The passive matching circuit can be realized via a specific printed circuit board (PCB) or conventional MMIC process. When the matching circuit is designed with a specific PCB such as high dielectric and ceramic, only the transmission line (TL) technique can be used, which reduces the design freedom. The manufacturing cost is also increased by the specific PCB usage, which reduces the circuit size [7]. Otherwise, the matching circuit created via conventional MMIC and silicon interposer technologies exhibits high freedom of design and integration levels [8], [9]. However, it still cannot overcome the disadvantages associated with the bonding wiring.

In order to resolve the disadvantages of bonding wiring, the PAs with GaN TR-embedded substrate have been studied [10], [11]. However, these studies exhibit appropriate electrical characteristics only at a relatively low-frequency and low-output power, and not under high-frequency and high-power output.

In this letter, the wafer-level-packaged (WLP) *X*-band internally matched PA (IMPA) using silicon interposer technology is presented. The proposed WLP IMPA provides high output power and high efficiency in *X*-band frequency with a high degree of integration and low manufacturing cost. It provides high design freedom due to the usage of silicon interposer technology. Moreover, the disadvantages of the bonding wiring can be overcome by embedding TR in the silicon substrate. For validation, the design procedure and experimental results of the WLP *X*-band IMPA using silicon interposer technology are provided.

Manuscript received June 19, 2019; revised August 19, 2019; accepted August 25, 2019. Date of publication September 12, 2019; date of current version October 7, 2019. This work was supported in part by the Institute of Civil-Military Technology Cooperation (ICMTC) of South Korea through the ICMTC Program under Grant 16-CM-SS-16 and in part by Chonbuk National University in 2019. *(Corresponding author: Yongchae Jeong.)*

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Digital Object Identifier 10.1109/LMWC.2019.2938309

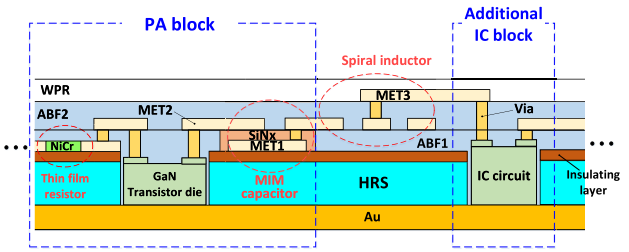


Fig. 1. Lateral view of proposed WLP *X*-band IMPA using silicon interposer technology.

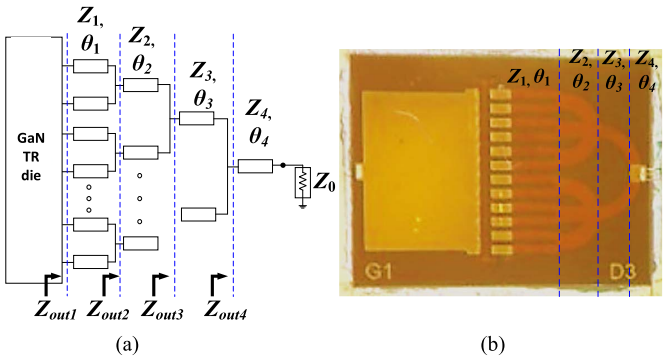
II. Wafer-Level-Packaged X-Band IMPA

Fig. 1 shows the lateral view of the proposed WLP *X*-band IMPA using silicon interposer technology. The fabrication technique is as follows. First, a cavity was made in the high resistive silicon (HRS) substrate using the etching process and a commercial GaN TR was mounted together with an additional IC circuit. The *RLC* passive device and TL were implemented using the conventional silicon interposer technology. Thin-film resistors were implemented using metal 1 (MET1) layer and NiCr. Metal–insulator–metal capacitors were inserted using SiNx between the MET1 and metal 2 (MET2) layers. Spiral inductors were created with patterns in MET2 and metal 3 (MET3) layers connected via hole at the center of the patterns. In addition, the TL schematics were implemented using three metal layers (MET1, MET2, and MET3) resulting in high design freedom due to the *RLC* elements and the TL technology for the passive design of matching circuit. After all the processes in the WPR, photosensitive insulation material product name from JSR Corporation, the layer was completed, the back surface of the HRS substrate was removed to the bottom of the GaN TR via chemical-mechanical polishing, and gold (Au) was deposited to yield the ground structure.

In the design of PAs, the passive matching circuits were connected via interposer using accurate design models and minimizing the length to overcome the disadvantages of the bonding wiring. The specific ICs, additionally inserted according to the system application, can be wired and connected using metal layers. An interstage matching circuit connecting IC blocks can be also implemented using the same method. In addition, the through substrate vias (TSV) also can be used to connect the circuit and the bottom ground. As GaN TR and IC circuits are embedded and packaged on the same wafer, it facilitates automated fabrication, mass production, and high levels of integration.

For experimental validation, the proposed WLP IMPA was designed and fabricated at 10.2 GHz for military radar application. The TR used for the proposed WLP IMPA was 70-W pulse mode GaN HEMT TR (CGHV1J070D) of Wolfspeed. The bias point was set as follows: $V_{DD} = 40$ V, $V_{GS} = -2.75$ V, and $I_{DQ} = 219$ mA. The target performances were greater than 70 W (48.45 dBm) output power and 40% drain efficiency (DE). Using load–pull and source–pull simulations, the optimum output and source impedances were selected as $1.27 + j2.64\ \Omega$ and $0.5\ \Omega$ with 49.27-dBm output power and 53.4% DE.

Fig. 2 shows the fabricated WLP *X*-band IMPA and output matching circuit block diagram. The input matching circuit was realized with a taper structure for very low source impedance ($0.5\ \Omega$). When using multiple metal layers for design, insertion loss is increased due to via connection, so the



(a) (b)

Fig. 2. (a) Block diagram of the output matching circuit. (b) Photograph of the fabricated WLP IMPA.

TABLE I
Impedances at the Branch Plane

Impedances (Ω)			
Z_{out1}	Z_{out2}	Z_{out3}	Z_{out4}
1.27+j2.64	1.15-j2.38	10.26-j12.42	32.46-j20.75

TABLE II
Parameters of Output Matching Circuit

Impedances (Ω)				Electrical length (degree)			
Z_1	Z_2	Z_3	Z_4	θ_1	θ_2	θ_3	θ_4
40	30	35	20	85	53	35	20

input matching circuit is designed using only MET3 single layer. For the output matching circuit, the signal line circuit (SLC) was used to sequentially combine the output signals derived from the 12 drain pads. In order to reduce the length of the circuit, the SLC was implemented in MET2 layer. The MET3 layer was used for the pad connections at the drain and the final output. The SLC circuit was designed to reduce Z_0 for matching of final impedance Z_{out1} at each branch point. The impedances Z_{out4}, Z_{out3}, Z_{out2}, and Z_{out1} at each branch plane are shown in Table I. The final impedance Z_{out1} is the same as the matching point obtained from the load–pull simulation. The used design parameters of the output matching circuit are shown in Table II. All input–output matching circuits were designed with full electromagnetic (EM) simulation using high-frequency structure simulation (HFSS) of Ansoft. Although the conventional GaN TR was usually attached using a thin Au, the fabricated WLP IMPA was attached to the aluminum heatsink using silver epoxy. The bias was established using external circuits and the size of the fabricated WLP IMPA was 7.5 mm × 5.8 mm × 0.12 mm.

Fig. 3 presents the simulated and measured S-parameters of the proposed WLP *X*-band IMPA. The measurement results show that the small-signal gain is decreased as the matching point moves about 100 MHz then the simulation. The measured gains as a fraction of return loss were 7.5 dB/5.7 dB, 8.7 dB/8.5 dB, and 7.7 dB/13.7 dB at 10.1, 10.2, and 10.3 GHz, respectively.

Fig. 4 shows the measured gain and DE including input–output bias tee insertion losses. The values of saturation output power measured at 10.1, 10.2, and 10.3 GHz were 48.63, 48.54, and 48.33 dBm, with efficiencies of 47.3%, 50.2%, and 49.2%, respectively. The saturation gains were 4.2, 4.3, and 4.43 dB at 10.1, 10.2, and 10.3 GHz, respectively.

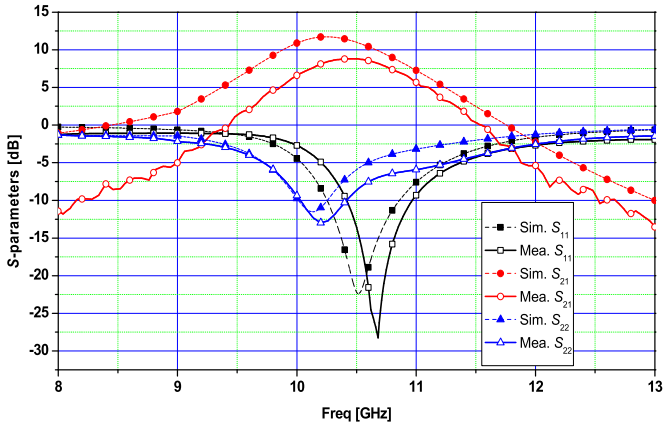


Fig. 3. S-parameter simulation and measurement results (at $V_{DD} = 40$ V, $V_{GS} = -2.75$ V, $I_{DQ} = 219$ mA).

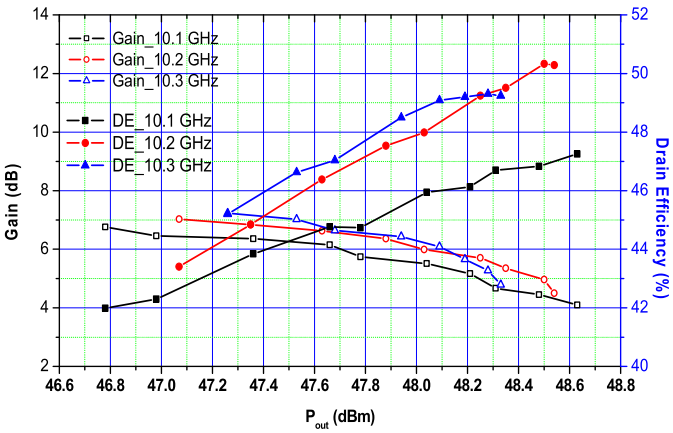


Fig. 4. Measured gain and DE according to the output power at 10.1, 10.2, and 10.3 GHz.

The measured bandwidth exceeding 70 W and 40% DE was 160 MHz (10.09–10.25 GHz).

III. Comparison With Conventional X-Band PAs

To demonstrate the superior performance of the proposed WLP *X*-band IMPA, the measured electrical performances and process technologies were compared with the state-of-the-art measurements. Table III shows the performance comparison of the conventional high power amplifier (HPA) works and the proposed WLP IMPA. The proposed WLP IMPA exhibits similar or higher output power and DE compared with GaN-on-SiC and Quasi-MMIC structures in the *X*-band frequency. In addition, [10] demonstrates a relatively low output power, but it shows the proposed technique is also applicable for WLP IMPA design on 14 GHz.

Fig. 5 depicts DE characteristics of state-of-the-art *X*-band PAs according to output power and operating frequency. The proposed WLP IMPA was compared alongside a few conventional studies to validate the proposed WLP IMPA yielding high output power and efficiency comparable to the silicon interposer technique. In particular, [9] used the same output matching structure, Si integrated passive device (IPD) technology, and measurement conditions. As a measurement result, the proposed WLP IMPA has better characteristics than that in [9]. Therefore, it can be verified that the proposed WLP IMPA can improve the performances by removing the bonding wire. Furthermore, the manufacturing cost was expected to be substantially lower than PAs using SiC or ceramic PCB due to the silicon substrate usage.

TABLE III
Performances Comparison With Previous Works

Ref.	Freq. [GHz]	Output power [W]	DE [%]	Fabrication process	Size [mm^2]
[1]	9.2	74.13	45.1*	GaN-on-SiC	3.5×3.8
[2]	10	13.4	25.7*	GaN-on-SiC	4.5×3
[5]	10	31.5	63*	Quasi-MMIC (3 kinds ceramic PCBs: ε_r= 10, 90 and 38)	5.4×3.8
[6]	X -band	60.3	51.57*	Quasi-MMIC (2 kinds ceramic PCBs: ε_r= 38 and 10)	7×7.7
[7]	9.4	66	52.8*	Quasi-MMIC (ceramic PCB: ε_r= 36)	9.6×8.6
[9]	8.5	70.8	45.5	Quasi-MMIC (Si IPD)	8.4×5.2
[10]	14	1	42.9	WLP IMPA	1.9×3.7
[11]	8	37.7	53	WLP IMPA	1.6×2.8
This work	**10.2**	**71.45**	**50.29**	**WLP IMPA**	**7.5×5.8**

*calculated value, IPD: integrated passive device

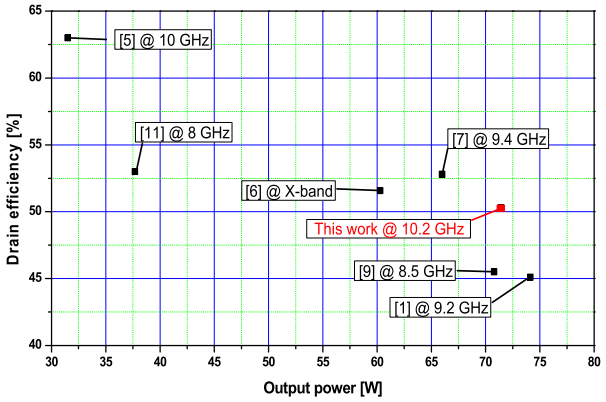


Fig. 5. DE characteristics of the state-of-the-art *X*-band PAs according to output power and operating frequency.

IV. Conclusion

In this letter, the WLP *X*-band IMPA using silicon interposer technology is proposed. It comprises an embedded commercial GaN HEMT TR mounted in the silicon wafer and matching networks using the silicon interposer technology. The proposed WLP *X*-band IMPA enhanced the output power and efficiency compared with the conventional quasi-MMIC HPAs due to the removal of bonding wires between matching networks and TR. From a system design perspective, it provides high levels of integration and design freedom because in addition to PA other IC circuits can be embedded using the WLP technology. Moreover, the manufacturing cost can be reduced compared with the *X*-band PA carrying SiC or ceramic substrate using the silicon substrate. The state-of-the-art comparison reveals superior output and drains efficiency of the proposed WLP IMPA compared with other *X*-band PAs. Therefore, the proposed structure is suitable for high-power and high-efficiency PA design at *X*-band as well as low frequency.

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