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Reconfigurable Negative Group Delay Circuit with a Low Insertion Loss Using a Coupled Line

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Abstract

This paper presents a design of a transmissive-type, low insertion loss (IL) negative group delay (NGD) circuit with a reconfigurable NGD. The proposed circuit consists of a series transmission lines (TLs) and shunt short-circuited coupled lines where an isolation port is terminated with a parasitic compensated PIN diode. Analytical design equations are derived to obtain the circuit parameters for the predefined NGD and IL. The low IL can be achieved because of the very high characteristic impedance of the short-circuited coupled lines. The TL terminated with a PIN diode is used to achieve the constant center frequency of reconfigurable NGD circuit. For experimental validation, the NGD circuit is designed and fabricated at a center frequency (f_0) of 2.14 GHz. In the measurement, the NGD varies from −0.5 ns to −2 ns with an IL variation of 2.08 to 3.60 dB at f_0 = 2.14 GHz. The NGD bandwidth (bandwidth of GD less than 0 ns) varies from 90 MHz to 50 MHz. The minimum input/output return losses are higher than 10 dB for the overall tuning range.

Key Words: Coupled Line, Low Insertion Loss, Parasitic Compensated PIN Diode, Reconfigurable Negative Group Delay Circuit.

I. INTRODUCTION

The propagation of electromagnetic waves in dispersive media can be characterized by abnormal phases, group delays, and velocities [1, 2]. In a specific frequency band of an anomalous dispersion, the abnormal group delay velocity is observed to be greater than the speed of light in vacuum or even a negative value [3]; this occurrence is defined as superluminal group velocity or negative group delay (NGD). NGD and NGD velocity are associated with each other. That is, the peak of the pulse envelope emerges from the medium at an instant before the peak of the pulse enters the medium.

Such a seemingly anti-causal phenomenon does not violate the principle of causality as the turn-on and turn-off points of the wave packet propagate with a positive delay in agreement with the causality requirements [4]. Theoretical and experimental investigations in the fields of electronic and microwave engineering have confirmed that different active and passive circuit topologies can generate the NGD phenomenon [5–13]. Moreover, researchers have been trying to find applications for NGD or the superluminal effect in various electronic circuits including enhancing the efficiency of a feed-forward amplifier, shortening delay lines, realizing non-Foster reactive elements, and minimizing beam-squint problems in series-fed antenna array systems [13–17].

As NGD can be generated within a limited frequency band under a signal attenuation condition, various RLC resonator-based NGD circuits have been presented in the literature [6–9]. However, these conventional circuits have a fixed NGD. Efforts have been made to design a reflective-type reconfigurable NGD circuit using a 3-dB hybrid and RLC resonator [18–20], which

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suffers from high insertion loss (IL). The IL in these works can be improved by increasing the characteristic impedance of the resonators and decreasing the value of R for the required NGD. However, the improvement of IL is limited because practically, implementing a high characteristic impedance (>130 Ω) microstrip line in PCB technology is difficult. A transmissive-type reconfigurable NGD circuit based on an open radial stub patch and a short-circuited stub with PIN diode is presented in [20]. To make a symmetrical structure, two units of NGD circuits are cascaded back to back, which increasing overall size and IL.

In this paper, a transmissive-type reconfigurable NGD circuit with low IL is demonstrated using a short-circuited coupled line and a PIN diode. Analytical design equations are derived to obtain the predefined NGD and IL.

II. Analytical Analysis

Fig. 1 shows the proposed structure of the reconfigurable NGD circuit, which consists of series transmission lines (TLs) and a shunt short-circuited coupled line where the isolation port is terminated with a variable resistor R. The characteristic impedance and electrical length of the series TLs are denoted as Z_0 and $\theta_0/2$, respectively. The even- and odd-mode impedances of the coupled line are represented as Z_{0e} and Z_{0o}, respectively. Z_{0e} and Z_{0o} are expressed in terms of the characteristic impedance Z_c and the coupling coefficient C of the short-circuited coupled line as (1).

$$Z_{0e} = \frac{Z_c C}{1-C} \tag{1a}$$

$$Z_{0o} = \frac{Z_c C}{1+C}. \tag{1b}$$

Using circuit theory, the overall S-parameters of the proposed circuit are derived as (2).

$$S_{11} = \frac{Z_0\left(x_1 - jx_2\right)}{x_3 - jx_4} e^{-j\frac{\theta_0 f}{f_0}} \tag{2a}$$

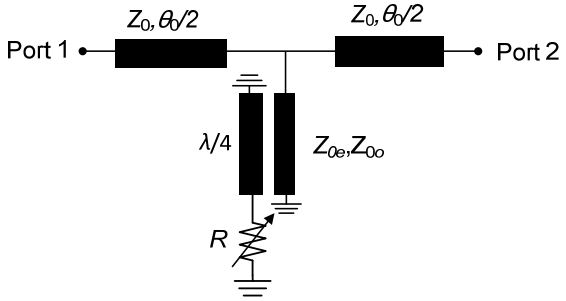


Fig. 1. Proposed reconfigurable NGD circuit with low IL.

$$S_{21} = \frac{2Z_c C\left(Z_c C - jR\cot\frac{\pi f}{2f_0}\right)}{x_3 - jx_4} e^{-j\frac{\theta_0 f}{f_0}}, \tag{2b}$$

where

$$x_1 = R\left(C^2\csc^2\frac{\pi f}{2f_0} - \cot^2\frac{\pi f}{2f_0}\right) \tag{3a}$$

$$x_2 = Z_c C\cot\frac{\pi f}{2f_0} \tag{3b}$$

$$x_3 = C^2\left(2Z_c^2 + Z_0 R\csc^2\frac{\pi f}{2f_0}\right) - Z_0 R\cot^2\frac{\pi f}{2f_0} \tag{3c}$$

$$x_4 = Z_c\left(Z_0 C + 2RC\right)\cot\frac{\pi f}{2f_0} \tag{3d}$$

Moreover, f and f_0 are the operating and design center frequencies, respectively. Using the phase of S_{21}, the group delay (GD) of the proposed circuit can be derived as (4).

$$\tau_{21} = \frac{1}{2\pi}\left\{\frac{\theta_0}{f_0} - \frac{RZ_c C\csc^2\frac{\pi f}{2f_0}}{2f_0\left(Z_c^2C^2 + R^2\cot^2\frac{\pi f}{2f_0}\right)} - \frac{x_3 x_4' - x_3' x_4}{x_3^2 + x_4^2}\right\}, \tag{4}$$

where

$$x_3' = \frac{\pi}{f_0} Z_0 R\left(1-C^2\right)\cot\frac{\pi f}{2f_0}\csc^2\frac{\pi f}{2f_0} \tag{5a}$$

$$x_4' = -\frac{\pi}{2f_0} Z_c C\left(Z_0 + 2R\right)\csc^2\frac{\pi f}{2f_0}. \tag{5b}$$

Finally, the S-parameters and GD at $f=f_0$ of the proposed circuit are simplified as (6).

$$S_{11}\big|_{f=f_0} = \frac{RZ_0}{2Z_c^2 + Z_0 R}, \tag{6a}$$

$$S_{21}\big|_{f=f_0} = \frac{2Z_c^2}{2Z_c^2 + Z_0 R} \tag{6b}$$

$$\tau_{21}\big|_{f=f_0} = \frac{1}{2f_0}\left\{\frac{\theta_0}{\pi} - \frac{R}{2Z_c C} + \frac{Z_c\left(Z_0 + 2R\right)}{2C\left(2Z_c^2 + Z_0 R\right)}\right\} \tag{6c}$$

From (6c), the proposed circuit can generate NGD (GD < 0 ns) if R is given as (7).

$$R > \frac{Z_c Z_0\theta_0 C + Z_c\sqrt{Z_0^2\theta_0^2C^2 + \pi Z_0\left(4\theta_0 CZ_c + \pi Z_0\right)}}{\pi Z_0} \tag{7}$$

To validate the analysis, the calculated circuit parameters of the proposed reconfigurable NGD circuit are shown in Fig. 2

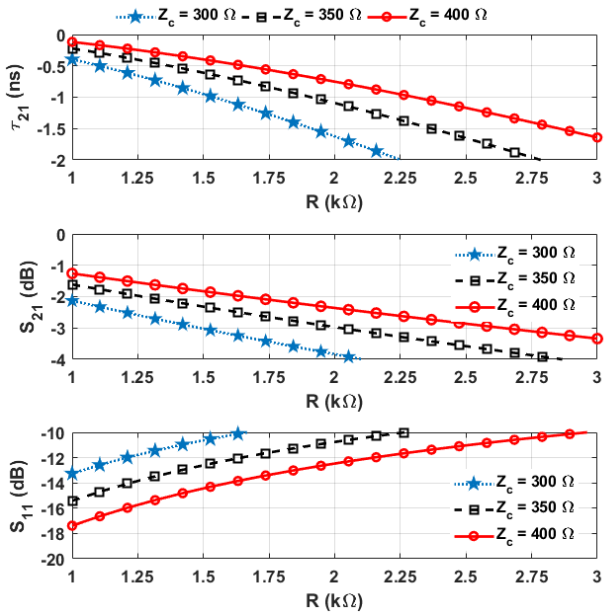


Fig. 2. Calculated group delay, $|S_{21}|$, and $|S_{11}|$ according to Z_c and R with $f_0 = 2.14$ GHz, $C = -16$ dB, and $\theta_0 = 70°$.

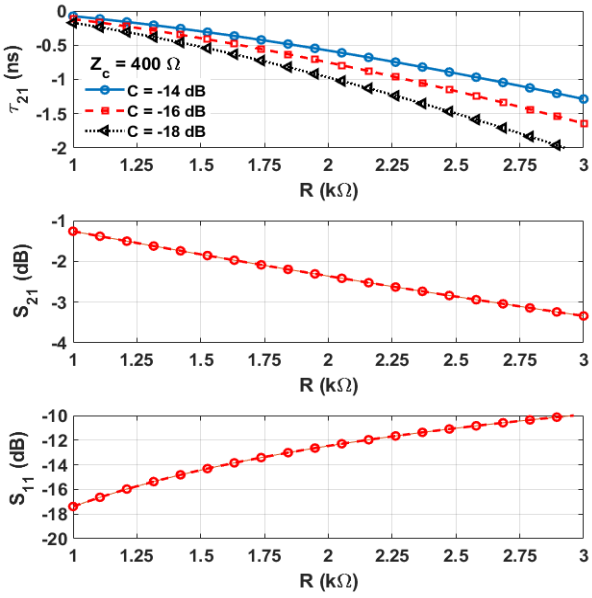


Fig. 3. Calculated group delay, $|S_{21}|$, and $|S_{11}|$ according to C and R with $f_0 = 2.14$ GHz, $Z_c = 400$ Ω, and $\theta_0 = 70°$.

with different Z_c and R. As observed in Fig. 2, the NGD and IL increased as R increases. Moreover, the proposed circuit can provide a low IL with the same NGD tuning range with high Z_c, but the range of R is high for the same NGD. Fig. 3 shows the calculated NGD, IL, and input/output return losses according to the coupling coefficient (C) of the coupled line. As shown in Fig. 3, a higher NGD with the same IL and input/output return losses can be achieved by decreasing C.

Fig. 4 shows the calculated S-parameters and GD response of the proposed circuit. As shown in Fig. 4, the NGD is reconfigured from -0.5 ns to -2 ns at $f_0 = 2.14$ GHz when R is

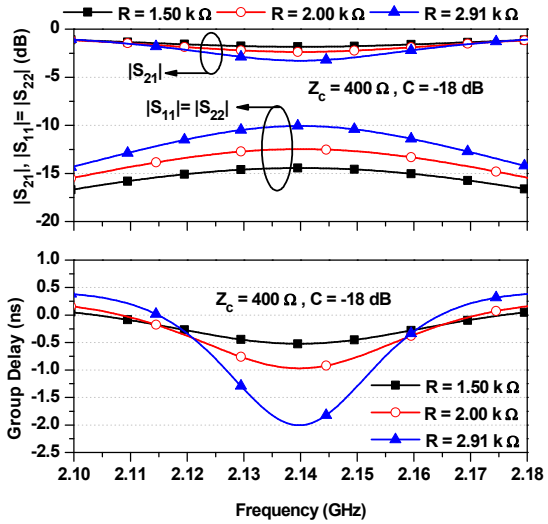


Fig. 4. Calculated S-parameters and GD with $Z_c = 400$ Ω, $C = -18$ dB, and $\theta_0/2 = 35°$.

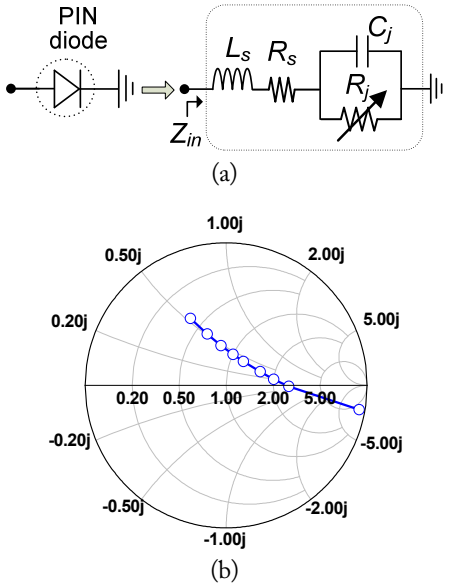


Fig. 5. (a) Equivalent circuit model and (b) measured reflection coefficient of the PIN diode HSMP-4810 at $f_0 = 2.14$ GHz. The parasitic components are $R_s = 3$ Ω, $L_s = 1$ nH, and $C_j = 0.35$ pF.

changed from 1.50 kΩ to 2.91 kΩ. The IL and input/output return losses vary from 1.829 dB to 3.27 dB and 14.43 to 10.6 dB at $f_0 = 2.14$ GHz, respectively.

To implement the proposed reconfigurable NGD circuit, R should be applied with the PIN diode, which functions as a current-controlled variable resistor at microwave frequencies. In this work, the PIN diode HSMP-4810 from Avago was used. Fig. 5(a) shows the equivalent circuit model of the PIN diode. The input impedance of the PIN diode HSMP-4810 is not purely resistance as shown in Fig. 5(b), because of the parasitic components, which degrade the NGD performance of the reconfigurable NGD circuit at f_0.

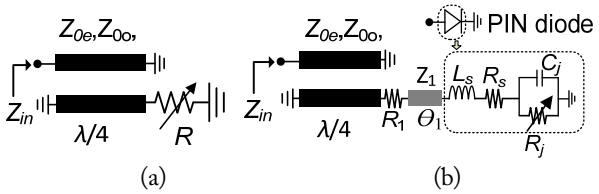


Fig. 6. (a) A short-circuited coupled line terminated with the ideal R and (b) a parasitic compensated PIN diode with $R_s = 3\ \Omega$, $L_s = 1$ nH, and $C_j = 0.35$ pF.

To obtain reconfigurable NGD results consistent with the analytical circuit analysis, the parasitic components of the PIN diode is compensated using TL (Z_1, θ_1) as shown in Fig. 6 [18]. To validate the proposed parasitic compensation method, the input impedances of the short-circuited coupled line with the ideal R and TL terminated with the PIN diode are shown in Fig. 7. As shown in the figures, the imaginary part of the input impedances (Fig. 6) at $f_0 = 2.14$ GHz are maintained at around zero, and reconfigurable real part of the input impedances is the same as the short-circuited couple line terminated with the ideal R.

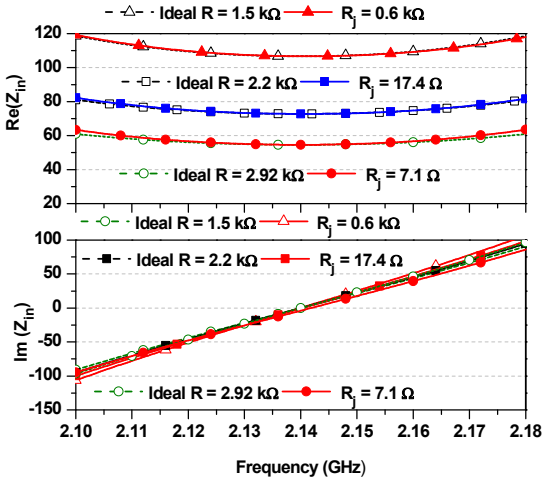


Fig. 7. Input impedance of a short-circuited coupled line terminated with the ideal R and a parasitic compensated PIN diode with $Z_c = 400\ \Omega$, $C = -18$ dB, $R_1 = 1{,}480\ \Omega$, $Z_1 = 120\ \Omega$, and $\theta_1 = 83.5°$

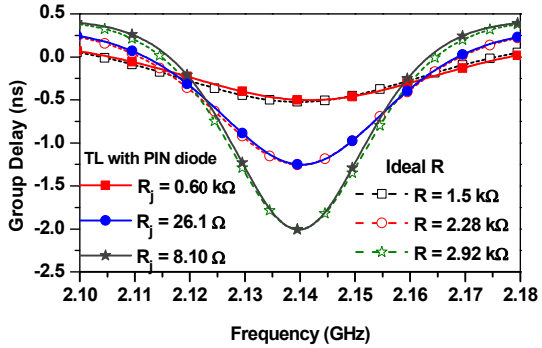


Fig. 8. Group delay with the ideal R and a parasitic compensated PIN diode with $Z_c = 400\ \Omega$, $C = -18$ dB, $R_1 = 1{,}480\ \Omega$, $Z_1 = 120\ \Omega$, $\theta_1 = 83.5°$, $R_s = 3\ \Omega$, $L_s = 1$ nH, and $C_j = 0.35$ pF.

Fig. 8 shows the GD responses of the proposed reconfigurable NGD circuit with the ideal R and parasitic compensated PIN diode. The GD of the parasitic compensated PIN diode is almost the same as the analytical calculated results using (4).

III. Simulation and Measurement

For experimental validation, the proposed circuit is designed, fabricated, and measured at $f_0 = 2.14$ GHz using the substrate RT/duroid 5880 with a dielectric constant of 2.2 and thickness of 0.787 mm. The goals are to achieve the GD variation of −0.5 ns to −2 ns and input/output return losses higher than 10 dB at f_0. Based on the above design specification, the calculated circuit parameters are determined as $Z_c = 400\ \Omega$, $C = -17$ dB, $Z_{0e} = 65.80\ \Omega$, $Z_{0o} = 49.51\ \Omega$, $\theta_0 = 70°$, $Z_0 = 50\ \Omega$, and $R = 1.57$ to 3.14 kΩ. The physical layout with the dimensions and a photograph of the fabricated circuit are shown Fig. 9.

Fig. 10 illustrates the simulated and measured GD and $|S_{21}|$ results. The measurement results agreed well with the simulation results. From the measurement, the GD is reconfigured from −0.49 ns to −2.02 ns with an IL variation of 2.08 to 3.60 dB at $f_0 = 2.14$ GHz when the bias voltage varies from 0.779 V to 0.66 V. The NGD bandwidths (bandwidth of GD < 0 ns) are achieved from 90 MHz to 50 MHz for the overall tuning range of GD. Fig. 11 shows the measured $|S_{11}|$ and $|S_{22}|$, which vary from −14.12 to −10.01 dB for the overall GD range. Table 1 shows the performance comparison of the proposed circuit with the state-of-the-art. As shown in Table 1, the proposed work has an IL of 3.60 dB when the GD is equal to −2 ns. However, the ILs—28.60 dB in [18], 19.50 dB in [19], and 4.50 dB in [20]—are higher than that of the proposed work for the same GD (e.g., GD = −2 ns). Therefore, the proposed

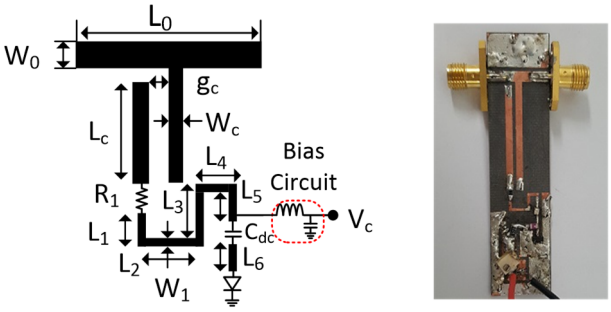
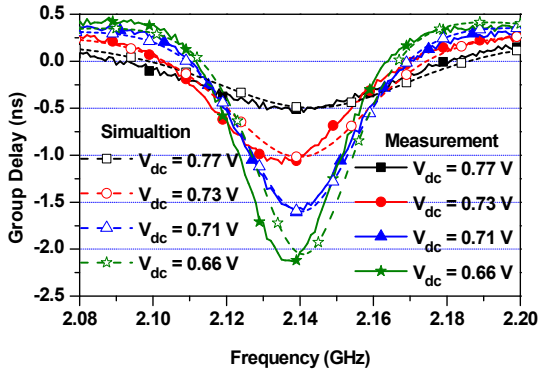
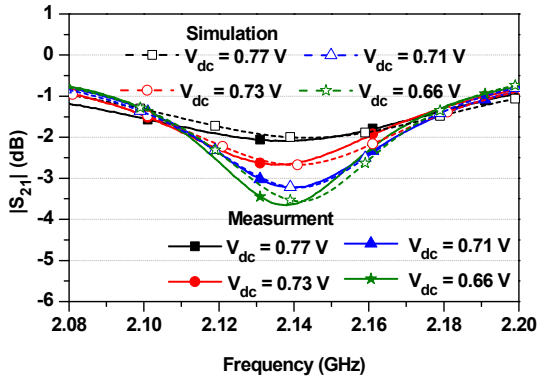


Fig. 9. (a) Physical layout and (b) photograph of the fabricated reconfigurable NGD circuit. Physical dimensions: $R_1 = 1.5$ kΩ, $C_{dc} = 18$ pF, $L_0 = 16$, $W_0 = 2.4$, $W_c = 1.8$, $g_c = 0.8$, $L_c = 25$, $W_1 = 0.5$, $L_1 = 3.7$, $L_2 = 5.6$, $L_3 = 3.70$, $L_4 = 3$, $L_5 = 4.4$, and $L_6 = 6$ (unit: mm).



(a)



(b)

Fig. 10. Simulated and measured results of the proposed reconfigurable NGD circuit: (a) group delay and (b) $|S_{21}|$.

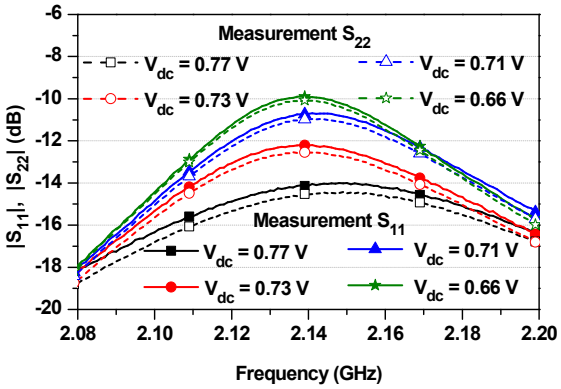


Fig. 11. Measured $|S_{11}|$ and $|S_{22}|$.

circuit provides a reconfigurable NGD with a low IL compared with the state-of-the-art [18–20].

IV. Conclusion

This paper demonstrates a reconfigurable NGD circuit with a low IL using a coupled line and a parasitic compensated PIN diode. Both the analytical and experimental results validate the proposed circuit. To obtain consistent results with the analytical analysis, the parasitic components are compensated by using the TL terminated PIN diode. The measurement results agreed well with the analytically predicated and simulation results. The proposed circuit is expected to apply in various applications of microwave communication systems.

Table 1. Performances comparison of proposed NGD circuit with state-of-the-arts

Ref.	f_0 (GHz)	GD (ns)	IL (dB)	NGD BW (MHz)	A
[6]	0.45	−1.52	14.5*	103	N
[7]	2.14	−1.76	16	60	N
[8]	1.96	−6.5	21.20	200	N
[9]	1.96	−5.90	39.25	140	N
[18]	2.14	−2 to −20	28.6–46.1	80–40	Y
[19]	2.14	−2 to −20	19.5–41.5	80–40	Y
[20]	1.73	−2 to −10	4.50–9.30	40–30	Y
This work	2.14	−0.5 to −2.02	2.08–3.60	90–50	Y

A = NGD tenability, NGD BW = bandwidth of GD < 0 ns, * = active NGD circuit.

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References

[1] L. Brillouin, *Wave Propagation and Group Velocity*. New York, NY: Academic Press, 1960.

[2] E. L. Bolda, R. Y. Chiao, and J. C. Garrison, "Two theorems for the group velocity in dispersive media," *Physical Review A*, vol. 48, no. 5, pp. 3890-3894, 1993.

[3] A. H. Dorrah, L. Kayili, and M. Mojahedi, "Superluminal propagation and information transfer: a statistical approach in the microwave domain," *Physics Letters A*, vol. 378, no. 44, pp. 3218-3224, 2014.

[4] C. M. Hymel, M. H. Skolnick, R. A. Stubbers, and M. E. Brandt, "Temporally advanced signal detection: a review of the technology and potential applications," *IEEE Circuits and Systems Magazine*, vol. 11, no. 3, pp. 10-25, 2011.

[5] B. Ravelo, A. Perennec, M. Le Roy, and Y. G. Boucher, "Active microwave circuit with negative group delay," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 12, pp. 861-863, 2007.

[6] M. Kandic and G. E. Bridges, "Asymptotic limits of negative group delay in active resonator-based distributed

circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 8, pp. 1727-1735, 2011.

[7] H. Choi, K. Song, C. D. Kim, and Y. Jeong, "Synthesis of negative group delay time circuit," in *Proceedings of 2008 Asia-Pacific Microwave Conference*, Macau, China, 2008, pp. 1-4.

[8] G. Chaudhary, Y. Jeong, and J. Lim, "Microstrip line negative group delay filters for microwave circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 2, pp. 234-243, 2014.

[9] J. Park, G. Chaudhary, J. Jeong, and Y. Jeong, "Microwave negative group delay circuit: filter synthesis approach," *Journal of Electromagnetic Engineering and Science*, vol. 16, no. 1, pp. 7-12, 2016.

[10] G. Chaudhary and Y. Jeong, "Distributed transmission line negative group delay circuit with improved signal attenuation," *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 1, pp. 20-22, 2013.

[11] G. Chaudhary, Y. Jeong, and J. Lim, "Miniaturized dual-band negative group delay circuit using dual-plane defected structures," *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 8, pp. 521-523, 2014.

[12] G. Chaudhary, J. Jeong, P. Kim, and Y. Jeong, "Negative group delay circuit with improved signal attenuation and multiple pole characteristics," *Journal of Electromagnetic Engineering and Science*, vol. 15, no. 2, pp. 76-81, 2015.

[13] G. Chaudhary and Y. Jeong, "A design of compact wideband negative group delay network using cross coupling," *Microwave and Optical Technology Letters*, vol. 56, no. 11, pp. 2495-2497, 2014.

[14] H. Choi, Y. Jeong, C. D. Kim, and J. S. Kenney, "Efficiency enhancement of feedforward amplifiers by employing a negative group-delay circuit," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 5, pp. 1116-1125, 2010.

[15] H. Noto, K. Yamauchi, M. Nakayama, and Y. Isota, "Negative group delay circuit for feed-forward amplifier," in *Proceedings of 2007 IEEE/MTT-S International Microwave Symposium*, Honolulu, HI, 2007, pp. 1103-1106.

[16] H. Mirzaei and G. V. Eleftheriades, "Realizing non-Foster reactive elements using negative-group-delay networks," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 12, pp. 4322-4332, 2013.

[17] H. Mirzaei and G. V. Eleftheriades, "Arbitrary-angle squint-free beamforming in series-fed antenna arrays using non-Foster elements synthesized by negative-group-delay networks," *IEEE Transactions on Antennas and Propagation*, vol. 63, no. 5, pp. 1997-2010, 2015.

[18] J. Jeong, S. Park, G. Chaudhary, and Y. Jeong, "Design of tunable negative group delay circuit for communication systems," in *Proceedings of 2012 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, Singapore, 2012, pp. 59-61.

[19] J. Jeong, K. Mok, J. Kim, Y. Jeong, and J. Lim, "Negative group delay circuit with independently tunable center frequency and group delay," in *Proceedings of 2013 Asia-Pacific Microwave Conference Proceedings (APMC)*, Seoul, Korea, 2013, pp. 197-199.

[20] G. Liu and J. Xu, "Reconfigurable negative group delay circuit with low signal attenuation," *Microwave and Optical Technology Letters*, vol. 59, no. 10, pp. 2538-2542, 2017.

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