# Frequency Selective Impedance Transformer With High-Impedance Transforming Ratio and Extremely High/Low Termination Impedances

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***Abstract*— This article presents a novel frequency selective impedance transformer (ITs) with high transforming ratio and extremely low/high termination impedances (1 Ω or 2 Ω and several kΩ). The design equations are derived for both low and high termination impedances and effectively demonstrated. For transforming extremely low or high termination impedances, the characteristic impedances of open or short-circuited transmission line (TL) load can be very high or low, which cannot be fabricated with normal substrates because of the very narrow or broad width of TL. To solve the practical realization problem, the parallel-coupled lines can be adopted instated of TL. For the validation, two types of ITs are designed and measured at a center frequency ($f_0$) of 3.5 GHz with impedance transforming ratios of $r = 25$ and $r = 71.43$ (2 Ω : 50 Ω and 35 Ω : 2500 Ω). The measurement results are consistent with simulation and theoretical predicated results. For achieving frequency selectivity, transmission zeros are generated very close to passband with stop-band suppression of higher than 40 dB.**

***Index Terms*— Coupled line, frequency selectivity, high impedance transforming ratio, impedance transformer.**

## I. Introduction

FREQUENCY selective impedance transformers (ITs) with a high impedance transforming ratio ($r$) of low/high termination impedances are important for various applications in modern wireless communication systems [1]–[5]. ITs with very low termination impedance, such as 1 or 2 Ω, can be used for high-power amplifier design [5], [6]. On the other hand, ITs with very high termination impedances (> 100 Ω) or extremely high impedances (such as several kΩ) have great potential applications in wireless power transfer and water antennas or underwater communications [7], [8] for perfect matching. These multi-functional ITs can improve electrical performance, reduce circuit size, and reduce system complexity.

A quarter-wave ($\lambda/4$) IT is simple and easy to use with limited $r$ and out-of-band suppression. The ITs with very low/high termination impedances have a drawback regarding fabrication with typical transmission lines (TLs). Recently, many researched works have proposed various structures and techniques to overcome such limitations. In [9], a wideband IT was designed by using a single coupled TL interconnected with a stepped-impedance TL. The passband fractional bandwidth (FBW) of 20 dB return loss was beyond 100%, with $r = 2$ (50 Ω: 100 Ω). ITs with parallel-coupled lines and shunt open stubs were designed for a wide passband and high selectivity [10], [11]. The ITs were designed for $r = 2$ (50 Ω: 25 Ω) with FBWs of 60 and 33.38%. Similarly, another IT was designed by using two parallel coupled lines at the input and output ports along with a multi-section TL [12]. A wide passband was obtained, with $r = 2$. In [13], an IT with $r = 5$ was designed by modifying the position of the shunt TL. Frequency selectivity was obtained with the FBW of 13.5%. For more flexibility, a $\lambda/2$ stepped impedance resonator (SIR) BPF with unequal real-to-real termination impedance was analyzed with any number of stages [14]. This BPF was designed with unequal termination impedances and controllable spurious frequency, but the passband bandwidth and $r$ are very limited. In [15], an IT with two cascading parallel coupled lines was analyzed with different passband responses. This IT can provide a bandpass response with a high $r$, but the bandwidth of the passband narrows as $r$ increases. Moreover, the IT is only applicable to low termination impedance. On the other hand, an IT with bandpass filtering performance was designed by using two parallel coupled lines and a short-circuited stub [16]. This IT provides high selectivity ($|S_{11}| = -18$ dB) and FBW of 19% for $r = 10$ (50 Ω : 500 Ω). However, it is only suitable for high termination impedance. For more flexible design, high $r$ ITs with both low and high termination impedances are presented in [17], [18]. In [17], the IT was designed using multi-stub TLs and a reactive element. Although this IT can terminate with both low and high impedance, the out-of-band suppression and return loss bandwidth are poor. Similarly, an IT with filtering response was designed in [18] for both low and high termination impedances (5 Ω : 520 Ω, 5 Ω : 475 Ω, and

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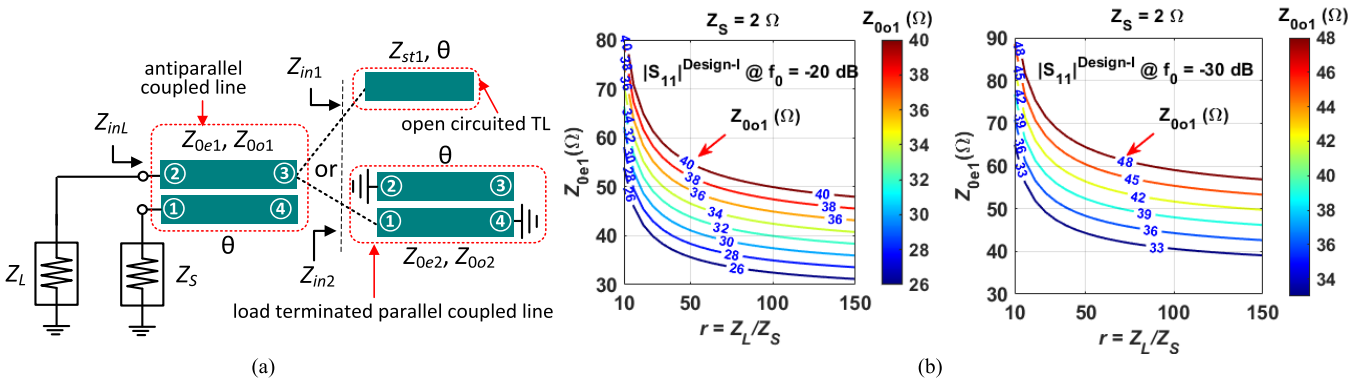



Fig. 1. (a) Proposed structure of design-I frequency-selective impedance transformer for low termination impedance and its variations, and (b) calculated $Z_{0e1}$ according to $r$ and $Z_{0o1}$. Colorbar represents $Z_{0o1}$.

10 Ω : 200 Ω). This IT was designed by using two $\pi$-tapped feeds at the input and output ports, and a parallel-coupled line or inductive coupling.

Despite significant research, IT with extremely low/high termination impedances and ratios are difficult to design. Only a few studies have been done with both low and high termination impedances [17], [18]. Furthermore, none of them have shown an IT with termination impedances of 1 Ω or 2 Ω and several kΩ. It is very challenging to design ITs with high-frequency selective characteristics and high $r$ at very low/high termination impedances (1 Ω, 2 Ω, and several kΩ) simultaneously, and with a compact circuit size.

In this research, frequency selective ITs with high $r$ including extremely low/high termination impedances (1 Ω, 2 Ω, and several kΩ) which are compact and simple structures; are designed and evaluated. The proposed ITs provide two transmission poles in the passband with controllable return loss at the center frequency ($f_0$). Moreover, two transmission zeros (TZs) close to the passband provide a high selectivity characteristic. Another three TZs in the stopband also provide a wide out-of-band suppression. Thus, the proposed ITs are more flexible and can be designed for practically any termination impedances.

## II. Design Theory

### *A. Design-I: Proposed Frequency Selective Impedance Transformer With Low Termination Impedance*

Fig. 1(a) shows the proposed structure of design-I frequency-selective IT, where the source and load impedances are terminated with $Z_S$ and $Z_L$, respectively. The proposed IT can transform from very low $Z_S$ (1 Ω) to another termination impedance $Z_L$ (> hundreds of Ω). The proposed design-I IT consists of an antiparallel coupled line that terminates with an open-circuited TL or parallel-coupled line. The even- and odd-mode impedances of the antiparallel coupled line are represented by $Z_{0e1}$ and $Z_{0o1}$, respectively, whereas electrical length is denoted with $\theta$. Similarly, characteristics impedance and electrical length of open-circuited TL are given as $Z_{st1}$ and $\theta$, respectively. The even- and odd-mode impedances and electrical length of loading parallel coupled line are denoted by $Z_{0e2}$, $Z_{0o2}$, and $\theta$, respectively. Assuming impedance transformation ratio $r = Z_L/Z_S$, providing $Z_L > Z_S$, the $S$-parameters of the proposed circuit can be found as (1) by using *ABCD*-to $S$-parameter conversion relation [19]. The detailed derivation of *ABCD*-parameters is shown in appendix A1.

$$S_{11}|^{\text{Design-I}} = \frac{A_1 r Z_S + B_1 - C_1 r Z_S^2 - D_1 Z_S}{A_1 r Z_S + B_1 + C_1 r Z_S^2 + D_1 Z_S} \tag{1a}$$

$$S_{21}|^{\text{Design-I}} = \frac{2Z_S\sqrt{r}}{A_1 r Z_S + B_1 + C_1 r Z_S^2 + D_1 Z_S} \tag{1b}$$

where $A_1$, $B_1$, $C_1$, and $D_1$ are given in (A5) in appendix. When electrical length $\theta = 90^{\text{o}}$ at center frequency $f_0$, the magnitude of $S_{11}$ is further simplified as (2).

$$|S_{11}|^{\text{Design-I}}_{f=f_0} = \frac{r\left(Z_{0e1} - Z_{0o1}\right)^2 - \left(Z_{0e1} + Z_{0o1}\right)^2}{\left(Z_{0e1} - Z_{0o1}\right)^2 r + \left(Z_{0e1} + Z_{0o1}\right)^2} \tag{2}$$

By solving (2), the value of $Z_{0e1}$ of the antiparallel coupled line in terms of $Z_{0o1}$ and specified $|S_{11}|$ at $f_0$ can be derived as (3)

$$Z_{0e1} = \frac{Z_{0o1}\left(x_1 + x_2 + 2\sqrt{x_2 x_1}\right)}{2\left(x_1 - x_2\right)}, \tag{3}$$

where

$$x_1 = r\left(1 - |S_{11}|^{\text{Design-I}}_{f_0}\right),\ x_2 = 1 + |S_{11}|^{\text{Design-I}}_{f_0} \tag{4}$$

As shown in (3), the $Z_{0o1}$ and $|S_{11}|$ at $f_0$ should be selected freely by the designer. Once the values of $Z_{0o1}$,$r$, and $|S_{11}|$ at $f_0$ are specified, $Z_{0e1}$ can be calculated by using (3). After obtaining even- and odd impedances ($Z_{0e1}$ and $Z_{0o1}$) of antiparallel coupled line, the $Z_{st1}$ of the open-circuited TL can be determined as (5) by equating the imaginary part of (1a) to zero at $\theta = 90^{\text{o}}$.

$$Z_{st1} = \frac{\left(Z_{0e1} + Z_{0o1}\right)\left(Z_{0e1}Z_{0o1} - rZ_L^2\right)}{2rZ_L^2} \tag{5}$$

Fig. 1(b) shows the calculated $Z_{0e1}$ according to $Z_{0o1}$, $r$, and $|S_{11}|$ at $f_0$. In these calculations, $Z_S$ is assumed as 2 Ω and $Z_{0o1}$ is varied from 25 Ω to 40 Ω as shown in color bar. $Z_{0e1}$ has a higher value for smaller $r$ and decreases with increasing $r$.

Fig. 2 shows the calculated circuit parameter of design-I impedance transformer with $Z_S = 2$ Ω and $|S_{11}| = -20$ dB at $f_0$. In these calculations, $Z_{0o1}$ is varied from 40 to 55 Ω

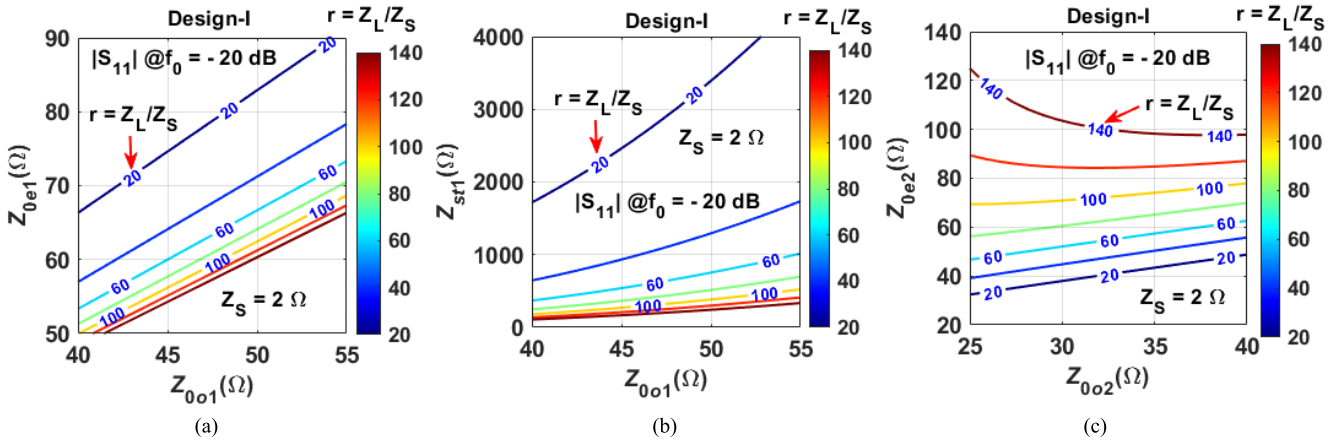



Fig. 2. Calculated circuit parameters of design-I impedance transformer: (a) $Z_{0e1}$ according to $Z_{0o1}$ and $r$, (b) $Z_{st1}$ according to $r$ and $Z_{0o1}$, and (c) $Z_{0e2}$ according to $Z_{0o2}$ and $r$. Colobar represents impedance transforming ratio ($r = Z_L/Z_S$).

whereas $r$ is varied from 20 to 140. $Z_{0e1}$ has a higher value for smaller $r$ and decreases with increasing $r$ as shown in Fig. 2(a). As seen in Fig. 2(b), $Z_{st1}$ is increased with an increase of $Z_{0o1}$ for the same $r$. Besides, $Z_{st1}$ is very high for lower $r$ and is decreased with increment of $r$. The microstrip line with $Z_{st1}$ value from 20 to 130 Ω can be easily fabricated. However, the $Z_{st1}$ value of the open-circuited TL may be very high ($\geq$ 130 Ω) for high $r$ and low $Z_S$, which is difficult for practical realization in microstrip technology because the width of the microstrip line for characteristic impedance higher than 130 Ω is too narrow.

To solve the practical realization problem of $Z_{st1} \geq 130$ Ω, the open-circuited TL can be replaced with a parallel short-circuited coupled line as shown in Fig. 1(a). To find the circuit parameters of the coupled line equivalent to $Z_{st1}$ of open-circuited TL, the input impedance ($Z_{in1}$) of open-circuited TL and an input impedance of ($Z_{in2}$) of the parallel-coupled line are given as (6). The detailed derivation of $Z_{in2}$ is shown in appendix A1.

$$Z_{in1} = -jZ_{st1}\cot\theta \tag{6a}$$

$$Z_{in2} = -j\frac{2Z_{0e2}Z_{0o2}(Z_{0e2}+Z_{0o2})\cot\theta}{(Z_{0e2}-Z_{0o2})^2\csc^2\theta-(Z_{0e2}+Z_{0o2})^2\cot^2\theta} \tag{6b}$$

where $Z_{0e2}$ and $Z_{0o2}$ are even- and odd-impedances of loading coupled line. By equating $Z_{in1} = Z_{in2}$, the relationship between $Z_{0e2}$ and $Z_{st1}$ can be obtained as (7).

$$Z_{0e2} = \frac{Z_{st1}Z_{0o2}}{Z_{0o2}+Z_{st1}-\sqrt{Z_{0o2}^2+4Z_{st1}Z_{0o2}}} \tag{7}$$

As shown in (7), $Z_{0o2}$ of the coupled line should be chosen arbitrarily by the designer whereas $Z_{st1}$ is calculated from (5).

Fig. 2(c) shows the calculated circuit parameters ($Z_{0e2}$, $Z_{0o2}$) of loading coupled line equivalent to $Z_{st1}$ of open-circuited TL. In these calculations, $Z_{0o2}$ is varied from 25 Ω to 40 Ω and $Z_{st1}$ is the same as shown in Fig. 2(b). The value of $Z_{0e2}$ is in the range of 35 to 160 Ω for $r$ = 20 to 140, therefore, proposed IT can be fabricated easily in microstrip line technology.

TABLE I

CALCULATED CIRCUIT PARAMETERS OF DESIGN-I IMPEDANCE TRANSFORMER WITH $|S_{11}| = -20$ dB

| $Z_S$ (Ω) | 1 | 2 | 3 | 5 |
|---|---|---|---|---|
| $Z_L$ (Ω) | 60 | 50 | 300 | 400 |
| $r = Z_L/Z_S$ | 60 | 25 | 100 | 80 |
| $Z_{0o1}$ (Ω) | 25 | 27 | 35 | 50 |
| $Z_{0e1}$ (Ω) | 33.32 | 42.393 | 43.7 | 64.104 |
| $Z_{st1}$ (Ω) | 375.76 | 361.51 | 27.38 | 34.38 |
| $Z_{0o2}$ (Ω) | 45 | 45 | | |
| $Z_{0e2}$ (Ω) | 107.82 | 110.31 | | |

To validate the analytical derivation of the proposed design-I frequency-selective IT, Fig. 3 shows the simulated results with $Z_S$ = 1,2, 3, and 5 Ω ($r$ = 60, 25, 100, and 80), $Z_{0o1}$ = 25, 27, 35, and 50 Ω, and $|S_{11}| = -20$ dB at $f_0$. In these simulations, $Z_{0o2} = 45$ Ω is chosen for the parallel-coupled line that is used for the high characteristic impedance of $Z_{st1}$. The calculated circuit parameters are in Table I using (3), (4), (5), and (7). Since the calculated $Z_{st1}$ = 375.76 Ω and 361.51 Ω are difficult to fabricate in the microstrip line technology with this impedance ratio, the parallel-coupled line was used instead of the open-circuited TL.

As shown in Fig. 3, high-frequency selective characteristics with two poles in the passband are obtained. The return loss at $f_0$ is 20 dB. The bandwidths of the passband differ according to the termination impedance, where a lower $Z_S$ has a narrower passband bandwidth. The 20-dB return loss (RL) fractional bandwidths (FBW) for $Z_S$ = 1,2, 3, and 5 Ω are 3, 5.1, 6.59, and 7.61%, respectively. The transmission zeros (TZs) of the IT with low $r$ are close to the passband and provide high frequency selectivity characteristics. However, the minimum stopband attenuation is around 20 dB. The passband responses of the two ITs with the open-circuited TL and parallel coupled line are identical. The TZs of the IT with the parallel-coupled TL are closer to the passband, which exhibits excellent passband selectivity.

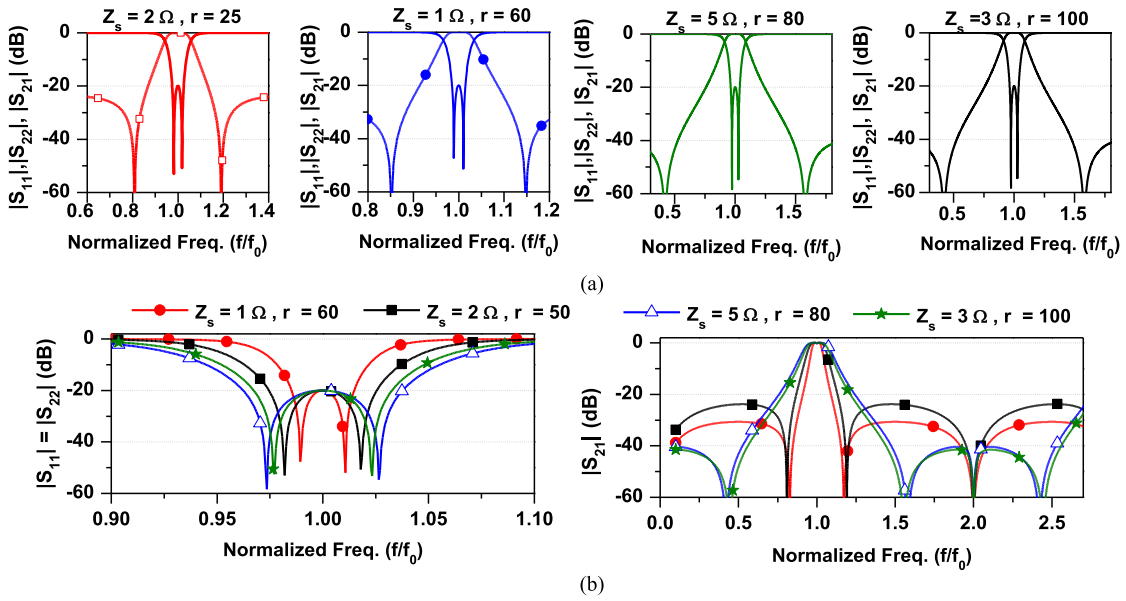



Fig. 3. Simulated $S$-parameter results of design-I frequency-selective impedance transformer: (a) narrowband frequency response with different Zs and $r$, and (b) narrowband frequency characteristic of $|S_{11}|$ and wideband frequency characteristics of $|S_{21}|$.

The proposed IT is designed with an antiparallel coupled line; thus, it can produce two transmission zeros (TZs) close to the passband as shown in Fig. 3. A location of TZ frequency pair can be derived by using the input impedance ($Z_{inL}$) looking at the RF port termination impedance $Z_L$ as shown in Fig. 1(a). The input impedance $Z_{inL}$ of design-I IT looking at RF port termination impedance $Z_L$ can be derived as (8) using *ABCD*-parameter [19].

$$Z_{inL} = \frac{D_1 Z_S + B_1}{C_1 Z_S + A_1} \tag{8}$$

where the value of $A_1$, $B_1$, $C_1$ and $D_1$ are given in (A5). When the real part of (8) is equal to zero, the input RF signal will be shorted, and no RF signal transmission occurs. This phenomenon produces the transmission zeros at stopband. By setting the real part of (8) equal to zero, the TZ frequencies are derived as (9).

$$f_{Z1,2}^{\text{Design-I}} = f_0\,(m + a)\,, m : 1, 3, 5, \cdots \tag{9}$$

where

$$a = \pm\frac{2}{\pi}\sin^{-1}\left(\sqrt{\frac{Z_{0e1} + Z_{0o1}}{2Z_{st1} + Z_{0e1} + Z_{0o1}}}\right). \tag{10}$$

As shown in (9) and (10), the TZ frequencies depend on the value of $Z_{0e1}$, $Z_{0o1}$, and $Z_{st1}$. Fig. 4 shows TZ pair frequencies according to $Z_{0o1}$ and $r$. The values of $Z_{0e2}$ and $Z_{st1}$ are calculated using (3) and (5), respectively. The TZs move closely to $f_0$ as $Z_{0o1}$ increases, thus, high selectivity can be obtained.

Fig. 5 shows the calculated 20-dB RL FBW according to $Z_{0o1}$ and $Z_S$. For these calculations, the value of $Z_{0e1}$ and $Z_{st1}$ are obtained using (3) and (5) assuming $|S_{11}| = -20$ dB at $f_0$, respectively. After obtaining $Z_{st1}$, the value of $Z_{0e2}$ is obtained from (7) assuming the value of $Z_{0o2}$. The FBW is increased as $Z_{0o1}$ decreases and $Z_S$ increases.

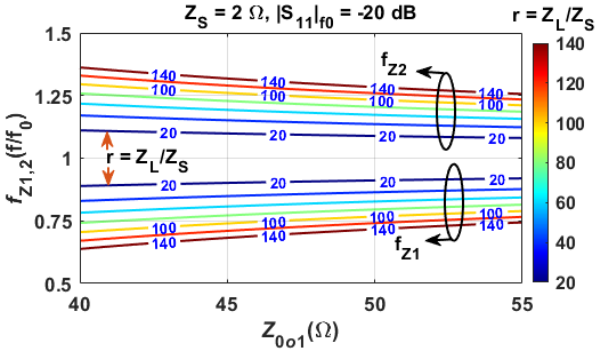



Fig. 4. Transmission zero locations of design-I frequency-selective impedance transformer according to $Z_{0o1}$, $Z_S$, and $r$.

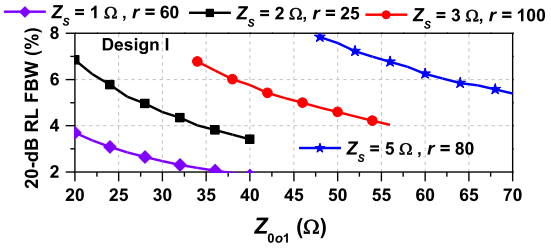



Fig. 5. Calculated fractional bandwidths of 20 dB return loss according to $Z_{0o1}$ and $Z_s$.

The proposed design-I IT provides bandpass response with two poles in the passband, high-frequency selectivity, and wide stopband attenuation characteristics for high $r$ at a very low termination impedance $Z_S$. However, the proposed design-I frequency-selective IT cannot transform $Z_S$ to high impedance (such as several kΩ). Thus, a design II frequency-selective IT is proposed to transform $Z_S$ to an extremely higher termination impedance $Z_L$.

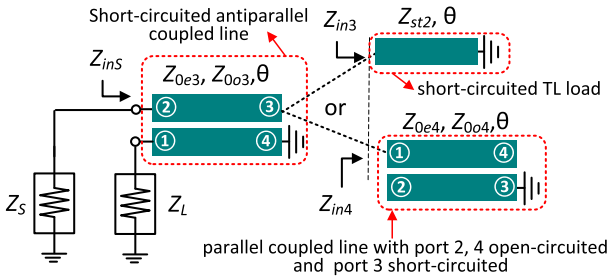



Fig. 6. The proposed structure of the design-II frequency-selective impedance transformer for extremely high termination impedance and its variations.

### *B. Design II: Proposed Frequency Selective Impedance Transformer With Extremely High Termination Impedance*

Fig. 6 shows the proposed structure of design-II the frequency selective IT. The proposed design-II IT can transform source termination impedance $Z_S$ ($\geq$ 10 Ω) to very high termination impedance $Z_L$ (several hundred Ω and kΩ) with a compact circuit size. The proposed circuit consists of a short-circuited antiparallel coupled line terminated with a short-circuited TL or short-circuited parallel-coupled line. The electrical length, even- and odd-mode impedances of the short-circuited antiparallel coupled line are represented with $\theta$, $Z_{0e3}$, and $Z_{0o3}$, respectively. Similarly, the characteristic impedance and electrical length of the short-circuited TL are denoted with $Z_{st2}$ and $\theta$, respectively. The electrical parameters of the loading short-circuited parallel-coupled line are depicted with $Z_{0e4}$, $Z_{0o4}$, and $\theta$.

The *S*-parameters of the proposed design-II IT can be found as (11) by converting *ABCD*-parameters to *S*-parameters. The detailed derivation of the *ABCD*-parameter of design-II frequency-selective IT is shown in appendix A1.

$$S_{11}|^{\text{Design-II}} = \frac{A_2 Z_S + B_2 - C_1 r Z_S^2 - D_2 r Z_S}{A_2 Z_S + B_2 + C_2 r Z_S^2 + D_2 r Z_S} \quad (11a)$$

$$S_{21}|^{\text{Design-II}} = \frac{2Z_S\sqrt{r}}{A_2 Z_S + B_2 + C_2 r Z_S^2 + D_2 r Z_S}, \quad (11b)$$

where values of $A_2$, $B_2$, $C_2$, and $D_2$ are given in (A10). As like design-I in previous section, $|S_{11}|$ at $f_0$ is further simplified as (12) by applying $\theta = 90$.

$$|S_{11}|^{\text{Design-II}}_{f=f_0} = \frac{r\,(Z_{0e3} - Z_{0o3})^2 - (Z_{0e3} + Z_{0o3})^2}{r\,(Z_{0e3} - Z_{0o3})^2 + (Z_{0e3} + Z_{0o3})^2} \quad (12)$$

From (10), a solution of $Z_{0e3} = 1/Y_{0e3}$ of the short-circuited antiparallel coupled line can be derived as (13) for specified $|S_{11}|$ at $f_0$.

$$Z_{0e3} = \frac{Z_{0o3}\,(x_4 - x_3)}{x_3 + x_4 - 2\sqrt{x_3 x_4}} \quad (13)$$

where

$$x_3 = 1 + |S_{11}|^{\text{Design-II}}_{f_0}, \quad x_4 = r\left(1 - |S_{11}|^{\text{Design-II}}_{f_0}\right). \quad (14)$$

As shown in (13), the values of $Z_{0o3}$ and $|S_{11}|$ at $f_0$ can be chosen arbitrarily by the designer. After obtaining $Z_{0e3}$ and $Z_{0o3}$, $Z_{st2} = 1/Y_{st2}$ of the short-circuited TL can be found as (15) by setting the imaginary part of (11a) equal to zero.

$$Z_{st2} = \frac{2Z_{0e3}^2 Z_{0o3}^2}{(Z_{0e3} + Z_{0o3})\left(rZ_S^2 - Z_{0e3}Z_{0o3}\right)} \quad (15)$$

To illustrate the analytical design equations, Fig. 7(a) shows the calculated $Z_{0e3}$ of the short-circuited coupled line according to $Z_{0o3}$, $r$, and $|S_{11}|$ at $f_0$. In these calculations, $Z_{0o3}$ is varied from 60 to 120 Ω. As shown in Fig. 7(a), the $Z_{0e3}$ is decreased if $r$ increases.

Fig. 7(b) shows the calculated $Z_{st2}$ with different $Z_S$, $r$, and $Z_{0o3}$. The value of $Z_{st2}$ is decreased when $r$ is increased. Moreover, the $Z_{st2}$ is slightly increased if $Z_{0o3}$ is chosen high for the same $Z_S$ and $r$. If the calculated $Z_{st2}$ value is low ($\leq$ 15 Ω), $Z_{st2}$ will be difficult to fabricate in microstrip technology because of very wide width of TL.

To solve practical fabrication issues of low $Z_{st2}$ ($\leq$ 15 Ω), the short-circuited TL can be replaced with a short-circuited parallel coupled line as shown in Fig. 6. To find the relationship between the $Z_{st2}$ of short-circuited TL and even- and odd-mode impedances ($Z_{0e4}$, $Z_{0o4}$) of short-circuited parallel coupled line, the input impedance of the short-circuited TL should be the same as the input impedance of the short-circuited parallel coupled line to obtain the same passband performances. The input impedance ($Z_{in3}$) of short- circuited TL and input impedance ($Z_{in4}$) of short-circuited coupled line are given as (16) using (A2), (A4), and (A12).

$$Z_{in3} = jZ_{st2}\tan\theta \quad (16a)$$

$$Z_{in4} = -j\frac{(Z_{0e4} - Z_{0o4})^2 \csc^2\theta - (Z_{0e4} + Z_{0o4})^2 \cot^2\theta}{2\,(Z_{0e4} + Z_{0o4})\cot\theta} \quad (16b)$$

By equating $Z_{in3} = Z_{in4}$, the $Z_{0e4}$ of the short-circuited parallel coupled line can be determined in terms of $Z_{0o3}$ and $Z_{st2}$ as (17).

$$Z_{0e4} = Z_{0o4} + Z_{st2} + \sqrt{Z_{st2}^2 + 4Z_{st2}Z_{0o4}}, \quad (17)$$

As depicted in (17), $Z_{0o4} = 1/Y_{0o4}$ should be selected arbitrarily by designer, whereas $Z_{st2}$ is calculated by using (15).

Fig. 7(c) shows the calculated $Z_{0e4}$ of loading short-circuited line corresponding to $Z_S$, $r$, $Z_{st2}$, and $Z_{0o4}$. In these calculations, $Z_{st2}$ is same as shown in Fig. 7(b) and $Z_{0o4}$ is varied from 40 Ω to 90 Ω. The $Z_{0e4}$ decreases when $Z_S$ and $r$ increase. Moreover, the value of $Z_{0e4}$ is in range of 50 Ω to 180 Ω for corresponding $Z_{0o4}$ = 40 Ω to 90 Ω, and $r$ = 50 to 200, which can be easily fabricated in microstrip technology.

To demonstrate the analytical derivation of the proposed design-II frequency-selective IT, Fig. 8 depicts simulated *S*-parameters of IT with $Z_S$ = 35 Ω and $Z_L$ = 2.5 kΩ ($r$ = 71.43), $Z_S$ = 15 Ω and $Z_L$ = 1.5 kΩ ($r$ = 71.43), $Z_S$ = 15 Ω and $Z_L$ = 0.9 kΩ ($r$ = 112.5), and $|S_{11}|$ = −20 dB at $f_0$. The calculated circuit parameters are given in Table II. Since $Z_{st2}$ = 11.57 Ω is difficult to fabricate in microstrip line technology, the short-circuited TL should be replaced with the short-circuited parallel-coupled line. The calculated $Z_{0e4}$ and $Z_{0o4}$ of short-circuited coupled line, which is equivalent to $Z_{st2}$ are shown in Table II. The proposed IT provides

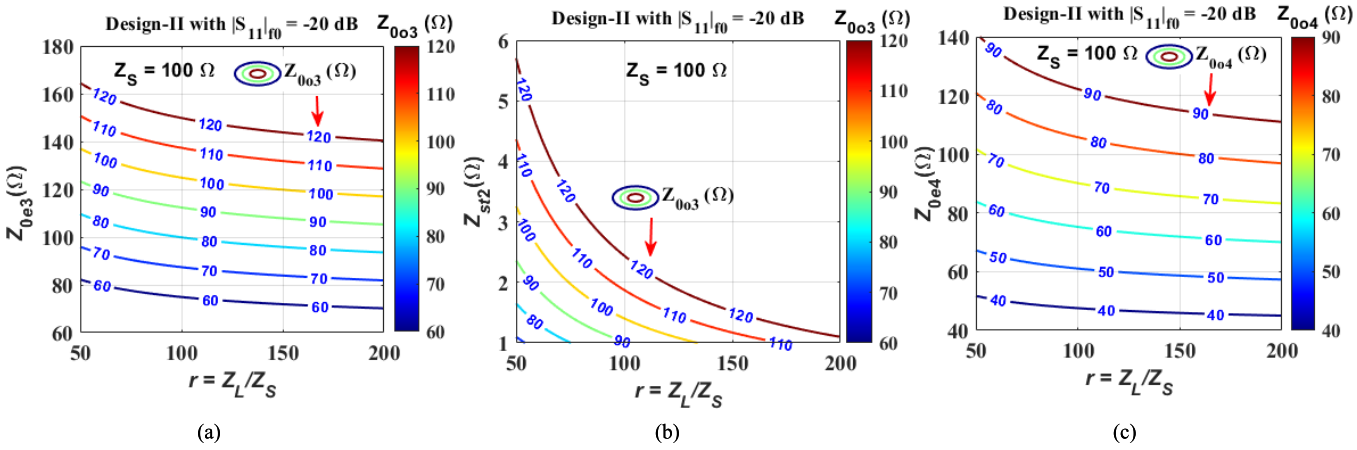



Fig. 7. Calculated circuit parameters of design-II frequency selective impedance transformer :(a) $Z_{0e3}$ according to $r$ and $Z_{0o3}$, (b) $Z_{st2}$ according to $r$ and $Z_{0o3}$, and (c) $Z_{0e4}$ according to $Z_{0o4}$ and $r$. Colorbar represents $Z_{0o3}$ and $Z_{0o4}$.

TABLE II
CALCULATED CIRCUIT PARAMETERS OF DESIGN-II IMPEDANCE TRANSFORMER WITH $|S_{11}| = -20$ dB

| $Z_S$ (Ω) | 35 | 15 | 8 |
|---|---|---|---|
| $Z_L$ (Ω) | 2500 | 1500 | 900 |
| $r = Z_L/Z_S$ | 71.42 | 100 | 112.5 |
| $Z_{0o3}$ (Ω) | 85 | 75 | 60 |
| $Z_{0e3}$ (Ω) | 110.58 | 93.64 | 73.96 |
| $Z_{st2}$ (Ω) | 11.57 | 37.79 | 106.44 |
| $Z_{0o4}$ (Ω) | 45 | | |
| $Z_{0e4}$ (Ω) | 103.64 | | |

high selectivity and a bandpass filtering response with two poles in the passband. The return loss at $f_0$ is 20 dB. The bandwidths of the passband differ according to the termination impedance. Higher $Z_S$ values correspond to narrower passband bandwidths. The 20-dB RL FBWs for $Z_L = 2.5$, 1.5, and 0.9 kΩ are 2.58, 4.78, and 6.36%, respectively.

The TZs of the design-II IT with low $r$ is close to the passband and provide high selectivity characteristics. However, the stopband attenuation is around 25 dB. The passband responses of the design II ITs using the short-circuited TL or short-circuited parallel-coupled line are identical. However, the TZs of the proposed IT with the short-circuited parallel-coupled line is closer to the passband than are those of the IT with short-circuited TL. Similarly, wide, and high stopband attenuation characteristics can be obtained with four TZs.

As like design-I, the TZ pair frequencies of design-II frequency-selective IT can be derived from the input impedance ($Z_{inS}$) seen at $Z_S$ given in (18) using *ABCD*-parameter [19].

$$Z_{inS} = \frac{D_2 Z_L + B_2}{C_2 Z_L + A_2}, \tag{18}$$

where the value of $A_2$, $B_2$, $C_2$, and $D_2$ are given in (A10). When the real part of (18) is equal to zero, the input RF signal will be shorted, and no transmission of the RF signal occurs, which results in the TZ at stopband. Therefore, the TZs pair can be derived as (19) by equating the real part of (18) to zero.

$$f_{Z1,2}^{\text{Design-II}} = f_0 \left(m + a_h\right), m : 1, 3, 5, \cdots \tag{19}$$

where

$$a_h = \pm \frac{2}{\pi} \sin^{-1} \left\{ \sqrt{\frac{Z_{st2}\left(Z_{0e3} + Z_{0o3}\right)}{2Z_{0e3}Z_{0o3} + Z_{st2}\left(Z_{0e3} + Z_{0o3}\right)}} \right\}. \tag{20}$$

Fig. 9 shows calculated the TZ pair frequencies of design-II frequency-selective impedance transformer according to $Z_{0o3}$, $Z_S$, and $r$. The TZs move closer to $f_0$ as $r$ increases and $Z_{0o3}$ decreases. Thus, high selectivity can be obtained at a lower value of $Z_{0o3}$.

Fig. 10 shows the 20-dB RL FBW according to $Z_{0o3}$ and $Z_S$. The calculations are done by fixing $|S_{11}| = -20$ dB at $f_0$. Unlike the proposed design-I IT, the 20-dB RL FBW of the proposed design II IT increases as $Z_{0o3}$ increases and $Z_S$ decreases. Similarly, the 20-dB RL FBW can be slightly improved by increasing $Z_{0o3}$ for the same $r$ and $Z_S$. Therefore, higher $Z_{0o3}$ is preferable for wider 20-dB RL FBW. Based on the discussion and observation presented above, Fig. 11 shows the design flow chart of both proposed ITs.

## III. SIMULATION AND EXPERIMENTAL RESULTS

For experimental verification, prototype of frequency selective IT with termination of $Z_S = 2$ Ω, $Z_L = 50$ Ω ($r = 25$) for design I and $Z_S = 35$ Ω, $Z_L = 2500$ Ω ($r = 71.43$) for design II were designed, simulated, and fabricated at $f_0 = 3.5$ GHz. The calculated circuit parameters are shown in Table I and Table II. The proposed ITs were fabricated on an RT/Duroid 5880 substrate with $\varepsilon_r = 2.2$ and $h = 31$ mils. The simulation is performed using the electromagnetic simulator ANSYS HFSS 2019.

### *A. Design-I: Frequency Selective It With Very Low $Z_S$ Termination Impedances*

Fig. 12(a) and 12(b) shows the layout and a photograph of the fabricated design-I IT, including its offset line. The overall

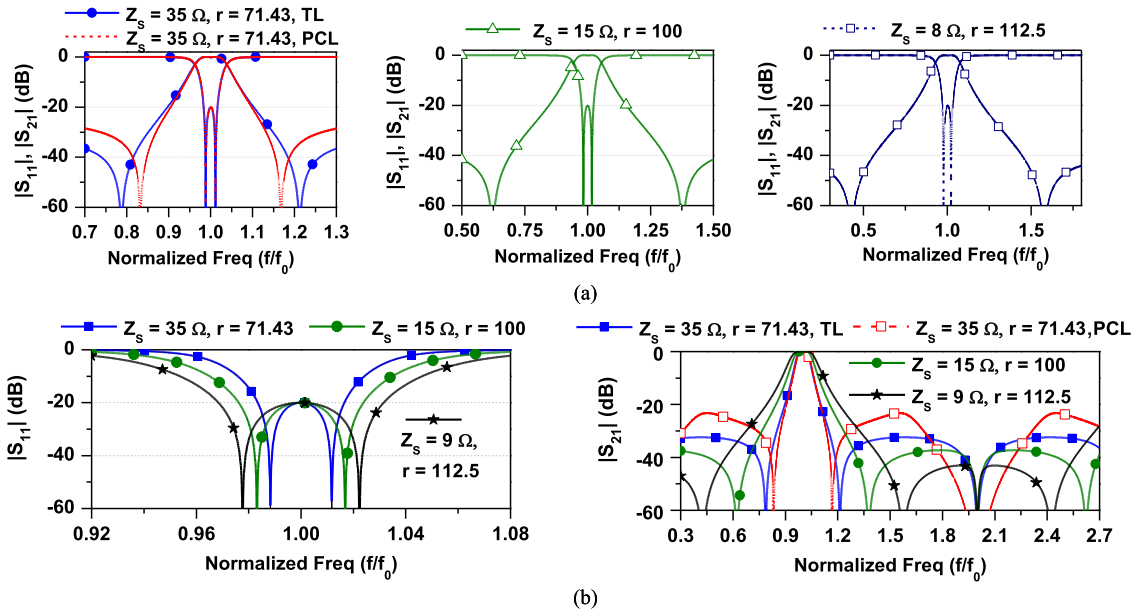



Fig. 8. Simulated S-parameters results of design-II frequency-selective impedance transformer : (a) narrowband frequency response with different Zs and $r$, and (b) narrowband frequency characteristic of $|S_{11}|$ and wideband frequency characteristics of $|S_{21}|$.

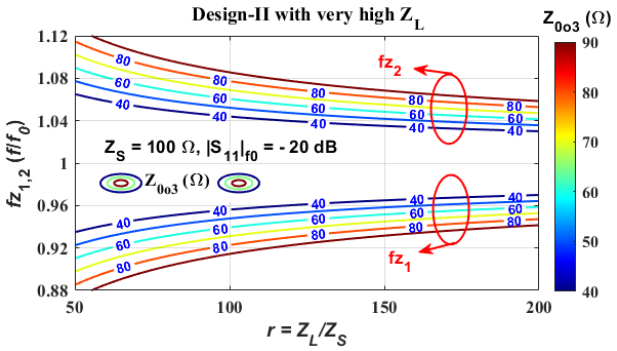



Fig. 9. Calculated transmission zero locations of design-II frequency-selective impedance transformer according to $Z_{0o3}$ and $r$.

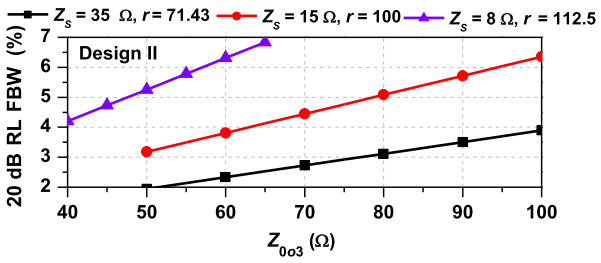



Fig. 10. Calculated 20-dB RL fractional bandwidths of design II frequency-selective IT according to $Z_{0o3}$ and $Z_S$.

circuit size of the fabricated circuit is 17.1 mm × 18.23 mm ($0.199\lambda_g \times 0.213\lambda_g$). The measurement is performed using HP 8720D vector network analyzer. The measurement results are obtained as follows:

a) Offset port 1 of network analyzer using an offset line after calibration.
b) Save the $S$-parameters results as a touchstone file.
c) Import touchstone file into circuit simulator Advanced System Design (ADS).

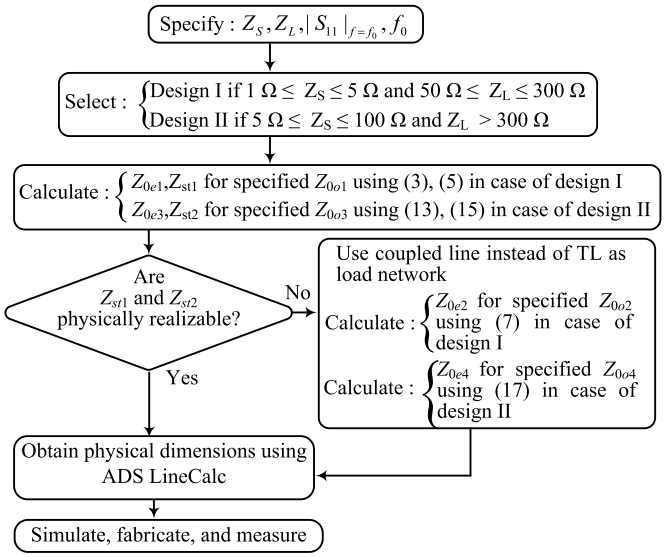
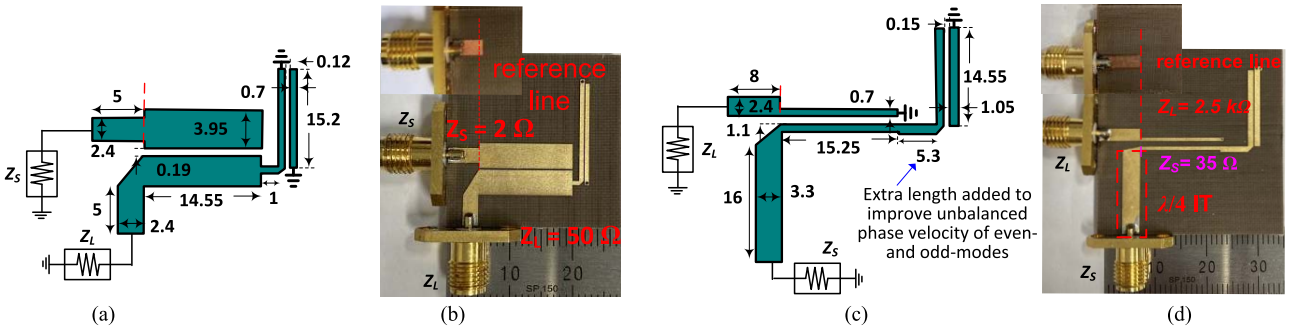



Fig. 11. Circuit parameter calculation flow chart of proposed design-I and design-II frequency-selective impedance transformer.

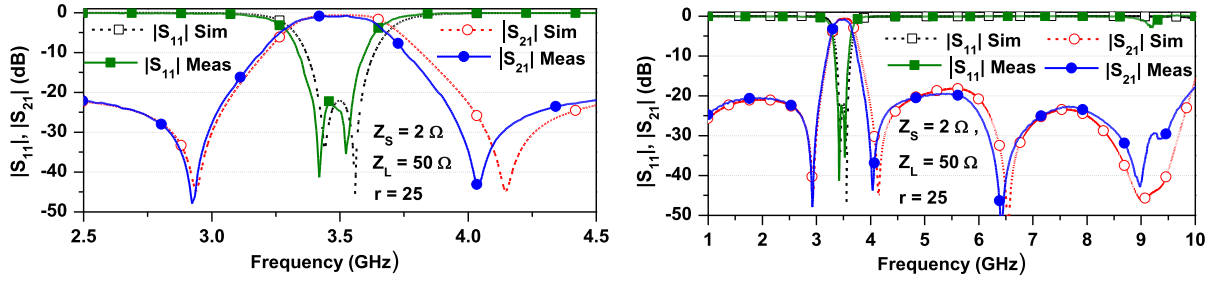
d) Finally, execute the circuit simulator by specifying $Z_S$ and $Z_L$.

Fig. 13 shows the simulated and measured $S$-parameters of the proposed design I IT. The measured results are consistent with the simulated results. The measured $S$-parameters are determined as $|S_{21}| = -0.72$ dB and $|S_{11}| = -24.97$ dB at $f_0 = 3.5$ GHz. The measured bandwidth of a 20-dB RL is extended from 3.438 GHz to 3.615 GHz, with FBW of 5.065%. Moreover, a maximum insertion loss of 0.9 dB is observed within the same passband. The two TZs close to the passband are observed at 2.9 and 4.1 GHz and provide high selectivity. The bandpass response with wide out-of-band suppression is obtained. Lower stopband suppression larger



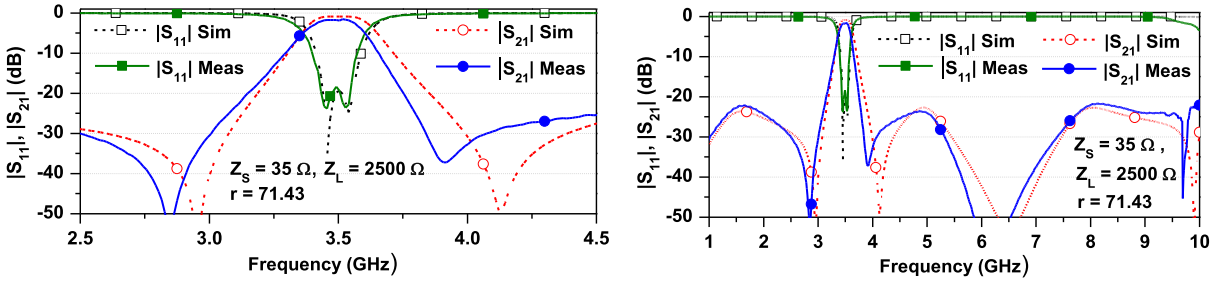

(a) (b) (c) (d)

Fig. 12. Layouts and photographs of the proposed design ITs: (a) EM simulation layout of design-I IT including offset line, and (b) photograph of fabricated PCB of design-I IT, (c) EM simulation layout of design-II IT including offset line, and (d) photograph of fabricated PCB of design-II IT. (Unit: mm).




(a) (b)

Fig. 13. Simulation and measurement results of proposed design-I frequency selective IT: (a) narrowband and (b) wideband frequency responses.




(a) (b)

Fig. 14. Simulation and measurement results of proposed design-II frequency selective IT: (a) narrowband and (b) wideband frequency responses.

than 20 dB is observed from DC to 3.07 GHz. Moreover, higher stopband suppression larger than 17.5 dB is observed from 3.93 GHz to 9.24 GHz.

### *B. Design-II: Frequency Selective IT With Very High $Z_L$ Termination Impedance*

Fig. 12(c) and 12(d) shows the layout and a photograph of the fabricated design-II IT, including its offset line. The overall circuit size of the fabricated circuit is 22.85 mm × 16.75 mm (0.266 $\lambda_g$ × 0.195 $\lambda_g$). An extra TL with a length of 5.3 mm was added to the short-circuited parallel coupled line to improve the unbalanced phase velocities of even- and odd- modes in the parallel coupled microstrip line [20].

Fig. 14 shows the simulated and measured *S*-parameters of the proposed design II IT. The measured results are consistent with the simulated results. The measured S-parameters are summarized as $|S_{21}| = -0.81$ dB and $|S_{11}| = -19.53$ dB at $f_0 = 3.5$ GHz. The measured bandwidth of 20 dB return loss is extended from 3.443 GHz to 3.557 GHz with an FBW of 3.25%. Moreover, the maximum insertion loss of 1 dB is observed within the same passband. The two TZs closed to the passband are measured at 2.92 GHz and 4 GHz and provide high selectivity. Similarly, a bandpass response with wide out-of-band suppression is obtained. Lower stopband suppression larger than 22 dB is measured from 1 GHz to 3.14 GHz, and higher stopband suppression larger than 20 dB from 3.79 to 9.55 GHz are measured.

A comparison of electrical performance with state-of-the-art is summarized in Table III. The previous ITs can transform an impedance with a large $r$, but the termination impedances are not very low/high. The proposed ITs can transform a high $r$ at extremely low/high termination impedances. Moreover, the proposed ITs provide bandpass filtering with high selectivity, higher $r$, and wide stopband suppression, simultaneously.

TABLE III
PERFORMANCES COMPARISON WITH PREVIOUS WORKS

| Ref. | $f_0$ (GHz) | IL (dB) | FBW | $r = Z_L/Z_S$ ($\Omega/\Omega$) | BP filtering | Circuit size |
|---|---|---|---|---|---|---|
| [15] | 2.6 | 0.8 | 8.27 % (18 dB RL) | 10 | Yes | $0.26\lambda_g \times 0.22\lambda_g$ |
| [16] | 3 | 0.87 | 19 % (3dB-IL) | 10 (500/50) | Yes | $0.24\lambda_g \times 0.20\lambda_g$ |
| [17] | 2.4 | 0.72 | 10.4 % (3 dB-IL) | 10 (50/5) | No | $0.09\lambda_g \times 0.50\lambda_g$ |
| [17] | 2.4 | 0.89 | 10 % (3 dB-IL) | 40 (2000/50) | No | $0.41\lambda_g \times 0.51\lambda_g$ |
| [18] | 2.5 | 0.883 | 13% (3 dB-IL) | 20 (200/10) | Yes | $0.20\lambda_g \times 0.09\lambda_g$ |
| [18] | 2 | 1.171 | 10 % (3 dB-IL) | 104 (520/5) | Yes | $0.20\lambda_g \times 0.16\lambda_g$ |
| **This work** | **3.5** | **0.72** | **5.065% (20 dB RL)** | **25 (50/2)** | **Yes** | **$0.19\lambda_g \times 0.21\lambda_g$** |
| | **3.5** | **1** | **3.442% (20 dB RL)** | **71.43 (2500/35)** | | **$0.27\lambda_g \times 0.19\lambda_g$** |

FBW: Fractional bandwidth, RL : Return Loss, IL : Insertion loss

## IV. CONCLUSION

Bandpass filtering and highly selective impedance transformers (ITs) with extremely high transforming ratio (r) and extremely low/high termination impedances are proposed in this work. The design equations of the proposed circuits are derived and verified with simulations and measurements. The open-/short-circuited transmission lines (TLs) with extreme low/high characteristic impedances that cannot be realized with typical microstrip lines are replaced with open/short-circuited parallel coupled lines. Therefore, the proposed ITs are more flexible for high/low termination impedances at high $r$. The two transmission zeros close to the passband provide high selectivity performance and wide stopband characteristics. The proposed ITs are compact and simple to design.

## APPENDIX: A1

Fig. 15 shows the 4-port coupled line with even- and odd-mode impedances of $Z_{0ei}$ and $Z_{0oi}$ and electrical length of $\theta$. The $Z$-parameters of 4-port coupled line is given as (A1).

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} \tag{A1}$$

where

$$Z_{11} = Z_{22} = Z_{33} = Z_{44} = -j\frac{Z_{0ei} + Z_{0oi}}{2}\cot\theta \tag{A2a}$$

$$Z_{12} = Z_{21} = Z_{34} = Z_{43} = -j\frac{Z_{0ei} - Z_{0oi}}{2}\cot\theta \tag{A2b}$$

$$Z_{13} = Z_{31} = Z_{24} = Z_{42} = -j\frac{Z_{0ei} - Z_{0oi}}{2}\csc\theta \tag{A2c}$$

$$Z_{14} = Z_{41} = Z_{23} = Z_{32} = -j\frac{Z_{0ei} + Z_{0oi}}{2}\csc\theta \tag{A2d}$$

Fig. 16 shows the 2-port network when port ③ is connected load ($V_3 = -I_3 Z_{in}$) and port ④ is open circuited ($I_4 = 0$). The new reduced 2-port network $Z$-parameters are derived (A3) as by applying boundary conditions: $V_3 = -I_3 Z_{in1}$ and $I_4 = 0$.

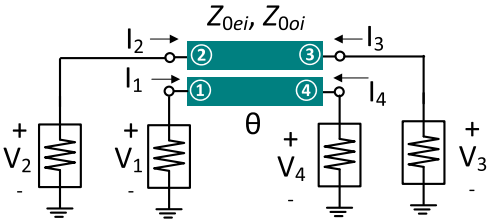



Fig. 15. Structure of 4-port coupled line.

$$Z'_{11} = Z'_{22} = Z_{11} - \frac{Z_{31}Z_{13}}{Z_{in1} + Z_{33}} \tag{A3a}$$

$$Z'_{21} = Z'_{12} = Z_{21} - \frac{Z_{31}Z_{23}}{Z_{in1} + Z_{33}}, \tag{A3b}$$

where

$$Z_{in1} = -jZ_{st1}\cot\theta \tag{A4}$$

By using $Z$-parameter to *ABCD*-parameter relation [20] and equation (A2)-(A4), the overall *ABCD*-parameters of 2-port network shown in Fig 16 are derived as (A5).

$$A_1 = \frac{Z'_{11}}{Z'_{21}} = \frac{\left\{ \begin{array}{l} (Z_{0e1} - Z_{0o1})^2 \csc^2\theta - (Z_{0e1} + Z_{0o1}) \\ (2Z_{st1} + Z_{0e1} + Z_{0o1})\cot^2\theta \end{array} \right\}}{(Z_{0e1} - Z_{0o1})\left(Z_{0e1} + Z_{0o1} - 2Z_{st1}\cot^2\theta\right)} \tag{A5a}$$

$$B_1 = \frac{Z'_{11}Z'_{22}}{Z'_{21}} = j\cot\theta\frac{(Z_{0e1} - Z_{0o1})^2 - (Z_{0e1} + Z_{0o1})^2}{2(Z_{0e1} - Z_{0o1})} \tag{A5b}$$

$$C_1 = \frac{1}{Z'_{21}} = -j\frac{2\cot\theta\,(2Z_{st1} + Z_{0e1} + Z_{0o1})}{(Z_{0e1} - Z_{0o1})\left(Z_{0e1} + Z_{0o1} - 2Z_{st1}\cot^2\theta\right)} \tag{A5c}$$

$$D_1 = \frac{Z'_{22}}{Z'_{21}} = \frac{Z_{0e1} + Z_{0o1}}{Z_{0e1} - Z_{0o1}} \tag{A5d}$$

The $Y$-parameters of the 4-port coupled line shown in Fig. 15 are given as (A6) where $Y_{0ei} = 1/Z_{0ei}$ and $Y_{0oi} = 1/Z_{0oi}$.

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix}, \tag{A6}$$

where

$$Y_{11} = Y_{22} = Y_{33} = Y_{44} = -j\frac{Y_{0oi} + Y_{0ei}}{2}\cot\theta \tag{A7a}$$

$$Y_{12} = Y_{21} = Y_{34} = Y_{43} = -j\frac{Y_{0oi} - Y_{0ei}}{2}\cot\theta \tag{A7b}$$

$$Y_{13} = Y_{31} = Y_{24} = Y_{42} = -j\frac{Y_{0oi} - Y_{0ei}}{2}\csc\theta \tag{A7c}$$

$$Y_{14} = Y_{41} = Y_{23} = Y_{32} = -j\frac{Y_{0oi} + Y_{0ei}}{2}\csc\theta \tag{A7d}$$

When port ③ is connected with load $Z_{in3}$ and port ④ is short-circuited, then 4-port coupled line is reduced to a 2-port circuit as shown in Fig. 17. Therefore, applying boundary

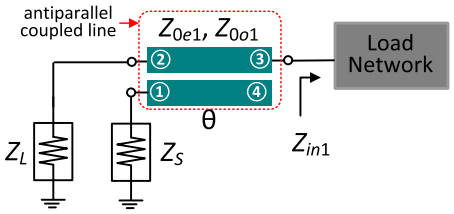



Fig. 16. Structure of reduced 2-port circuit when port 3 is connected with load $Z_{in}$ and port 4 is open-circuited.

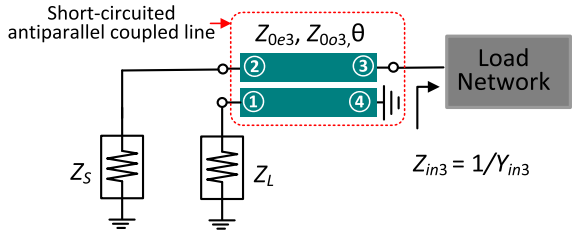



Fig. 17. Structure of reduced 2-port circuit when port 3 is connected with load $Z_{in}3$ and port 4 is short-circuited.

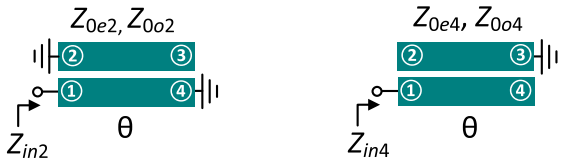



Fig. 18. Structure of reduced 1-port circuit: (a) when port 3 is open-circuited and port 2 and 4 are short-circuited and (b) port 3 is short-circuited and port 2 and 4 are open circuited.

conditions $I_3 = -V_3/Z_{\text{in}3}$ and $V_4 = 0$, the new $Y$-parameters of reduced 2-port are derived as (A8).

$$Y'_{11} = Y'_{22} = Y_{11} - \frac{Y_{31}Y_{13}}{Y_{in3} + Y_{33}} \tag{A8a}$$

$$Y'_{21} = Y'_{12} = Y_{21} - \frac{Y_{31}Y_{23}}{Y_{in3} + Y_{33}}, \tag{A8b}$$

where

$$Y_{in3} = 1/Z_{in3} = -jY_{st2}\cot\theta,\ \ Y_{st2} = 1/Z_{st2} \tag{A9}$$

The overall *ABCD*-parameters of 2-port network shown in Fig 17 are derived as (A10) by using $Y$-parameter to *ABCD*-parameter relation [20] and equation (A7)-(A9).

$$A_2 = \frac{Y'_{22}}{Y'_{21}} = \frac{Y_{0e3} + Y_{0o3}}{Y_{0o3} - Y_{0e3}} \tag{A10a}$$

$$B_2 = \frac{1}{Y'_{21}} = -j\frac{2\cot\theta\,(2Y_{st2} + Y_{0o3} + Y_{0e3})}{(Y_{0o3} - Y_{0e3})\left(Y_{0e3} + Y_{0o3} - 2Y_{st2}\cot^2\theta\right)} \tag{A10b}$$

$$C_2 = \frac{Y'_{11}Y'_{22}}{Y'_{21}} = j\cot\theta\frac{(Y_{0o3} - Y_{0e3})^2 - (Y_{0e3} + Y_{0o3})^2}{2\,(Y_{0o3} - Y_{0e3})} \tag{A10c}$$

$$D_2 = \frac{Y'_{22}}{Y'_{21}} = \frac{\left\{\begin{array}{l}(Y_{0o3} - Y_{0e3})^2\csc^2\theta - (Y_{0e3} + Y_{0o3})\\ (2Y_{st1} + Y_{0e3} + Y_{0o3})\cot^2\theta\end{array}\right\}}{(Y_{0o3} - Y_{0e3})\left(Y_{0e3} + Y_{0o3} - 2Y_{st2}\cot^2\theta\right)} \tag{A10d}$$

Fig. 18(a) shows the 1-port coupled line circuit when port ③ is open-circuited and ports ② and ④ are short-circuited. By applying boundary condition $V_2 = V_4 = 0$ and $I_3 = 0$ in equation (A6), the input impedance of a 1-port coupled line circuit can be derived as (A11).

$$Z_{in2} = \frac{Y_{22}}{Y_{11}^2 - Y_{12}^2} \tag{A11}$$

Fig. 18(b) shows the 1-port coupled line circuit when port ③ is short-circuited and ports ② and ④ are open-circuited. By applying boundary conditions $I_2 = I_4 = 0$ and $V_3 = 0$ in equation (A1), the input impedance of a 1-port coupled line circuit can be derived as (A12).

$$Z_{in4} = \frac{Z_{11}^2 - Z_{12}^2}{Z_{22}} \tag{A12}$$

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