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Design and analysis of variable attenuator with simultaneous minimized flat amplitude error and insertion phase variations

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Abstract

This paper presents a design of an analog variable attenuator with simultaneous minimized flat amplitude error and insertion phase variation over a wide bandwidth and high attenuation range. The parasitic of PIN is compensated with series transmission lines loaded and shunt capacitors to achieve minimum flat amplitude error and insertion phase variation. Mechanism for simultaneous reduction in flat amplitude error and phase variations is obtained by developing an analytical design equation using the PIN diode equivalent circuit model. For the experimental validation, two kinds of proposed attenuators are designed and measured over 1 GHz bandwidth at a center frequency (f_0) of 3.5 GHz. The measurement results are consistent with the simulation results. From the experiments, design-I provides an attenuation variation of 0.9 dB to 20 dB with a maximum flat amplitude error of 0.65 dB and insertion phase variation of 5.70° over 1 GHz bandwidth. Similarly, the design-II provides an attenuation variation of 1.06 dB to 20 dB with a maximum amplitude error of 0.49 dB and insertion phase variation of 3.19° over the same 1 GHz bandwidth.

KEYWORDS

analog attenuator, low amplitude error, low insertion phase variation, phased array, PIN diode, wide bandwidth

1 | INTRODUCTION

Variable attenuators, which primary function is to provide amplitude control for various applications, are key components in wireless communication, radar, and measurement systems.[1-3] Variable attenuators are widely used for self-interference cancelation in in-band full-duplex, amplitude weighting in T/R modules of wideband phased array antennas, and beamforming systems.[4-9] The variable attenuators are also used in measurement systems for gain control. Variable-gain amplifiers (VGAs) also perform a gain control function similar as attenuators, however, they typically exhibit limitations such as large amplitude variation, narrow operating bandwidth, limited linearity, unidirectional operation and large power consumptions, and complex system configurations as compared to attenuators.[10,11] For phased array beamforming networks, variable attenuators are placed in series with a phase shifter, where insertion phase variation

of attenuator and amplitude error must be as small as possible to quickly steer the lobes and nulls of antenna beams.

Variable attenuators are analog (continuous) and digital step attenuators based on the type of control voltage. Digital attenuators can provide the 2^N-1 attenuation level with respect to reference mode by controlling N-bit control voltage. Different configurations of digital attenuator are presented in the literature, including distributed, switched-path, and switched pi/T-type.[12-18] Digital attenuators have relatively low insertion phase variations; however, these attenuators still suffer from drawbacks of relatively high flat amplitude error and potential limit of fine amplitude control in wideband applications because of the parasitic effect of the MOS switch. Moreover, simultaneous minimization of flat amplitude error and insertion phase variation of variable attenuators are challenging.

In contrast to digital attenuators, analog attenuators have continuous attenuation control with very fine amplitude. With regards to analog attenuators, reflection-type attenuators are widely used because of their excellent return loss characteristics. In,[19] the varactor-based reflection-type attenuator is designed for 0.4 GHz bandwidth at a center frequency (f_0) of 2.5 GHz. However, the parasitic effect of varactor diodes influences transmission phase and insertion losses, which results in high insertion phase variations and flat amplitude error with respect to frequency. Similarly, a wideband reflection-type attenuator is presented in[20] without providing flat amplitude error and insertion phase variation. In,[21-23] multi-layer graphene flakes are used for the variable attenuator. The graphene resistance was controlled with dc bias voltage and the current flowing. Although variable attenuations are obtained over wideband, flat amplitude error and insertion phase variations are high.

In recent years, there are some efforts to minimize the insertion phase variation of analog attenuators. In,[24] a reflection-type attenuator is presented by using PIN diode terminated with the open-circuited transmission line (TL), which provides low insertion phase variation only at the single center frequency. Similarly, reflection-type and transmission-type attenuators have been presented in[25] without any results of the flat amplitude error and insertion phase variations. In,[26] a variable attenuator is presented by using TL terminated with a PIN diode, which provides low insertion phase variation with high attenuation range only at around center frequency. Similarly, three shunt PIN diodes are used in a branch-line directional coupler for a variable attenuator with a large circuit size.[27] In,[28-31] substrate integrated waveguide attenuators were presented. Despite significant research in the field of analog/digital attenuators, the previously presented works[19-31] are mainly focused on amplitude control rather than simultaneous flat amplitude error and insertion phase variations minimization, which are significantly essential for phased array and beamforming systems in wireless communication systems.

In this paper, we present in-depth and through investigation of reflection-type variable attenuator with high attenuation variation and simultaneous minimized flat amplitude error and insertion phase variation over the wide bandwidth. By developing the analytical equations based on the PIN diode equivalent circuit model, the mechanism of a simultaneous reduction in amplitude and phase variation is shown. The proposed attenuators achieved a high attenuation range with very small flat amplitude error and low phase variation by compensating the PIN diode parasitic with transmission line and shunt capacitors.

2 | ANALYSIS AND DESIGN METHOD

2.1 | Implementation of two-port reflection-type circuit

Figure 1 shows the structure of the reflection-type analog attenuator, which consists of a 3-dB hybrid, where coupled and through ports are terminated with reflection load (Γ_L). Assuming the coupled and through responses of the hybrid coupler are S_{21}^H and S_{31}^H, respectively, the *S*-parameters of the two-port reflection-type attenuator with the two-reflection termination load (Γ_L)[32] are expressed as (1).

$$S_{11} = S_{22} = \left[\left(S_{21}^H\right)^2 + \left(S_{31}^H\right)^2\right]\Gamma_L = R^H\Gamma_L \tag{1a}$$

$$S_{21} = S_{12} = 2S_{21}^H S_{31}^H\Gamma_L = T^H\Gamma_L \tag{1b}$$

The combined two-port reflection-type attenuator exhibits perfect matching only if the hybrid coupler exhibits the *S*-parameters such that $|R^H| = |\left(S_{21}^H\right)^2 + \left(S_{31}^H\right)^2| = 0$ and $|T^H| = |2S_{21}^H S_{31}^H| = 1$. However, practical hybrid coupler *S*-parameters vary with respect to frequency. To address issue, the designer should choose a

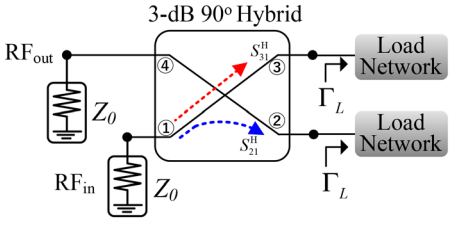

FIGURE 1 General structure of reflection-type attenuator with reflection load (Γ_L)

wideband hybrid coupler with minimum magnitude and phase imbalance between through and coupled port and a high return loss of more than 20 dB over a wide operating band. Assuming an ideal hybrid coupler, the *S*-parameter of the reflection-type attenuator can be simplified as (2).

$$[S]_{\text{attnuator}} = \begin{bmatrix} 0 & \Gamma_L \\ \Gamma_L & 0 \end{bmatrix} \tag{2}$$

As seen from (2), the insertion magnitude and phase mainly depend on Γ_L, we will analyze the proposed attenuator by deriving the Γ_L.

2.2 | Design-I: Reflection-type attenuator with single series transmission line and shunt capacitor

Figure 2 shows the proposed structure of the design-I reflection-type attenuator. The proposed structure consists of a 3-dB hybrid, where coupled and through ports are terminated reflection load. The reflection load (Γ_L) consists of TL with shunt capacitor (C_S) and PIN diode. The characteristic impedance and electrical length of TL are denoted by Z_1 and θ_1, respectively. The equivalent circuit of the PIN diode is also shown in Figure 2, which consists of variable resistor R_j along with parasitic series inductor L_s, resistance R_s, and junction capacitor C_j.[33] Using the equivalent circuit model of the PIN diode, Γ_L of the proposed attenuator is derived as (3).

$$\Gamma_L = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} = \frac{\alpha_3 - Z_0\alpha_5 + j(\alpha_4 - Z_0\alpha_6)}{\alpha_3 + Z_0\alpha_5 + j(\alpha_4 + Z_0\alpha_6)}, \tag{3}$$

where

$$\alpha_1 = R_s + \frac{R_j}{1 + 4\pi^2 f^2 C_j^2 R_j^2} \tag{4a}$$

$$\alpha_2 = \omega\left(L_s - \frac{R_j^2 C_j}{1 + 4\pi^2 f^2 C_j^2 R_j^2}\right) \tag{4b}$$

$$\alpha_3 = Z_1\alpha_1\{1 - 2\pi f C_S Z_1 \tan(\theta f/f_0)\} \tag{4c}$$

$$\alpha_4 = Z_1\alpha_2 + Z_1^2(1 - 2\pi f C_S\alpha_2)\tan(\theta f/f_0) \tag{4d}$$

$$\alpha_5 = Z_1(1 - 2\pi f C_S\alpha_2) - \alpha_2\tan(\theta f/f_0) \tag{4e}$$

$$\alpha_6 = \alpha_1\{2\pi f Z_1 C_S + \tan(\theta f/f_0)\}, \tag{4f}$$

and f and f_0 are the operating frequency and center frequency, respectively. Similarly, $Z_0 = 50\ \Omega$ is RF port reference impedance. From (3), the magnitude and phase of reflection load are determined as (5).

$$|\Gamma_L| = \sqrt{\frac{(\alpha_3 - Z_0\alpha_5)^2 + (\alpha_4 - Z_0\alpha_6)^2}{(\alpha_3 + Z_0\alpha_5)^2 + (\alpha_4 + Z_0\alpha_6)^2}} \tag{5a}$$

$$\varphi = \angle\Gamma_L = \tan^{-1}\left(\frac{\alpha_4 - Z_0\alpha_6}{\alpha_3 - Z_0\alpha_5}\right) - \tan^{-1}\left(\frac{\alpha_4 + Z_0\alpha_6}{\alpha_3 + Z_0\alpha_5}\right) \tag{5b}$$

The maximum attenuation is achieved when $R_j = (R_j)_{\min} \approx 50\ \Omega$ since the RF signal is not transmitted to load at isolation port. On the other hand, the RF signal is completely transmitted to load when $R_j = (R_j)_{\max} \approx \infty\ \Omega$ because of the total reflection at Γ_L. In this case, attenuation is 0 dB. The parasitic of PIN diode will influence amplitude and insertion phase. Therefore, the flat amplitude error and insertion phase variation will be degraded if attenuation level is changed. To investigate this issue, the flat amplitude error (Δ_{err}) and relative phase variation (ϕ_{var}) of the proposed attenuator are defined as (6).

$$\Delta_{err} = \max\left(|\Gamma_L|_{R_j = (R_j)_{\max} : (R_j)_{\min}} - |\Gamma_L|^{f=f_0}_{R_j = (R_j)_{\max} : (R_j)_{\min}}\right) \tag{6a}$$

$$\phi_{\text{var}} = \max\left(\phi|_{R_j = (R_j)_{\max} : (R_j)_{\min}} - \phi|_{R_j = (R_j)_{\max}}\right) \tag{6b}$$

Since $|\Gamma_L|$ and ϕ are a function of C_S, Z_1, and θ, the proposed attenuator with simultaneous minimized Δ_{err}

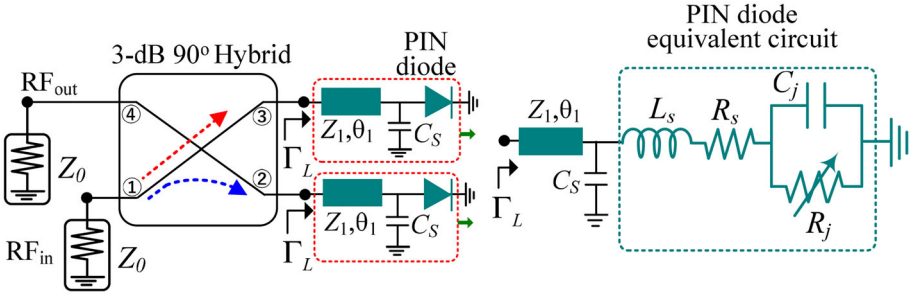

FIGURE 2 Proposed structure of reflection-type design-I attenuator using PIN and its equivalent circuit

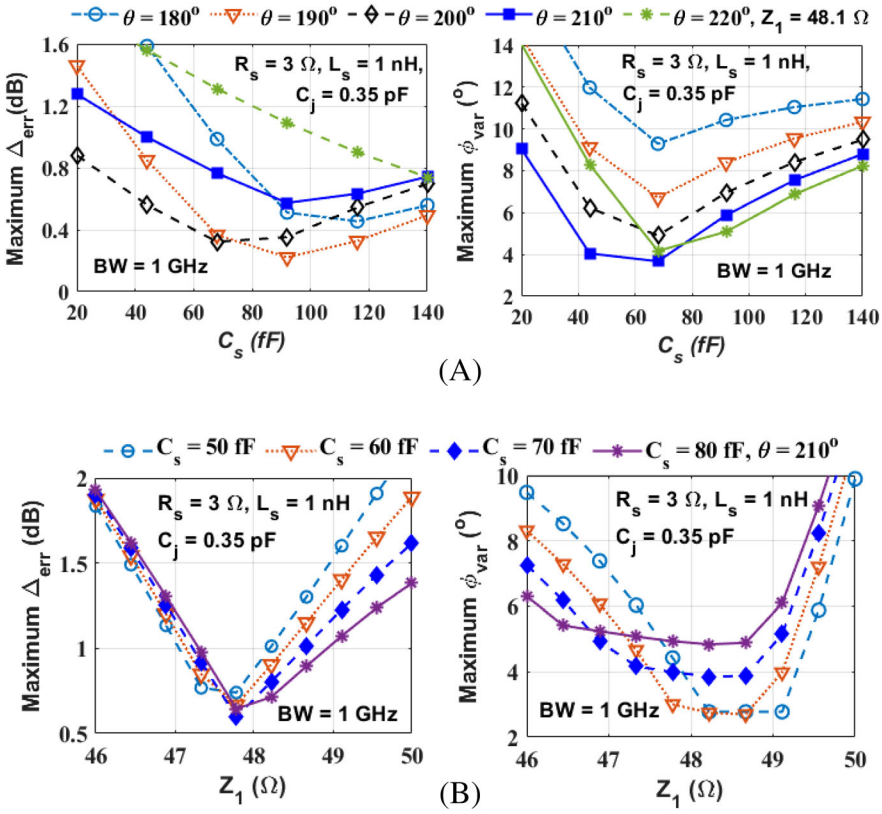

FIGURE 3 Calculated maximum amplitude error and insertion phase variation of design-I attenuator with different: (A) θ and C_s with fixed Z_1, and (B) Z_1 and C_s with fixed θ. PIN diode HSMP-4810 with parasitic elements: $R_s = 3\ \Omega$, $L_s = 1$ nH, and $C_j = 0.35$ pF. R_j is varied from 62 to 2000 Ω for an attenuation range of 20 to 0.8 dB

and ϕ_{var} can be implemented by selecting appropriate values of C_S, Z_1, and θ. Because of an analytical solution difficulty, the MATLAB tool is used to analyze optimum values of C_S, Z_1, and θ for minimum Δ_{err} and ϕ_{var}.

Figure 3A shows the calculated Δ_{err} and φ_{var} according to C_s and θ. In these calculations, PIN diode HSMP 4810 from Avago is used. The parasitic elements of PIN diode provided by manufacture are given as $R_s = 3\ \Omega$, $L_s = 1$ nH and $C_j = 0.35$ pF.[33] With fixed Z_1, Δ_{err} is minimum (< 0.25 dB) when $\theta = 190°$ and $C_s = 90$ fF, however, φ_{var} is around 9°. Similarly, ϕ_{var} is minimum (< 4°) when $\theta = 210°$ and $C_s = 65$ fF, however, Δ_{err} is 0.85 dB. Therefore, a trade-off exists between Δ_{err} and ϕ_{var}. Figure 3B shows the calculated maximum Δ_{err} and ϕ_{var} of design-I attenuator according to C_s, $Z_1$and fixed θ. The Δ_{err} is minimum if Z_1 is around 47.8 Ω, whereas ϕ_{var} is minimum if Z_1 is around 48.5 Ω.

To validate the simultaneous minimization of amplitude error and phase variation of the proposed design-I attenuator, Figure 4 shows calculated $|\Gamma_L|$, phase of Γ_L, Δ_{err} and ϕ_{var} according to different R_j. From the analysis, the values of C_s, Z_1, and θ are chosen by compromising between minimum Δ_{err} and ϕ_{var}. The results showed that attenuation is achieved between 0.6 dB to 20 dB with Δ_{err} of 0.7 dB and ϕ_{var} of 4.6° within 1 GHz bandwidth at f_0 of 3.5 GHz. As seen from the above analysis, the Δ_{err} and ϕ_{var} cannot be minimized lower than 0.6 dB and 4° simultaneously with single C_S and TL. To further minimize Δ_{err} and ϕ_{var}, we extended several shunt capacitors and series TL. The detailed description of the design-II attenuator will be described in the next section.

2.3 | Design-II: Reflection type attenuator with two series transmission line and two shunt capacitors

Figure 5 shows the proposed structure of the design-II attenuator, which consists of a 3-dB hybrid and reflection load. The reflection load consists of two sections of TL and shunt capacitor terminated with a PIN diode. The characteristic impedance and electrical lengths of two section TL are represented with Z_1, θ_1, and θ_2, respectively. Similarly, two shunt capacitors are denoted with C_{S1} and C_{S2}. Using the equivalent circuit of PIN diode, the reflection coefficient Γ_L of load network is determined as (7).

$$\Gamma_L = \frac{k_7 - Z_0 k_9 + j(k_8 - Z_0 k_{10})}{k_7 + Z_0 k_9 + j(k_8 + Z_0 k_{10})}, \tag{7}$$

where

$$k_1 = R_s + \frac{R_j}{1 + 4\pi^2 f^2 C_j^2 R_j^2} \tag{8a}$$

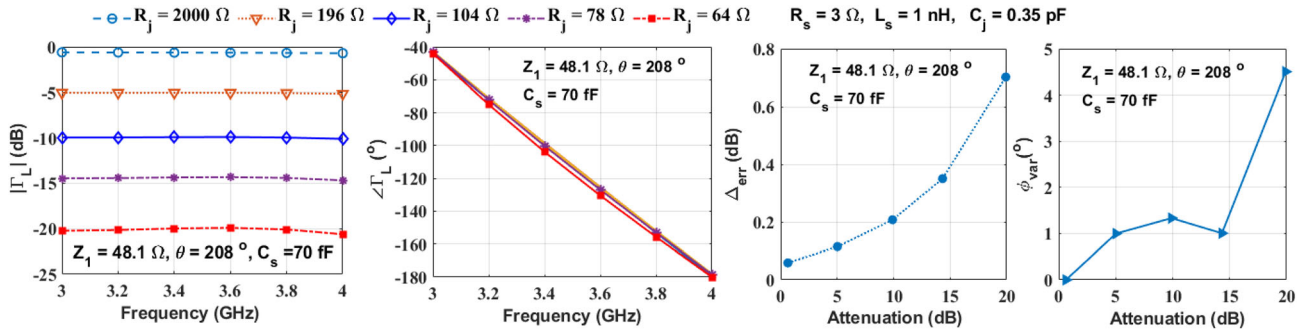

FIGURE 4 Calculated amplitude, insertion phase, amplitude error, and phase variation of design-I attenuator using PIN diode HSMP-4810 of Avago with parasitic elements: $R_s = 3\ \Omega$, $L_s = 1$ nH, and $C_j = 0.35$ pF

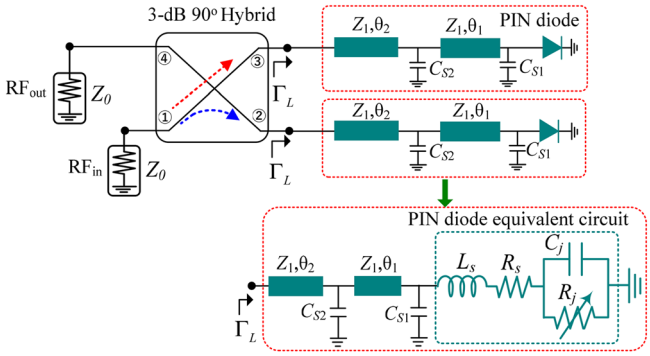

FIGURE 5 Proposed structure of design-II attenuator using PIN and its equivalent circuit

$$k_2 = \omega\left(L_s - \frac{R_j^2 C_j}{1 + 4\pi^2 f^2 C_j^2 R_j^2}\right) \tag{8b}$$

$$k_3 = Z_1 k_1\{1 - 2\pi f C_{S1} Z_1 \tan(\theta_1 f/f_0)\} \tag{8c}$$

$$k_4 = Z_1 k_2 + Z_1^2(1 - 2\pi f C_{S1} k_2)\tan(\theta_1 f/f_0) \tag{8d}$$

$$k_5 = Z_1(1 - 2\pi f C_{S1} k_2) - k_2 \tan(\theta_1 f/f_0) \tag{8e}$$

$$k_6 = k_1\{2\pi f Z_1 C_{S1} + \tan(\theta_1 f/f_0)\} \tag{8f}$$

$$k_7 = k_3 Z_1 - Z_1 Z_1 \tan(\theta_2 f/f_0)(2\pi f C_{s2} k_3 + k_6) \tag{8g}$$

$$k_8 = Z_1\{k_4 + Z_1 k_5 \tan(\theta_2 f/f_0) - 2\pi f Z_1 C_{s2} k_4 \tan(\theta_2 f/f_0)\} \tag{8h}$$

$$k_9 = Z_1(k_5 - 2\pi f C_{s2} k_4) - k_4 \tan(\theta_2 f/f_0) \tag{8i}$$

$$k_{10} = k_3 \tan(\theta_2 f/f_0) + Z_1(2\pi f C_{s2} k_3 + k_6) \tag{8j}$$

From (7), the magnitude and phase of reflection load are determined as (9).

$$|\Gamma_L| = \sqrt{\frac{(k_7 - Z_0 k_9)^2 + (k_8 - Z_0 k_{10})^2}{(k_7 + Z_0 k_9)^2 + (k_8 + Z_0 k_{10})^2}} \tag{9a}$$

$$\phi = \angle\Gamma_L = \tan^{-1}\left(\frac{k_8 - Z_0 k_{10}}{k_7 - Z_0 k_9}\right) - \tan^{-1}\left(\frac{k_8 + Z_0 k_{10}}{k_7 + Z_0 k_9}\right) \tag{9b}$$

Since the reflection load of the design-II attenuator is also a function of R_j, the maximum attenuation is achieved when $R_j = (R_j)_{\min} \approx 50\ \Omega$ since no RF signal is reflected ($|\Gamma_L| = 0$) from reflection load. On the other hand, the RF signal is completely transmitted to load when $R_j = (R_j)_{\max} \approx \infty\ \Omega$ because of the total reflection ($|\Gamma_L| = 1$). In this case, attenuation is 0 dB. However, amplitude and phase will be changed with frequency because of parasitic R_s, L_s, and C_j. The amplitude error (Δ_{err}) and phase variation (ϕ_{var}) are given by (6) by replacing $|\Gamma_L|$ and ϕ of design-I attenuator with $|\Gamma_L|$ and ϕ of design-II attenuator as given in (7).

Since $|\Gamma_L|$ and ϕ of the design-II attenuator is a function of Z_1, C_{S1}, C_{S2}, θ_1, and θ_2 (five degrees of freedom), the simultaneous minimization of Δ_{err} and ϕ_{var} can be achieved by finding the optimum value of Z_1, C_{S1}, C_{S2}, θ_1, and θ_2. Since finding an analytical solution of Z_1, C_{S1}, C_{S2}, θ_1, and θ_2 for minimum Δ_{err} and ϕ_{var} are difficult, the MATLAB tool is used for analysis.

Figure 6A shows calculated the maximum Δ_{err} and ϕ_{var} of design-II attenuator according to C_{S1} and C_{S2} with fixed Z_1, θ_1, and θ_2. For these calculations, we use the equivalent model of PIN diode HSMP-4810 from Avago with parasitic elements of $L_s = 1$ nH, $R_s = 3\ \Omega$ and $C_j = 0.35$ pF provided by manufacture.[33] Δ_{err} is minimum when $C_{S1} = 0.28$ pF and $C_{S2} = 0.14$ pF. On the other hand, ϕ_{var} is minimum when $C_{S1} = 0.26$ pF and $C_{S2} = 0.12$ pF. Figure 6B shows calculated the maximum Δ_{err} and ϕ_{var} according to θ_1 and θ_2 with fixed C_{S1}, C_{S2} and Z_1. In this case, Δ_{err} is minimum

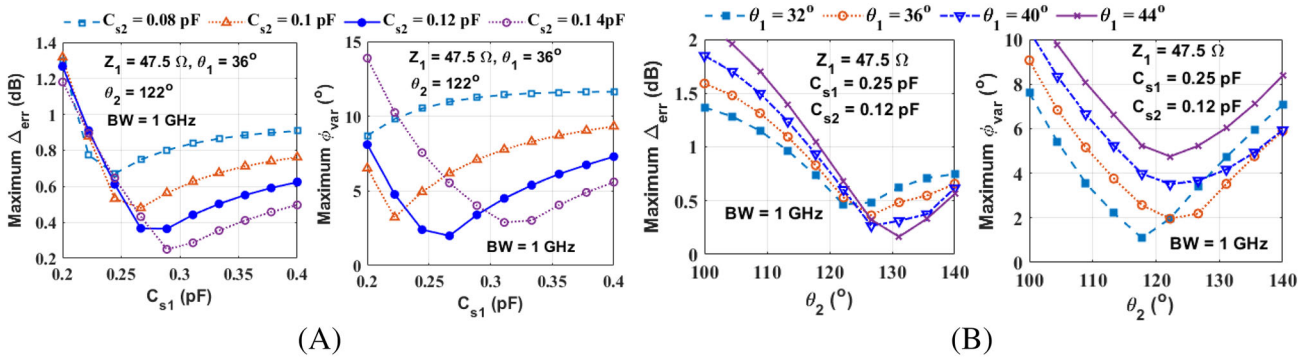

FIGURE 6 Calculated maximum amplitude error and insertion phase variation of design-II attenuator with different: (A) C_{S1} and C_{S2} with fixed θ_1, θ_2, and Z_1, and (B) θ_1 and θ_2 with fixed Z_1, C_{S1}, and C_{S2}. PIN diode HSMP-4810 of Avago with parasitic element $R_s = 3\ \Omega$, $L_s = 1$ nH, and $C_j = 0.35$ pF. R_j is varied from 2000 to 62 Ω for an attenuation range of 0.8 dB to 20 dB

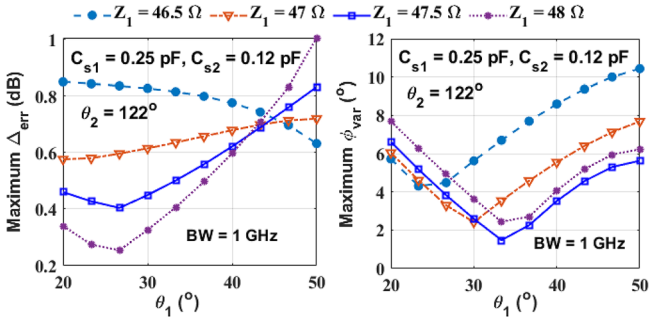

FIGURE 7 Calculated maximum amplitude error and insertion phase variation of design-I attenuator with different θ_1 and Z_1 and fixed θ_2, C_{S1}, and C_{S2}. PIN diode HSMP-4810 with parasitic elements: $R_s = 3\ \Omega$, $L_s = 1$ nH, and $C_j = 0.35$ pF. R_j is varied from 2000 to 62 Ω for an attenuation range of 0.8 dB to 20 dB

when $\theta_1 = 44°$ and $\theta_2 = 132°$, however, ϕ_{var} is high. Similarly, ϕ_{var} is minimum when $\theta_1 = 32°$ and $\theta_2 = 118°$, however, Δ_{err} is higher than 0.5 dB.

Figure 7 shows the shows calculated maximum Δ_{err} and ϕ_{var} according to θ_1, and Z_1 with fixed C_{S1}, C_{S2}, and θ_2. In this case, Δ_{err} is minimum when $Z_1 = 48\ \Omega$ and $\theta_1 = 28°$, whereas ϕ_{var} is minimum when $Z_1 = 47.5\ \Omega$ and $\theta_1 = 36°$. Based on results shown in Figures 6 and 7, the optimum values of Z_1, C_{S1}, C_{S2}, θ_1, and θ_2 for simultaneous minimized Δ_{err} and ϕ_{var} should be chosen by considering a trade-off between them. By trade-off between Δ_{err} (< 0.5 dB) and ϕ_{var} (< 2°), the optimum circuit parameters of design-II are determined as $C_{S1} = 0.25$ pF, $C_{S2} = 0.12$ pF, $Z_1 = 47.5\ \Omega$, $\theta_1 = 36.3°$, and $\theta_2 = 122°$.

Figure 8 shows the calculated $|\Gamma_L|$, $\angle\Gamma_L$, Δ_{err}, and ϕ_{var} of design-II attenuator according to R_j. The attenuation is achieved between 0.5 to 20 dB by varying $R_j = 2000$ to 51.8 Ω. Similarly, maximum Δ_{err}, and ϕ_{var} is less than 0.45 dB and 1.80°, respectively.

Figure 9 shows the calculated Δ_{err} and ϕ_{var} according to operating bandwidth (BW) of design-I and design-II attenuator. The maximum flat amplitude error and relative phase variation are increased with an increase of BW. So, trade-off exhibits among operating BW, amplitude error, and insertion phase variation.

Figure 10A shows the flat Δ_{err}, and ϕ_{var} of attenuator with and without phase/amplitude compensation technique. The flat amplitude error and phase variation are high if we do not adopt the compensation technique. On other hand, the proposed attenuators, which adopt the simultaneous amplitude error and phase variation compensation technique using series TL and shunt capacitor, provides the very low amplitude error and phase variation. Figure 10B shows the design flow diagram of the proposed attenuators. Based on the above analysis of the proposed attenuators (design-I and design-II), the calculation method of optimum circuits for simultaneous minimized amplitude error and phase variation is summarized as follows:

a. Define center frequency f_0, bandwidth (BW), required flat amplitude error ($\Delta_{err}^{\text{Req}}$), and insertion phase variation ($\phi_{\text{var}}^{\text{Req}}$).
b. Obtain PIN diode parasitic elements R_s, L_s, and C_j provided manufacture. These values are generally given in the datasheet of the PIN diode.
c. Once parasitic elements of PIN diode are obtained, select initial values of Z_1, θ, and C_S in case of design-I and Z_1, θ_1, θ_2, C_{S1}, and C_{S2} in case of design-II. For initial circuit parameters selection, refer to Figure 3 in case of design-I and Figures 6, 7 in case of design-II.
d. By varying the value of R_j from $(R_j)_{\max}$ to $(R_j)_{\min}$, calculate flat amplitude error ($\Delta_{err}^{\text{cal}}$) and insertion phase variation ($\phi_{\text{var}}^{\text{cal}}$) using (5) and (6) in case design-I and using (9) and (6) in case of design-II.
e. Compare calculated amplitude error and phase variation with the required values. If $\Delta_{err}^{\text{cal}} < \Delta_{err}^{\text{Req}}$ and $\phi_{\text{var}}^{\text{cal}} < \phi_{\text{var}}^{\text{Req}}$, then Z_1, θ, and C_S are optimum values in the

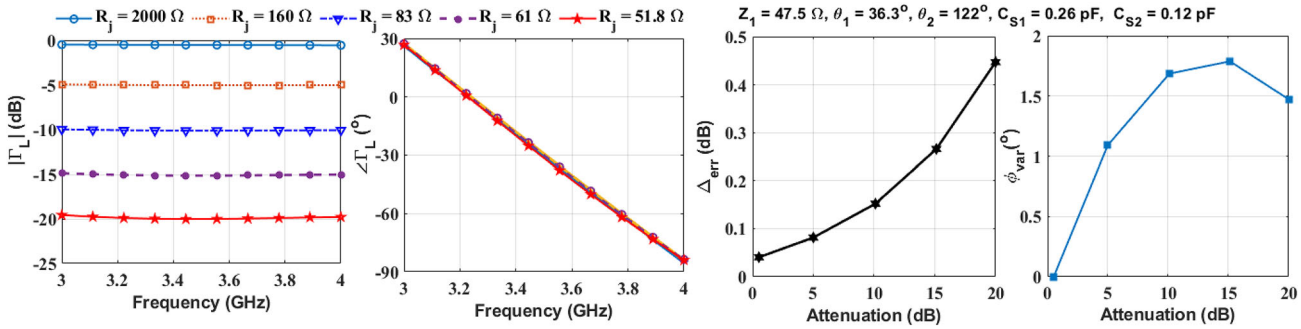

FIGURE 8 Calculated amplitude, insertion phase, amplitude error and phase variation of design-II attenuator using PIN diode HSMP-4810 of Avago with parasitic elements: $R_s = 3\ \Omega$, $L_s = 1$ nH, and $C_j = 0.35$ pF

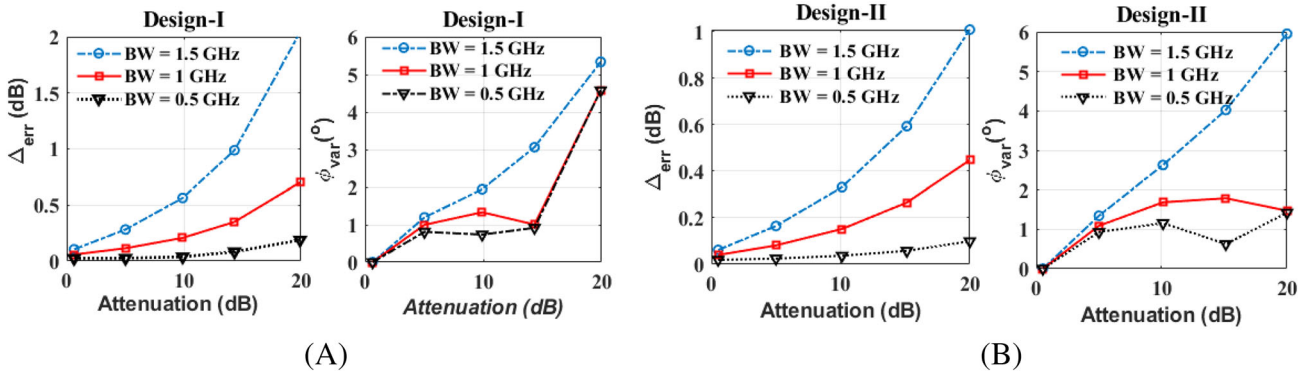

FIGURE 9 Calculated maximum amplitude error and insertion phase variation of the proposed attenuators with different bandwidths: (A) design-I and (B) design-II. PIN diode HSMP-4810 of Avago with parasitic elements: $R_s = 3\ \Omega$, $L_s = 1$ nH, and $C_j = 0.35$ pF

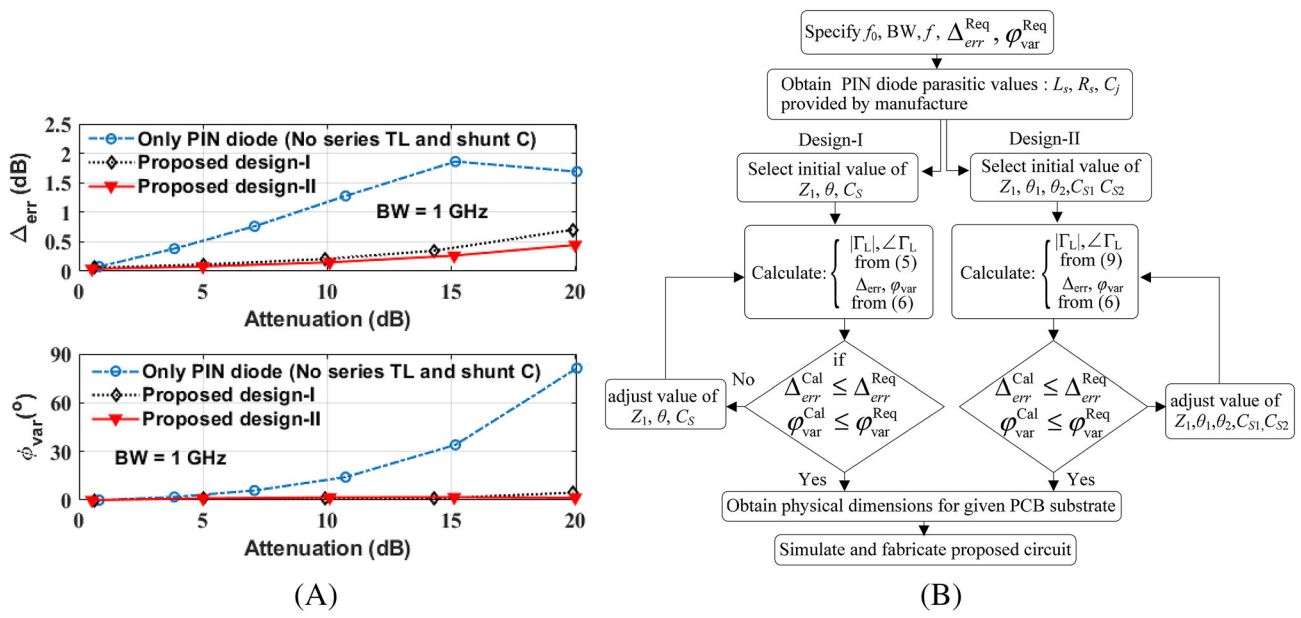

FIGURE 10 (A) Comparison between with/without simultaneous amplitude and phase variation compensation technique and (B) design flow of the proposed reflection-type attenuators. PIN diode HSMP-4810 of Avago with parasitic elements: $R_s = 3\ \Omega$, $L_s = 1$ nH, and $C_j = 0.35$ pF

case of design-I and Z_1, θ_1, θ_2, C_{S1}, and C_{S2} are optimum values in case of design of design-II.

f. If conditions ($\Delta_{err}^{cal} < \Delta_{err}^{Req}$ and $\phi_{var}^{cal} < \phi_{var}^{Req}$) are not satisfied, then adjust the values of Z_1, Z_1, θ, and C_S in case of design-I and Z_1, θ_1, θ_2, C_{S1}, and C_{S2} in case of design-II, and repeat process (d) and (e).

g. After obtaining optimum circuit parameters, fabricate the circuit with a given PCB substrate and perform the measurement.

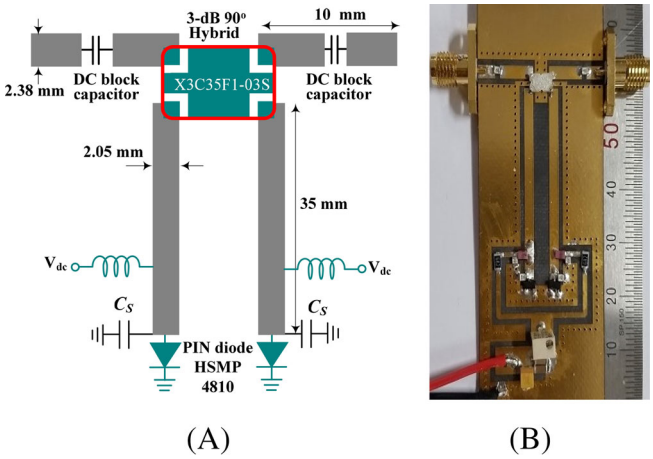

FIGURE 11 (A) Layout and (B) photograph of fabricated design-I reflection type attenuator

3 | EXPERIMENTAL RESULTS

For experimental verification, prototypes of the proposed attenuators (design-I and design-II) are designed and fabricated at f_0 of 3.5 GHz. The substrate RT/Duroid 5880 with a dielectric constant (ε_r) of 2.2 and thickness (h) of 0.787 mm was used. Avago surface mount RF PIN diode HSMP-4810[33] and ANAREN hybrid coupler X3C35F1-03S were used.[34]

3.1 | Design-I: Reflection-type attenuator with single series TL and shunt capacitor

The goal of the design-I attenuator is to achieve simultaneous Δerr and ϕ_{var} less than 0.7 dB and 5°, respectively, for 0.8 to 20 dB attenuation range and 1 GHz BW. According to design goal, the optimum circuit parameters are determined as $Z_1 = 48.1\ \Omega$, $C_S = 0.1$ pF, and $\theta_1 = 208°$. Figure 11 shows a layout and a photograph of the design-I fabricated attenuator. The overall size of the fabricated circuit is 56 mm × 28.36 mm.

Figure 12 depicts the simulation and measurement results of a design-I attenuator. As shown in Figure 12A, the attenuation is flat and varies from 0.9 to 20 dB within 1 GHz BW. The input return loss is better than 13 dB, as shown in Figure 12B. The measured return loss is slightly

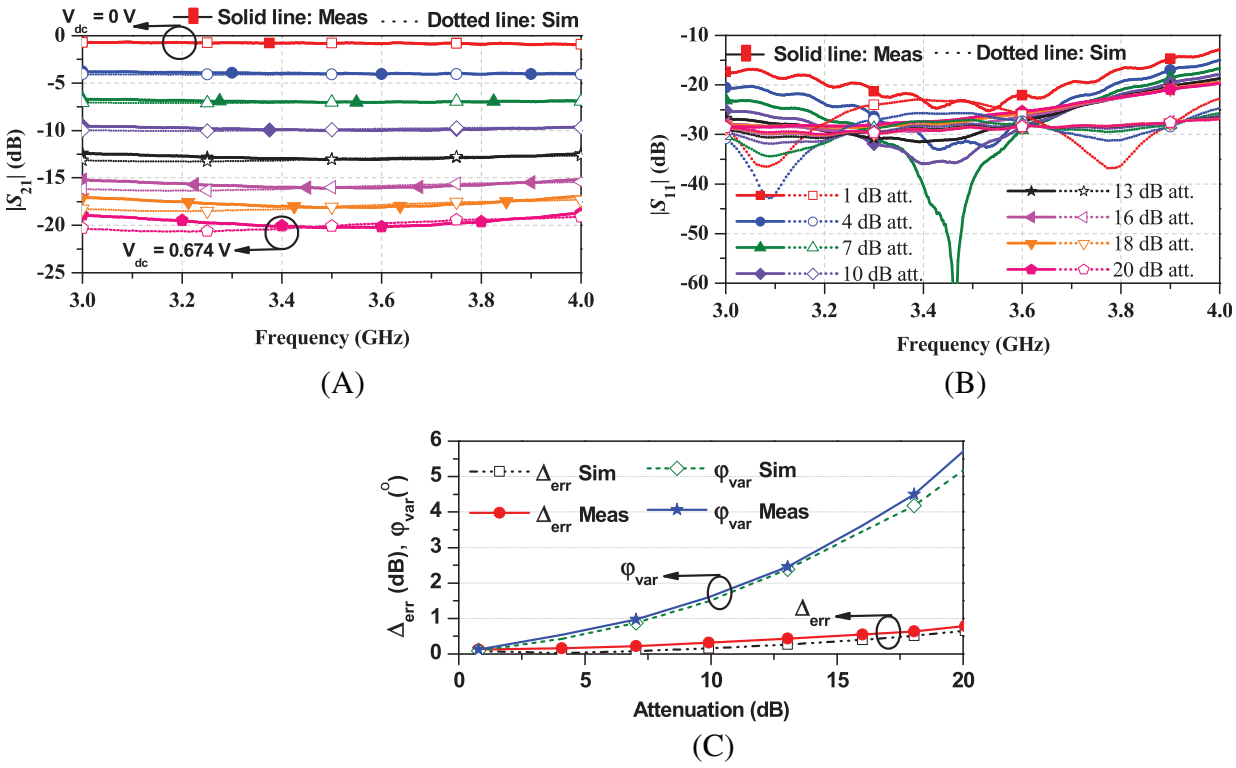

FIGURE 12 Simulation and measure results of the design-I reflection type attenuator: (A) magnitude of S_{21}, (B) input/output return loss, and (b) measured amplitude error and insertion phase variation

degraded as compared to the simulation due to non-ideal capacitors. The measured maximum Δ_{err} and ϕ_{var} are 0.65 dB and 5.7° for an attenuation range of 0.9 to 20 dB within 1 GHz BW, as shown in Figure 12C. The measured results of design-I attenuator is summarized in Table 1.

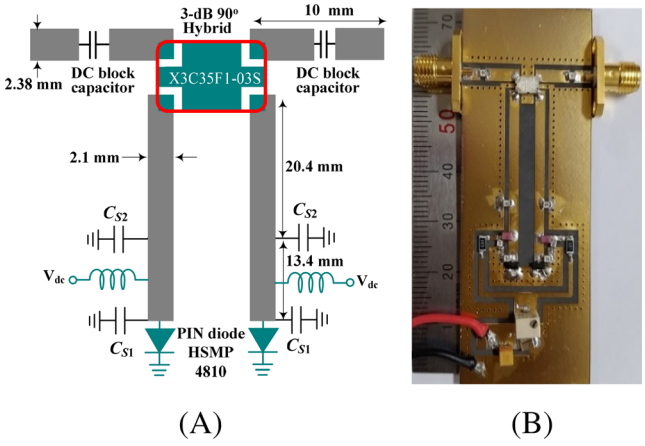

FIGURE 13 (A) Layout and (B) photograph of fabricated design-II reflection type attenuator

3.2 | Design-II: Reflection-type attenuator with two series TLs and shunt capacitor

The goal of the design-II attenuator is to achieve Δ_{err} and ϕ_{var} less than 0.5 dB and 3°, respectively, for 0.8 to 20 dB attenuation range and 1 GHz BW. For this purpose, the circuit parameters of design-II attenuator are given as $Z_1 = 47.6\ \Omega$, $\theta_1 = 36°$, $\theta_2 = 122°$, $C_{S1} = 0.25$ pF and $C_{S2} = 0.12$ pF. Figure 13 shows the layout and photograph of the fabricated attenuator. The overall size of the fabricated circuit is 54 mm × 28.36 mm.

Figure 14 shows that the measurement and simulation results. As shown in Figure 14A, the attenuation varies from 1.06 dB to 20 dB at f_0 and almost flat over the 1 GHz bandwidth. The input return loss is better than 17.3 dB, as shown in Figure 14B. The maximum Δ_{err} and ϕ_{var} are 0.49 dB and 3.19°, respectively, as shown in Figure 14C. The measured Δ_{err} and ϕ_{var} of the design-II attenuator is smaller than design-I because more degree of freedom to simultaneous minimization of flat amplitude error and phase variation as compared to design I. The measured results of design-II attenuator is summarized in Table 2.

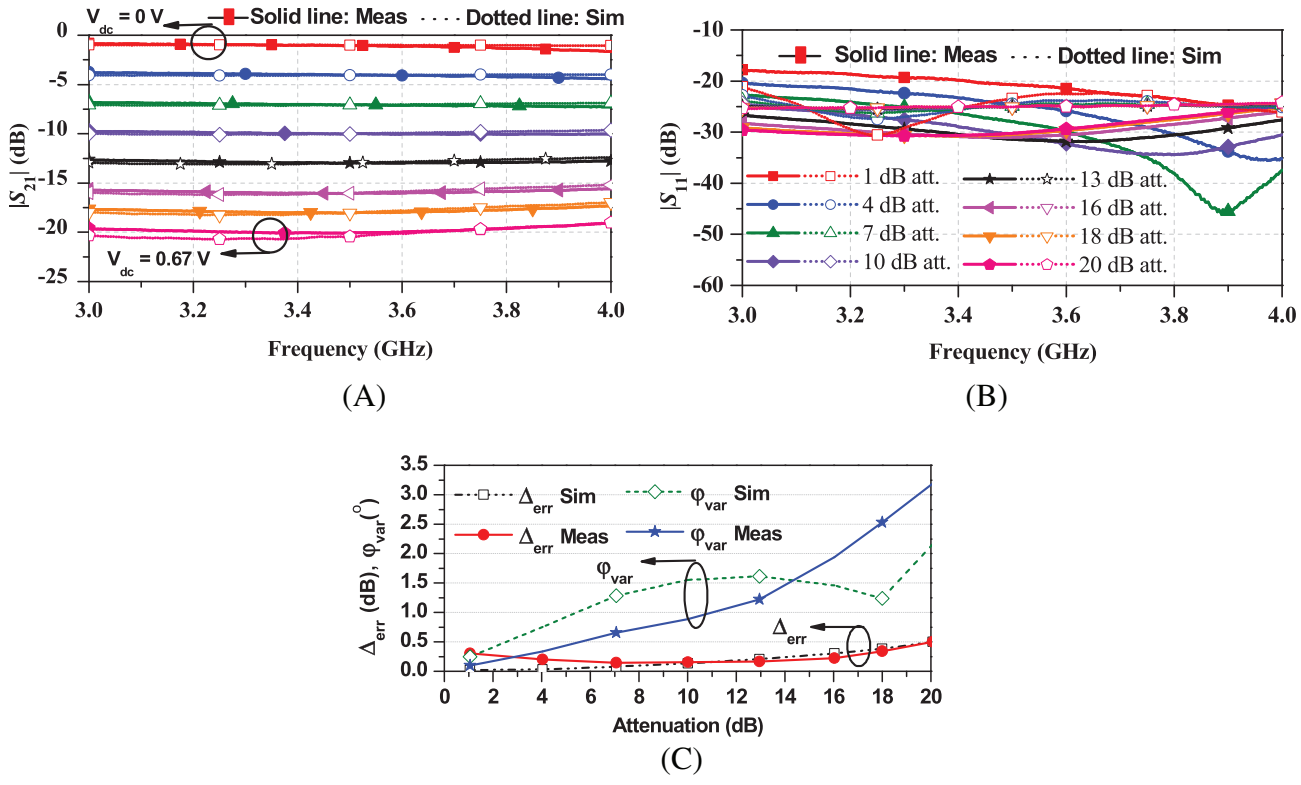

FIGURE 14 Simulated and measured performance of the proposed variable attenuator II: (A) attenuation, (B) return loss, and (C) flat amplitude error and insertion phase variation

TABLE 1 Measurement results of design-I attenuator

Attenuation (dB)	V_{dc} (V)	DC current (mA)	Δ_{err} (dB)	φ_{var} (Deg)
0.9	0	1	0.12	0.12
4	0.591	1	0.15	0.54
7	0.627	1	0.22	0.97
10	0.645	2	0.31	1.59
13	0.658	2	0.43	2.45
16	0.666	2	0.54	3.62
18	0.67	2	0.63	4.52
20	0.674	2	0.78	5.76

TABLE 2 Measurement results of design-II attenuator

Attenuation (dB)	V_{dc} (V)	DC current (mA)	Δ_{err} (dB)	φ_{var} (Deg)
1.06	0	1	0.30	0
4	0.582	1	0.20	0.33
7	0.622	1	0.14	0.65
10	0.642	2	0.15	0.88
13	0.655	2	0.16	1.22
16	0.662	2	0.22	1.94
18	0.666	2	0.33	2.53
20	0.670	2	0.49	3.19

TABLE 3 Performance comparison with state-of-the-art

References	Freq (GHz)	Type	Technology	Attenuation range (dB)	Δ_{err} (dB)	ϕ_{var} (Deg)	Return loss (dB)	FBW (%)	DC power (mW)	FOM
14	50 ∼ 110	Digital	CMOS	5 ∼ 15	1.5	11	>15	75	NA	45.45
15	0.4 ∼ 3.7	Digital	CMOS	2.1 ∼ 33	3	65	>9	160	NA	25.35
16	DC ∼20	6-bit digital	CMOS	0.5 ∼ 31	1.8	16	>12	200	NA	211.80
17	37 ∼ 40	5-bit digital	CMOS	1 ∼ 31	0.8	12	>12	7.79	NA	24.35
18	DC ∼ 18*	6-bit digital	CMOS	2.1 ∼ 31	0.90	11	>11	200	NA	590
19	2.3 ∼ 2.7	Analog	Microstrip line	1.6 ∼ 38	10	NA	>9.8	16	NA	NA
20	2.8 ∼ 4.2	Analog	Microstrip line	2.2 ∼ 17	NA	NA	NA	40	NA	NA
24	1.855	Analog	Microstrip line	0.5 ∼ 30	NA	3	>17	NA	NA	NA
25	9.1 ∼ 9.6	Analog	Microstrip line	2.5 ∼ 28	NA	NA	>9.8	5.35	NA	NA
26	2.11 ∼ 2.17	Analog	Microstrip line	1 ∼ 30	0.8	3	>15	2.80	NA	35
27	1.3 ∼ 2.6	Analog	Microstrip line	0.7 ∼ 23	5	NA	NA	66.6	NA	NA
29	7.29 ∼ 14.90	Analog	SIW	2.5 ∼ 6.5	1	NA	NA	68.5	NA	NA
This work^{I}	**3 ∼ 4**	**Analog**	Microstrip line	**0.9 ∼ 20**	**0.65**	**5.70**	**> 13**	**28.6**	**1.348**	**154.38**
This work^{II}	**3 ∼ 4**	**Analog**	Microstrip line	**1.06 ∼ 20**	**0.49**	**3.19**	**>17.3**	**28.6**	**1.340**	**365.93**

Note: Δ_{err}: Maximum flat attenuation amplitude error. *: Simulated results, NA: No data. ϕ_{var}: Maximum relative insertion phase variation between minimum and maximum attenuation.

Attenuators should provide a high attenuation range with low flat amplitude error (Δ_{err}) and low insertion phase variation (ϕ_{var}) within wide bandwidth. Therefore, to compare the overall performances with those of the state-of-the-art wideband attenuators, the figure of merit (FoM) is defined as (10) in terms of Δ, ϕ_{var}, attenuation range, and FBW.

$$\text{FoM} = \frac{\text{FBW}(\%) \times \text{A}_{\text{range}}\,(\text{dB})}{\varphi_{\text{var}}\,(\text{deg}) \times \Delta_{err}(dB)} \tag{10a}$$

where

$$\text{A}_{\text{range}} = \text{Maximum attenuation}\,(\text{dB}) - \text{Minimum attenuation}\,(\text{dB}) \tag{10b}$$

As seen from (10), the FoM is inversely proportional to the ϕ_{var} and Δ_{err}, Thus, the small Δ_{err} and ϕ_{var} must be guaranteed within the operating bandwidth for high FoM.

The performance comparison of the proposed variable attenuators with previously reported attenuators is shown in Table 3. As seen from the table, the CMOS digital attenuators have excellent performances in terms of bandwidth, however, their fabrication cost is excessive. Besides, the proposed attenuators provide the low amplitude and phase variation over the wide bandwidth among the previously reported analog attenuators.

4 | CONCLUSION

Wideband reflection-type analog variable attenuators with simultaneous minimized flat amplitude error and insertion phase variation are theoretically analyzed and experimentally demonstrated using PIN diode. The parasitic components of the PIN diode, which are the main cause of degrading amplitude error and insertion phase variation, are compensated with one or two-stage series transmission lines and shunt capacitors. For experimental validation, two prototypes of the proposed analog attenuators (design-I and design-II) are designed and fabricated for 1 GHz bandwidth at a center frequency of 3.5 GHz. The proposed attenuators provide very small amplitude error and phase variation among the state-of-arts analog attenuators. Although digital attenuators in CMOS and MMIC technology can provide flat attenuation with small amplitude error and phase variation in microwave and millimeter frequency ranges, their design time and fabrication cost are excessive. Further, CMOS or MMIC attenuator designs for the UHF band or relatively low-frequency bands are almost impossible due to the relatively huge size and fabrication cost. The proposed circuit will be very advantageous in many applications such as next-generation communication systems, MIMO antenna systems, and accurate RF signal control systems.

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DATA AVAILABILITY STATEMENT

I confirm that my Data Availability Statement complies with the Expects Data Policy.

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REFERENCES

1. Dogan H, Meyer RG. Intermodulation distortion in CMOS attenuators and switches. *IEEE J Solid-State Circuits*. 2007; 42(3):529-539.
2. Hlali A, Zairi H. Performance analysis of dynamically controllable terahertz grounded coplanar waveguide attenuator based on graphene using wave concept iterative process method. *Int J RF Microwave Comput-Aid Eng*. 2021;31:e22517. https://doi.org/10.1002/mmce.22517.
3. Nehring J et al. Highly integrated 4–32-GHz two-port vector network analyzers for instrumentation and biomedical applications. *IEEE Trans Microw Theory Tech*. 2017;65(1): 229-244.
4. Kang DW et al. Single and four-element Ka-band transmit/receive phased-Array silicon RFICs with 5-bit amplitude and phase control. *IEEE Trans Microw Theory Tech*. 2009; 57(12):3534-3543.
5. Sim S, Jeon L, Kim J-G. A compact X-band bi-directional phased-array T/R chipset in 0.13 μm CMOS technology. *IEEE Trans Microw Theory Tech*. 2013;61(1):562-569.
6. Hong S et al. Applications of self-interference cancellation in 5G and beyond. *IEEE Commun Mag*. 2014;52(2):114-121.
7. Lee J, Oh T, Moon J, Song C, Lee B, Lee I. Hybrid beamforming with variable attenuator for multi-user mmWave systems. *IEEE Trans Vehicular Technol*. 2020;69(8):9131-9134.
8. Nawaz H, Niazi A, Chaudhry SM. High isolation, proximity-fed monostatic patch antennas with integrated self-interference cancellation taps for ISM band full duplex applications. *Int J RF Microwave Comput-Aid Eng*. 2021;3:e22484. https://doi.org/10.1002/mmce.22484.
9. Yuan Y, Mu S, Guo Y. 6-bit step attenuators for phased-array system with temperature compensation technique. *IEEE Microwave Wireless Compon Lett*. 2018;28(8):690-692.
10. Huang Y-Y, Woo W, Jeon H, Lee C-H, Kenney JS. Compact wideband linear CMOS variable gain amplifier for analog-predistortion power amplifiers. *IEEE Trans Microw Theory Tech*. 2012;60(1):68-76.
11. Cheng W, Alink MSO, Annema AJ, Wienk GJM, Nauta B. A wideband IM3 cancellation technique for CMOS II- and T-attenuators. *IEEE J Solid-State Circuits*. 2013;48(2):358-368.
12. Wang K, Zhou T, Zhang H, Qiu L. A 28-40 GHz digital step attenuator with low amplitude and phase variations. *IEEE Microwave Wireless Compon Lett*. 2021;31(1):64-67.

13. Pakasiri C, Zhu F, Wang S. A 4-bit ultra-wideband complementary metal-oxide semiconductor attenuator with low root-means-square amplitude error. *Int J RF Microwave Comput-Aid Eng*. 2019;29:e21922. https://doi.org/10.1002/mmce.21922.
14. Kim K, Min B-W. V-W band CMOS distributed step attenuator with low phase imbalance. *IEEE Microw Wireless Compon Lett*. 2014;24(8):548-550.
15. Huang Y-Y, Woo W, Yoon Y, Lee C-H. Highly linear RF CMOS variable attenuators with adaptive body biasing. *IEEE J. Solid-State Circuits*. 2011;46(5):1023-1033.
16. Song I, Cho M, Cressler JD. Design and analysis of a low loss, wideband digital step attenuator with minimized amplitude and phase variations. *IEEE J Solid-State Circuits*. 2018;53(8): 2202-2212.
17. Zhao C, Zeng X, Zhang L, et al. A 37-40 GHz low phase imbalance CMOS attenuator with tail-capacitor compensation technique. *IEEE Trans Circuits Sys-I Regular Papers*. 2020;67(10): 3400-3408.
18. Ahmadikia A, Karami P, Atarodi SM. Analysis and design of a DC to 18 GHz 6-bit attenuator with simultaneous phase and gain error correction. *Int J Electron Commun (AEU)*. 2019;110:152829. https://doi.org/10.1016/j.aeue.2019.152829.
19. Bulja S, Grebennikov A. Variable reflection-type attenuators based on varactor diodes. *IEEE Trans Microw Theory Tech*. 2012;60(12):3719-3727.
20. Trent CR, Weller TM. S-band reflection type variable attenuator. *IEEE Microw Wirel Compon Lett*. 2002;12(7): 243-245.
21. Pierantoni L, Mencarelli D, Bozzi M, et al. Broadband microwave attenuator based on few layer graphene flakes. *IEEE Trans Microw Theory Tech*. 2015;63(8):2491-2497.
22. Yasir M, Bistarelli S, Cataldo A, Bozzi M, Perregrini L, Bellucci S. Enhanced tunable microstrip attenuator based on few layer graphene flakes. *IEEE Microw Wirel Compon Lett*. 2017;27(4):332-334.
23. Zhang A, Lu W, Liu Z, Chen H, Huang B. Dynamically tunable substrate-integrated-waveguide attenuator using graphene. *IEEE Trans Microw Theory Tech*. 2018;66(6):3081-3089.
24. Kang W, Chang I, Kang M. Reflection-type low-phase attenuator. *IEEE Trans Microw Theory Tech*. 1998;46(7):1019-1021.
25. Shireesha C, Sadhu R, Harikumar R. X-band voltage variable attenuators using PIN diodes. *IEEE Int Microw RF Conf*. 2014; 323-326.
26. Kim Y, Shim S, Moon T, Chaudhary G, Jeong Y. Mathematical analysis of novel low phase deviation variable attenuator. *Proceeding Asia-Pacific Microw Conf*. 2010;1743-1746.
27. Sun K, Choi M, Weide D. A PIN diode controlled variable attenuator using a 0-dB branch-line coupler. *IEEE Microw Wirel Compon Lett*. 2005;15(6):440-442.
28. Eom D, Lee H. An X-band substrate integrated waveguide attenuator. *Microw Opt Tech Lett*. 2014;56(10):2446-2449.
29. Eom D, Lee H. Broadband half mode substrate integrated waveguide attenuator in 7.29-14.90 GHz. *IEEE Microw Wirel Compon Lett*. 2015;25(9):564-566.
30. Cheng KM, Chik MJ. A varactor-based variable attenuator design with enhanced linearity performance. *IEEE Trans Microw Theory Tech*. 2015;63(10):3191-3198.
31. Nam S, Ashtiani AE, Oztek-Yerli CF, Robertson ID. Wideband reflection type MMIC attenuator with constant phase. *Electron Lett*. 1998;34(1):91-93.
32. Chaudhary G, Jeong Y. Reflection-type topologies with arbitrary wideband flat group delays using coupled lines. *IEEE Access*. 2018;6:3310-3319.
33. HSMP-381x,481x, Surface mount RF PIN low distortion attenuator diodes, Avago technologies.
34. Model X3C35F1-03S, Surface mount Hybrid Coupler 3 dB 90°, Anaren.

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