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Best Demo Award

Design of High Efficient CMOS RF Energy Harvesting Rectifier
using a Body Bias Feedback

Junsik Park, Seungwook Lee, and Yongchae Jeong
전북대학교

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IDEC SoC Congress
Design of High Efficient CMOS RF Energy Harvesting Rectifier using a Body Bias Feedback
Joonh Park, Seungyeon Lee, and Yongbae Jeong
jeong@knu.ac.kr
Chonbuk National University, Republic of Korea

1. OUTLINE
This paper presents a design of CMOS RF energy harvesting rectifier using a body bias feedback technique and low-pass filter for high conversion efficiency. Some portion of DC output voltage is applied to the body of MOSFET in a feedback loop to increase the bias voltage. Furthermore, it is possible to increase the conversion efficiency by suppressing the harmonic components generated by the MOSFET and flattening DC signal using an in-pass filter. The test network was optimized for the optimum conversion efficiency at carrier frequency of 2.44 GHz. From the results, output voltage of 1~2 V and power conversion efficiency of 20% or more is obtained for an input power of 3~10 dBm.

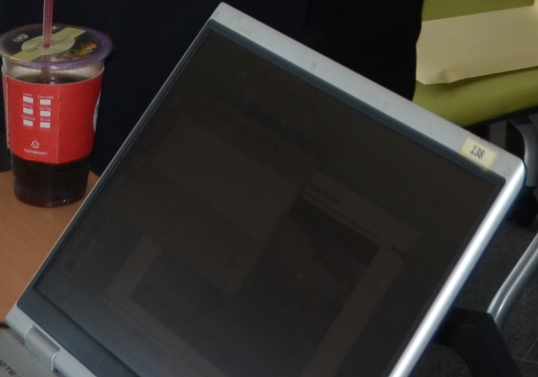
2. INTRODUCTION
Recent developments in wireless communication such as ubiquitous sensor networks and RF energy harvesting technology in the RF energy utilization technology. Energy harvesting systems that harvest the RF energy from the available DC power. Efficiency of the electronic device applied to major components that make rectifier / receiver as well as mobile device.

3. DESCRIPTION
The proposed rectifier, first designed in Dongbu 0.11 μm RF CMOS technology using thick oxide devices for Wi-Fi application around 2.44 GHz. The overall chip area is 770 × 580 μm² including bonding pads. From the results, the proposed RF energy harvesting rectifier has a maximum conversion efficiency of 22% at the input power of 10 dBm. At this condition, it is able to generate the 2.8 V of DC output voltage from the charging capacitor.

4. CHIP IMPLEMENTATION AND RESULTS
The proposed rectifier, first designed in Dongbu 0.11 μm RF CMOS technology using thick oxide devices for Wi-Fi application around 2.44 GHz. The overall chip area is 770 × 580 μm² including bonding pads. From the results, the proposed RF energy harvesting rectifier has a maximum conversion efficiency of 22% at the input power of 10 dBm. At this condition, it is able to generate the 2.8 V of DC output voltage from the charging capacitor.



이승욱





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IEEE SoC Congress

Design of High Efficient CMOS RF Energy Harvesting Rectifier using a Body Bias Feedback

1. OUTLINE

The paper presents a design of CMOS RF energy harvesting rectifier using a body bias feedback technique and the proposed rectifier structure. In order to increase the rectifier efficiency, a body bias feedback technique is proposed. It is possible to control the rectifier efficiency by adjusting the body bias voltage. The proposed rectifier structure is implemented in a 65nm CMOS technology. The rectifier efficiency is measured at various frequencies of 1.2 GHz. The proposed rectifier structure shows a higher rectifier efficiency than the conventional rectifier structure.

2. CHIP IMPLEMENTATION AND RESULTS

The proposed rectifier chip is implemented in a 65nm CMOS technology. The chip is fabricated using a standard CMOS process. The rectifier efficiency is measured at various frequencies of 1.2 GHz. The proposed rectifier structure shows a higher rectifier efficiency than the conventional rectifier structure.

3. CONCLUSION

The proposed rectifier structure shows a higher rectifier efficiency than the conventional rectifier structure. The proposed rectifier structure is suitable for CMOS RF energy harvesting applications.

4. REFERENCES

[1] S. K. Lee, K. S. Lee, C. M. Lee, "Design of High Efficient CMOS RF Energy Harvesting Rectifier using a Body Bias Feedback Technique," *IEEE SoC Congress*, 2013.

5. CONTACT

Dr. S. K. Lee, E-mail: sklee@kist.ac.kr

박준식 04192

이동통신

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DEC CoC Congress

Design of High Efficient CMOS RF Energy Harvesting Rectifier using a Body Bias Feedback

Seung-Ho, Sangwon Lee, and Taehwan Kim
KAIST Graduate School, Republic of Korea

1. OUTLINE
This paper presents a design of CMOS RF energy harvesting rectifier using a body bias feedback technique and the design for high conversion efficiency. The proposed rectifier is implemented in the 65nm CMOS technology. To improve the conversion efficiency, the body bias feedback technique is used to reduce the forward voltage drop. Furthermore, it is possible to improve the conversion efficiency by implementing the body bias feedback technique to the rectifier circuit. The proposed rectifier is simulated using the HSPICE simulator. The simulation results show that the proposed rectifier can harvest the RF energy efficiently. The proposed rectifier can harvest the RF energy efficiently. The proposed rectifier can harvest the RF energy efficiently.

2. INTRODUCTION
The energy harvesting technique is one of the most important techniques for the development of the wireless sensor network. The energy harvesting technique is one of the most important techniques for the development of the wireless sensor network. The energy harvesting technique is one of the most important techniques for the development of the wireless sensor network.

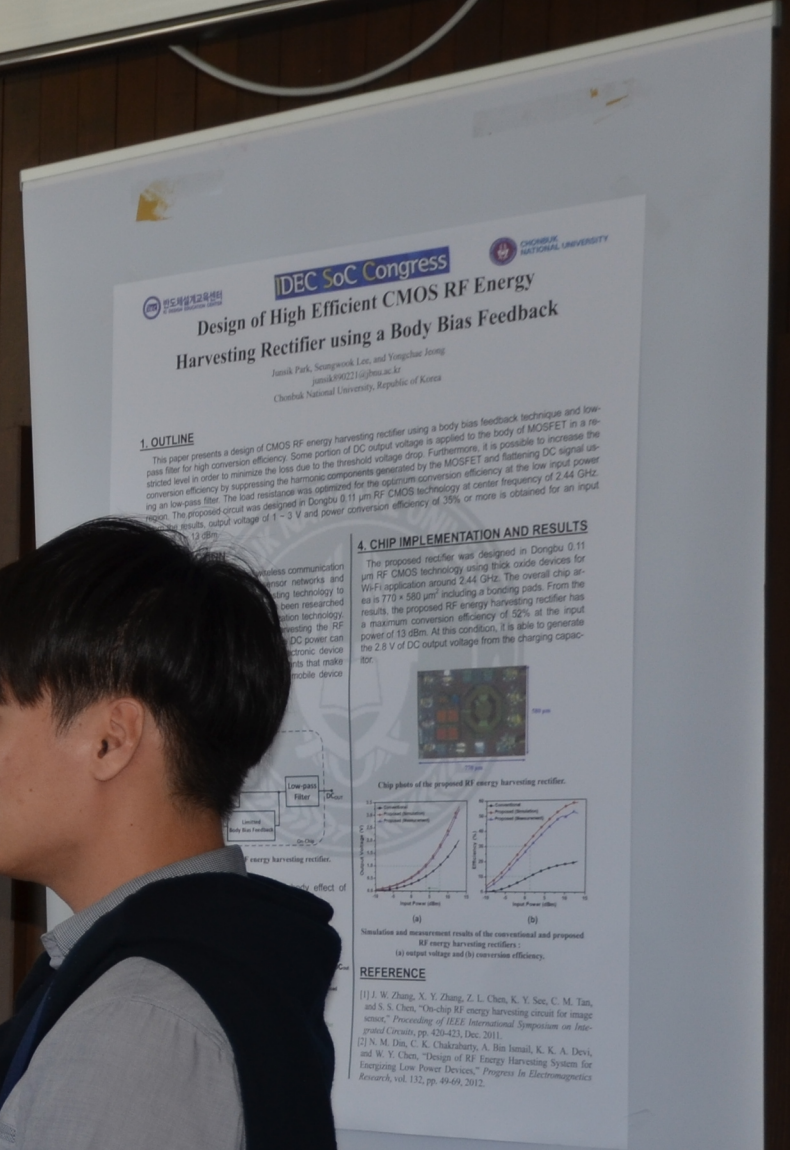
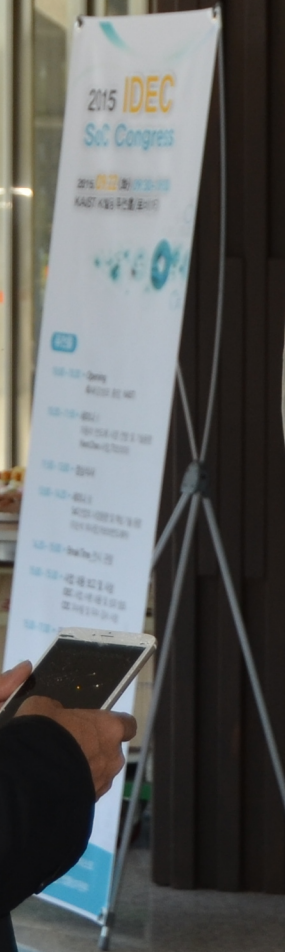
3. CIRCUIT DESCRIPTION
The proposed rectifier consists of a CMOS RF energy harvesting rectifier using a body bias feedback technique and the design for high conversion efficiency. The proposed rectifier is implemented in the 65nm CMOS technology. To improve the conversion efficiency, the body bias feedback technique is used to reduce the forward voltage drop. Furthermore, it is possible to improve the conversion efficiency by implementing the body bias feedback technique to the rectifier circuit. The proposed rectifier is simulated using the HSPICE simulator. The simulation results show that the proposed rectifier can harvest the RF energy efficiently.

4. CONCLUSION
The proposed rectifier can harvest the RF energy efficiently. The proposed rectifier can harvest the RF energy efficiently. The proposed rectifier can harvest the RF energy efficiently.

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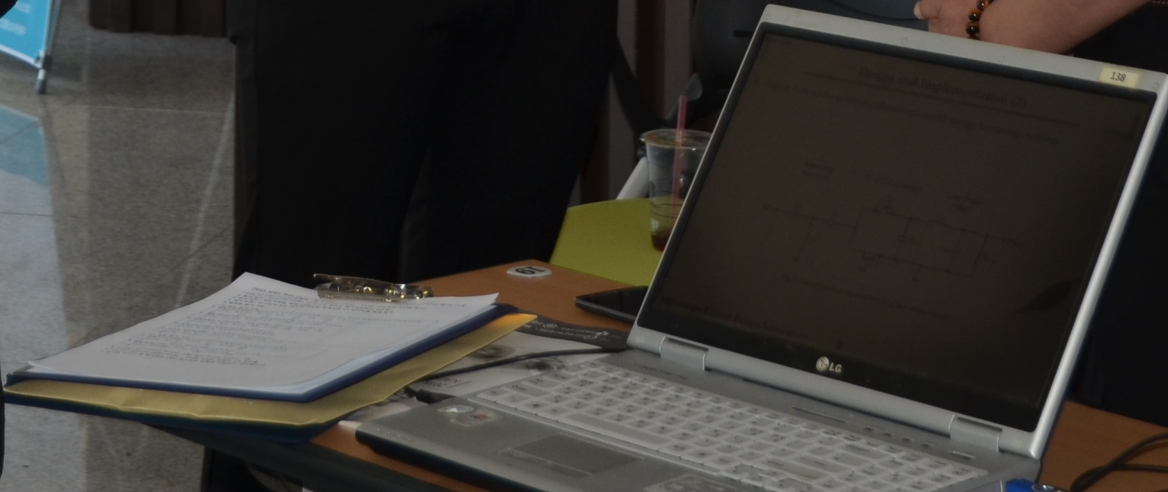
IDEC SoC Congress
Design of High Efficient CMOS RF Energy Harvesting Rectifier using a Body Bias Feedback
Jaehuk Park, Seungwook Lee, and Yongjae Jeong
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Cheonbuk National University, Republic of Korea

1. OUTLINE
This paper presents a design of CMOS RF energy harvesting rectifier using a body bias feedback technique and low-pass filter for high conversion efficiency. Some portion of DC output voltage is applied to the body of MOSFET in a regulated level in order to minimize the loss due to the threshold voltage drop. Furthermore, it is possible to increase the conversion efficiency by suppressing the harmonics components generated by the MOSFET and flattening DC signal using an RF matching network. The load resistance was optimized for the maximum conversion efficiency at the low input power range. The proposed circuit was designed in Dongbu 0.11 μm CMOS technology at carrier frequency of 2.44 GHz. The proposed circuit shows output voltage of 1~3 V and power conversion efficiency of 30% or more is obtained for an input power of 13 dBm.

4. CHIP IMPLEMENTATION AND RESULTS
The proposed rectifier was designed in Dongbu 0.11 μm RF CMOS technology using 8K3 die oxide devices for WiFi application around 2.44 GHz. The overall chip area is 770 × 580 μm² including a bonding pads. From the results, the proposed RF energy harvesting rectifier has a maximum conversion efficiency of 30% at the input power of 13 dBm. At the condition, it is able to generate the 2.5 V of DC output voltage from the charging capacitor.

Simulation and measurement results of the conventional and proposed RF energy harvesting rectifiers:
(a) output voltage and (b) conversion efficiency.

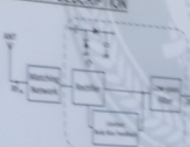
REFERENCE
[1] J. W. Zhang, X. Y. Zhang, Z. L. Chen, K. Y. Seo, C. M. Tan, and S. S. Chen, "On-chip RF energy harvesting circuit for image sensor," *Proceeding of IEEE International Symposium on Integrated Circuits*, pp. 420-423, Dec. 2011.
[2] N. M. Dao, C. K. Chakrabarty, A. Bin Islam, K. K. A. Devi, and W. S. Chen, "Design of RF Energy Harvesting System for Energizing Low Power Devices," *Progress in Electromagnetics Research*, vol. 132, pp. 49-69, 2012.



DEC SoC Congress
Design of High Efficient CMOS RF Energy Harvesting Rectifier using a Body Bias Feedback
 Jaeh-Park, Sangyeop Lee, and Donghwan Jung
 Samsung Electronics Co., Ltd.
 Chonbuk National University, Republic of Korea

1. OUTLINE
 This paper presents a design of CMOS RF energy harvesting rectifier using a body bias feedback technique and the pass filter for high conversion efficiency. Some portion of DC output voltage is applied to the body of MOSFET in an order to increase the conversion efficiency. Some portion of DC output voltage is applied to the body of MOSFET in an order to increase the conversion efficiency by suppressing the harmonic components generated by the MOSFET and lowering DC output voltage on low-conductance state. The test measurement was performed for the system conversion efficiency at the low input power region. The proposed circuit was designed in 0.18 μm CMOS technology at carrier frequency of 2.44 GHz. From the results, output voltage of 1 ~ 1.5 V and power conversion efficiency of 20% or more is obtained for an input power of 2 ~ 12 dBm.

2. INTRODUCTION
 With the rapid development of wireless communication technology such as localization sensor networks and RFID system, the RF energy harvesting technology is one of the alternative energy utilization technologies. RF energy harvesting system that harvests the RF signal power to replenish the available DC power can improve the power efficiency of the electronic device since it can be applied to major components that make up the transmitter/receiver as well as mobile device [1].

3. CIRCUIT DESCRIPTION

 Block diagram of proposed RF energy harvesting rectifier.
 The threshold voltage (V_{th}) with the body effect of transistor can be given as [2]:

$$V_{th} = V_{th0} + \gamma \sqrt{2\phi_F + V_{sb}} - \gamma \sqrt{2\phi_F}$$
 where V_{th0} is the threshold voltage of the transistor and V_{sb} is the substrate bias voltage.

4. CHIP IMPLEMENTATION AND RESULTS
 The proposed rectifier was designed in 0.18 μm CMOS technology using 99% metal device for high-conductance state. L-match network was used for 77.1 Ω input impedance matching. The overall chip area is 0.15 mm^2 including a loading area. From the results, the proposed RF energy harvesting rectifier has a maximum conversion efficiency of 20% at the input power of 10 dBm. At the condition, it is able to generate the 2.1 V of DC output voltage from the charging capacitor.

REFERENCE
 [1] J. N. Zhang, S. Y. Zhang, L. J. Chen, X. Y. Shi, L. W. Shi, and S. Y. Chen, "70-dBm RF energy harvesting circuit for sleep mode," *Proceeding of IEEE International Symposium on Intelligent Systems and Knowledge Engineering*, pp. 429-432, Dec. 2011.
 [2] N. W. Shi, C. K. Chaudhary, N. Shi, and S. Y. Chen, "Design of RF Energy Harvesting System for Supporting Low Power Device," *Program in Electromagnetic Research*, vol. 12, pp. 80-88, 2012.

Design of multimedia system controller with low-A processor

System architecture

Chip photo

Chip photo

Two men in light blue shirts and dark ties are looking at a small electronic device held by one of them. They are standing in a hallway with other people and posters in the background.

A man in a dark suit is looking at a clipboard with papers. He is standing in a hallway with other people and posters in the background. There are laptops and other equipment on a table in front of him.

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DEC soC Congress
Design of High Efficient CMOS RF Energy Harvesting Rectifier using a Body Bias Feedback

1. OUTLINE

2. INTRODUCTION

3. CIRCUIT DESCRIPTION

4. CHIP IMPLEMENTATION AND RESULTS

REFERENCES

The rectifier voltage (V_{rect}) with the body effect feedback can be given as:

$$V_{rect} = V_{DD} - V_{th} - V_{gs}$$

Design of multimedia system controller with low-4 process

Table 1: Performance Comparison

Parameter	Proposed	Reference [1]	Reference [2]
Area (μm ²)	1.2	1.5	1.8
Power (mW)	0.5	0.8	1.0
Efficiency (%)	85	75	70
Bandwidth (MHz)	10	15	20

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Design of High Efficient CMOS RF Energy Harvesting Rectifier using a Body Bias Feedback

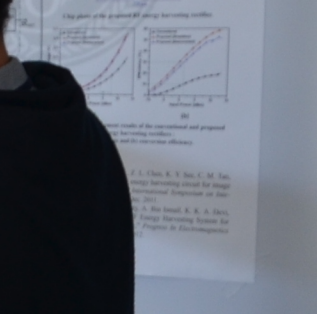
Yoon-Pil Park, Sangwon Lee, and Sangwon Hong
POSTECH, Pohang, Republic of Korea

1. OUTLINE

The paper presents a design of CMOS RF energy harvesting rectifier using a body bias feedback technique and low noise floor for high conversion efficiency. Some authors of DC output voltage are applied to increase the output level in order to maximize the harvestable energy. Furthermore, it is possible to increase the conversion efficiency by supporting the harvestable energy generated by the MOSFET gate feedback DC signal as a body bias. The low noise floor is supported by the gate feedback technique in series frequency of 1.84 GHz. The proposed rectifier was designed in 65nm CMOS technology and the measured efficiency of 30% at the input power of 0.1 mW and output voltage of 1.2 V and load impedance of 50 Ω is demonstrated for an input power of 0.1 mW.

4. CHIP IMPLEMENTATION AND RESULTS


The proposed rectifier was designed in 65nm CMOS technology and implemented on a 1.5x1.5 cm² silicon die. The overall chip size is 1.5 x 1.5 cm² including a bonding pad. From the measurement results, the proposed RF energy harvesting rectifier has a maximum conversion efficiency of 30% at the input power of 0.1 mW. In this condition, it is able to generate the 1.2 V of DC output voltage from the incoming power of 0.1 mW.



Design of multimedia with Core-A processor

Multimedia system controller

- Feature list
 - Core-A with JTAG (on-chip debugger)
 - AMBA BUS
 - DDR, SRAM, SPI, I2C
 - Memory
 - SRAM, FLASH, MEMORY, DRAM
 - Peripherals
 - UART, Ethernet, Bluetooth, UART, USB 2.0, PCI, SPI
- Distinct features
 - Support processor debugging through On-chip debugger
 - Support instruction/data cache memory
- Design verification
 - FPGA verification board including multimedia I/O
 - Various power output for FPGA and peripheral units
 - Kernel debugger emulator board for debugging
 - Support various memory - SRAM, FLASH, DDR, SD card
 - Support Video/Audio output through D-sub port
 - Ethernet, Bluetooth, USB 2.0, UART
- Chip Test
 - Chip function test
 - Chip power pin test : pass
 - Chip I/O test : pass
 - Core-A debugger test
 - Core-A register read/write : pass
 - Core-A memory read/write : pass
 - Core-A break/watch point set/reset : pass
 - Core-A instruction test : pass
 - Core-A cache memory test : fail
 - unstable cache memory
 - Chip demonstration
 - Core-A debugger working



Two men in business attire are engaged in a discussion. One man is holding a folder and a pen, while the other is gesturing towards a laptop on the table. A black messenger bag is slung over the man on the left.

Workstation setup on a table including:

- An LG laptop displaying a "Demonstration Video" with a spectrum plot showing a signal between -10 and 0 dBm.
- A mouse and keyboard.
- A name tag on the table that reads "박준식" (Park Jun-sik) and "전북대학교" (Jeonju National University).
- A brochure for the "2015 IDEC SOC Congress" is also visible on the table.

Another workstation setup on the right side of the table, featuring a laptop displaying a software interface with various data fields and graphs.



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DEC SoC Congress

Design of High Efficient CMOS RF Energy Harvesting Rectifier using a Body Bias Feedback

Seok Park, Sangmin Lee, and Hocheol Park
Department of Electronic Engineering
Chonbuk National University, Republic of Korea

1. OUTLINE
This paper presents a design of CMOS RF energy harvesting rectifier using a body bias feedback technique and compares the high conversion efficiency. Some portion of DC output voltage is applied to the body of M1/M2ET in a common source level to increase the bias voltage in the feedback loop. Furthermore, it is possible to increase the conversion efficiency by separating the feedback capacitance generated by the M1/M2ET and feedback DC signal outputting in the same level. The test prototype was fabricated for the optimum conversion efficiency at the input power range. The proposed circuit was designed in 0.18μm CMOS technology at central frequency of 2.44 GHz region. The measured output voltage of 2.1 V is achieved with conversion efficiency of 30%, or more is obtained for an input power of 10 dBm.

2. INTRODUCTION
With the rapid development of wireless communication systems, the demand for portable wireless systems and IoT systems has increased. In order to reduce the power consumption of these systems, energy harvesting technology is one of the most promising energy harvesting technologies. The energy harvesting system that separates the DC and AC signals is a promising technology. However, the conversion efficiency of the rectifier is a major concern that needs to be improved. In this paper, we propose a new method for the rectifier.

3. CIRCUIT DESCRIPTION
The proposed rectifier consists of a common source level and a feedback loop. The feedback loop is connected to the body of M1/M2ET in a common source level. The feedback loop is connected to the body of M1/M2ET in a common source level. The feedback loop is connected to the body of M1/M2ET in a common source level.

4. CHIP IMPLEMENTATION AND RESULTS
The proposed rectifier was designed in 0.18μm CMOS technology using the test prototype. The measured output voltage of 2.1 V is achieved with conversion efficiency of 30%, or more is obtained for an input power of 10 dBm. The proposed RF energy harvesting rectifier has a conversion efficiency of 30% at the input power of 10 dBm. In this conference, it is also presented that the 2.1 V of DC output voltage from the energy capacitor.

REFERENCE
[1] W. Zhang, X. Y. Peng, J. L. Chen, X. Y. Sun, C. M. Sun, and S. Y. Chen, "Highly efficient energy harvesting circuit for energy sensor," *Proceedings of 2012 International Symposium on Design, Automation & Test in Europe*, pp. 439-443, Jun. 2012.
[2] M. Wu, X. Y. Peng, J. L. Chen, X. Y. Sun, C. M. Sun, and S. Y. Chen, "Design of RF Energy Harvesting System for Energy Sensor," *Proceedings of 2012 International Symposium on Design, Automation & Test in Europe*, pp. 444-448, Jun. 2012.

Design of multimedia sys with Core-A processor

Multimedia system controller

- Feature list
 - Main processor: Core-A multi-IO (on-chip debugger)
 - ASBIA BUS
 - Cache: SRAM, DRAM
 - Memory: SRAM, DRAM, FLASH memory, SD/MMC
 - Peripherals: I2C, Ethernet, Bluetooth, UART, USB 2.0, PCI, SPI
- Distinct features
 - Support processor debugging through On-chip debugger
 - Support instruction/data cache memory

Design verification

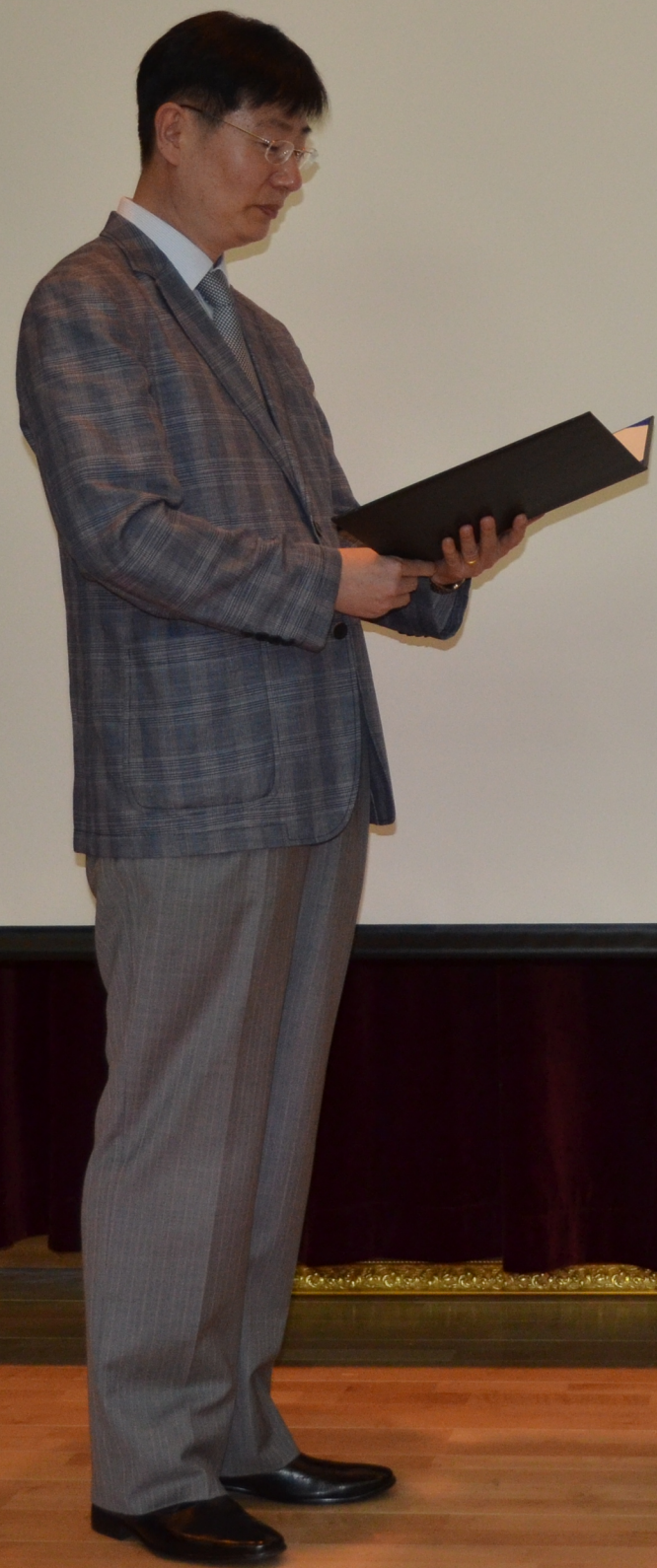
- FPGA board test
 - FPGA verification board including multimedia I/O
 - Various power output for FPGA and peripheral units
 - Embedded debugger simulator board for debugging
 - Support various memory - SRAM, FLASH, DDR, SD card
 - Support Video/Audio output through D-sub port
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 - unstable cache memory
 - Chip demonstration
 - Core-A debugger working



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2015 IDEC SoC Congress

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